

TO: John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)
FROM: Dennis Pak (408)974-4874
IEEE P1285 Liaison to X3T9.2/DADI
DATE: November 10, 1993
SUBJECT: P1285 Liaison Report for November 1993

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o One controller, multiple slaves model
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

The first draft for review of the logical layer is ready. Please contact Martin Freeman (freeman@cis.stanford.edu) for a copy of the draft.

The document defines the following topics:

- o Command block structure & status format
- o Transfer unit description & operation

- o Control & Status Register (CSR) definition - both common & device specific
- o Identification of potential physical layers (PCI, RamLink, SerialBus, etc.)

The group is currently reviewing the document for technical content and additional clarification. At the same time, the group is trying to understand issues associated with implementing P1285 over PCI. The plan is to include an appendix at the back of a later draft showing a PCI implementation. Other physical levels are also being studied.

Upcoming Events

P1285 tentative meeting dates and locations:

November	11/10/93	@Co-located meeting, Colorado Springs, CO
December	12/2/93	@Quantum Corp, 500 McCarthy Blvd, Milpitas, CA
January	1/6/94	@Apple Computer, 1 Infinite Loop, Cupertino, CA
February	2/3/94	@Quantum Corp, 500 McCarthy Blvd, Milpitas, CA
March	3/4/94	@Apple Computer, 1 Infinite Loop, Cupertino, CA

These meetings are normally scheduled from 2:00-5:00 PM (except the co-located meeting). Please contact Martin Freeman at (415)354-0329 for exact date and location, or for additional information.