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Subject: Ultra-SCSI Timing Proposal

1. Summary

This is a proposal for a new, faster, backward compatible version of the interlocked SCSI bus. The changes below add two optional "ultra-speed" sets of timing parameters to the SCSI-3 SPI document. The new timing options allow the SCSI data phase to transfer at rates of 40 and 80 MBytes per second on a 16 bit parallel bus.

It is expected that these timing values will only be practical on certain bus implementations, but this limitation is not embedded in the speed control mechanism. This is the same approach used in the current fast timing selection method.

3. Changes to Text

All the changes proposed here apply to the SCSI-3 SCSI Parallel Interconnect (SPI) document.

4. Synchronous Data Transfer Request (SDTR) Message

Faster timings must be signalled to the chip in some fashion. The current method uses the Transfer Period specified in the SDTR message to control the timing selection. This proposal simply expands this method as follows.

Transfer type	async	sync	fast	ultra-1	ultra-2
Transfer period factor	0	>50	>25	>12	>6
Transfer period (nsec)	async	>200	>100	>50	>25
Megatransfers/second	0-5	0-5	5-10	10-20	20-40
MByte/sec on wide bus	0-10	0-10	10-20	20-40	40-80

5. Timing Parameters

The following timing parameters must be changed to support the two levels of Ultra-SCSI. This version of the proposal simply has the current fast values divided by two or four for ultra-1 and ultra-2 timing, but this may need to be changed based on chip implementation issues.

Timing Parameter	sync	fast	ultra-1	ultra-2
Transfer period (nsec)	200	100	50	25
Transmit assertion period	80	30	15	7
Transmit negation period	80	30	15	7
Transmit hold time	53	33	16	8
Transmit setup time	23	23	11	5
Receive assertion period	70	22	11	5
Receive negation period	70	22	11	5
Receive hold time	25	25	12	6
Receive setup time	15	15	7	3