X3T9.2/93-168

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cc:
From: John Masiewicz
Date: 11/02/93 05:17:31 PM
Subject: ATA-2 Draft Comments from 10/28 SSWG

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At the October 26-27 ATA-2 working group, I presented my comments against X3T9.2 working draft 948D (dated Sep 1, 1993). After much discussion, the committee asked me to update my comments as agreed by the group. The following comments and tables should reflect the general consensus and provide input to the editors for the next draft revision.
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The Tables at the end of this document include the agreed-upon changes discussed at the 10/26-27 ATA-2 working groups in Milpitas. It was decided at that time to divide the tables into ATA-1 and ATA-2 specific tables.

In addition to the tables, the following changes were agreed to:

> Electrical descriptions would be removed from the signal descriptions and described in the electrical descriptions. The following tables include driver type, electrical, loading, and termination (Pull-ups) required or allowed. The editors will remove references to electrical specifications elsewhere in the ATA-2 document as part of their re-write for ATA-2. (e.g. references to pull-ups, open-collector, TTL compatible, etc)

> All references to "TTL Compatible" will be removed and specific electrical specifications will be detailed in the electrical section.

> The comment in section 4.5 that "Cable length may be exceeded" will be removed.

> Section 4.5 I/O cable capacitance comment will be removed and included in the cable electrical specifications section.

> Deassertion of DMACK will be allowed for the host to suspend DMA transfers. Timing diagrams and text will be changed as necessary.

> A warning note on sharing DMARQ and INTRQ with non-ATA devices will be included in the notes for the ATA-1 and ATA-2 Electrical Characteristics.

> Delete note in section 5.2.10 which says "Some drives may negate INTRQ on a PIO data transfer completion, except on a single sector read or on the last sector of a multi-sector read".

> Section 5.2.14 Reset timing, change paragraph to read: "This signal from the host shall be asserted beginning with the

application of power and held asserted until at least 25 usec after the voltage levels have stabilized to the minimum operating voltage of the device, and negated thereafter unless some event requires that the device(s) again be reset.

> D.4.5 and D.4.6, remove statement "Devices shall hold this signal negated if the function is not implemented."

> Editor to add note that timings are at device connector.

X.X.X ATA-1 Driver Types and Allowed Pull-ups

The table below represents the generally accepted driver/receiver and terminations used for ATA-1. Most of these were not specified by the ATA-1 specification, but have been adopted de-facto by the industry. New I/O transfer modes added by ATA-2 may not work with the following ATA-1 drivers and loading. See tables 3 and 4 for ATA-2 driver types and terminations.

Signal	Source	Driver Type	Pull-up at Host	Pull-up at Each Device	Notes
Reset	Host	TP			
DD 0:15	Bidir.	TS	8.2-10K		Note 1
DMARQ	Device	TP	5.6K PD		Note 1,2
DIOR- DIOW-	Host	TS	4.7-8.2K		Note 1
IORDY	Device	OC/TS	1.0K		Note 1,3
SPSYNC/CSEL					Note 4
CSEL	Host		Ground	10K	Note 2,5
SPSYNC	Device	TS/OC		VU	Note 6
DMACK-	Host	TP			
INTRQ	Device	TS	2.2K-8.2K		Note 1
IOCS16-	Device	OC	300		Note 1
DA0:2	Host	TP			
PDIAG-	Device	TP			
CS0- CS1-	Host	TP			
DASP-	Device	OC		10K	Note 4

Table 1 - ATA-1 Driver Type and Allowed Pull-ups

Table 1 NOTES

Note 1: Pull-up resistors normally associated with ISA/EISA busses may be seen by ATA devices in unbuffered implementations, These pull-ups reside only on the Host, not on the devices. The use of these pull-ups were not defined by ATA-1 and this summary is provided for informational purposes.
Note 2: Some host systems use 5.6K pull-down on this line. ATA-1 specified a pull-down but did not specify value or location. EISA specified 5.6K pull-down at Host. ATA-1 permitted use of totem-pole drivers. If the system cannot tolerate totem-pole driver due to non-ATA signal-sharing applications, appropriate buffering or series protection resistor (up to 47 ohm) should be employed at the host or ATA adapter.
Note 3: If TS is used, should be "sink only". If actively asserted, this signal should only be enabled during DIOR/DIOW cycles to the selected device.
Note 4: See signal descriptions for information on dual use of this signal.
Note 5: When used as CSEL, Line is grounded at Host and 10K Pull-up is required at both devices.
Note 6: When Used as SPSYNC, application is vendor unique.

X.X.X ATA-1 Electrical Characteristics

The following table represents the generally accepted driver and receiver specifications used for ATA-1. The source and sink specifications in ATA-1 were widely ignored by the industry, and the threshold voltages listed below are by general agreement. New I/O transfer modes added by ATA-2 may not work with the following ATA-1 drivers and loading. See Tables 3 and 4 for ATA-2 compatible electrical characteristics and loading.

	Description	Min	Max
IoL	Output LOW current, 5V operation, @ 0.5V (Table 1 loading)(Note 1)	12mA	
IoL	Output LOW current, 3.3V operation @ 0.5V (Table 1 Loading)(Note 1)	8mA	
IoH	Output HIGH current @ 2.4V (Table 1 Loading)	-400uA	
Vih	Voltage Input High	2.0 V	
Vil	Voltage Input Low		0.8 V
Voh	Voltage Output High (Ioh = -400 u A)	2.4 V	
Vol	Voltage Output Low (5V, Iol = 12ma)		0.5 V
	Cable Capacitive Loading		200pF

Table 2 - ATA-1 Electrical Characteristics

Table 2 NOTES

Note 1: IoL on IOCS16 is 16 ma because ISA/EISA systems use pull-up resistors on IOCS16 as low as 300 Ohms. In these applications, IoL of 12ma may not be sufficient to guarantee VoL.

X.X.X ATA-2 Driver Types and Required Pull-ups

Signal	Source	Driver Type	Pull-up at Host	Pull-up at each Device	Notes
Reset	Host	TP			
DD 0:15	Bidir.	TS			
DMARQ	Device	TS	5.6K PD		Note 1
DIOR- DIOW-	Host	TS			
IORDY	Device	TS	1.0K		Note 2
SPSYNC/CSEL					Note 3
CSEL	Host		Ground	10K	Note 4
SPSYNC	Device	TS/OC		VU	Note 5
DMACK-	Host	TP			
INTRQ	Device	TS			
IOCS16-	Device	OC	1.0K		
DA0:2	Host	TP			
PDIAG-	Device	TP			
CS0- CS1-	Host	TP			
DASP-	Device	OC		10K	Note 3

Table 3 - ATA-2 Driver Types and Required Pull-ups

TABLE 3 NOTES

All resistor values are minimum (lowest) allowed.

Note 1: ATA-2 defines this line to be tri-stated whenever the device is not selected or is not executing a DMA data transfer. When enabled by DMA transfer, it will be driven high and low by the device.
Note 2: This signal should only be enabled during DIOR/DIOW cycles to the selected device.
Note 3: See signal descriptions for information on dual use of this signal.
Note 4: When used as CSEL, Line is grounded at Host and 10K Pull-up is required at both devices.
Note 5: When Used as SPSYNC, application is vendor unique.

X.X.X ATA-2 Electrical Characteristics

The following table should be used for ATA-2 applications which use PIO Mode 3 or greater and DMA Mode 1 or greater where table 3 loading is used.

	Description	Min	Max
IoL	Output LOW current, 5V operation, @ 0.5 V with Thevinin Load Rt > 700 Ohms at equiv Voltage of 3.0 V Load Capacitance CL < 50pf	4mA	
IoH	Output HIGH current @ 2.4V with Thevinin Load Rt > 700 Ohms at equiv Voltage of 3.0 V Load Cap CL < 50pf	-4ma	
Vih	Voltage Input High	2.0 V	
Vil	Voltage Input Low		0.8 V
Voh	Voltage Output High	2.4 V	
Vol	Voltage Output Low		0.5 V
Vol	Voltage Output Low		0.5 V
Cin	Input Capacitance (of Device)		25 pf
Cout	Output Capacitance (of Device)		25 pf
tRISE	Rise time for any signal on AT interface (Note 1)	5ns	
tFALL	Rise time for any signal on AT interface (Note 1)	5ns	

Table 4 - ATA-2 Electrical Characteristics

Table 4 NOTES

Note 1: tRISE and tFALL are measured from 0.5V to 2.8V with a resistive load of 1K Ohm and a capacitive load of 50 pF.

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Section 10.3 Add the following definitions:

TS - "Tri-State"

OC - "Open Collector"

TP - "Totem-Pole"

PU - "Pull-up"

PD - "Pull-down"