

Accredited Standards Committee\*  
**X3, Information Processing Systems**

**Doc. No.:** X3T9.2/93-166R0

**Date:** August 11, 2000

**Project:**

**Ref. Doc.:**

**Reply to:** S. Finch

To: Membership of X3T9.2

From: Lamers/Finch

Subject: Minutes of X3T9.2 Disk Drive Working Group November 8, 1993

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**Agenda**

1. Opening Remarks
2. Attendance and Membership
3. Approval of Agenda
4. Document Distribution
5. ATA Working Group Goals and Methods
6. Report on X3T9.2 ATA Working Group Meeting, October 26-27
7.
  - 7.1 SFF ATAPI/SSWG (Hanan)
  - 7.2 Activities centered on 528 MB Limitations
8. General Working Group Items
  - 8.1 Format Track Logical Block (X3T9.2/92-185) [Lamers]
  - 8.2 ATA DMA Issues (X3T9.2/93-110r4) [Landis]
  - 8.3 Download Microcode (X3T9.2/93-xxx) [McGrath]
  - 8.4 20 MB/s Issues (X3T9.2/93-xxx) []
    - 8.4.1 Interface Modeling (X3T9.2/93-xxx) [Wallace]
    - 8.4.2 Transfer Timings (X3T9.2/93-xxx) [Geldman]
    - 8.4.3 PIO Flow Control (X3T9.2/93-xxx) [Geldman]
    - 8.4.4 New Read Protocol (X3T9.2/93-xxx) [Geldman]
9. New Business
  - 9.1 Power Management (X3T9.2/93-xxx) [Landis]
  - 9.2 Shared Interrupts (X3T9.2/93-xxx) [Jesup]
  - 9.3 Set Multiple Compliance (X3T9.2/93-xxx) [Jesup]
  - 9.4 Better Information Setup & Boot Commands (X3T9.2/93-xxx) [Jesup/Landis]
  - 9.5 ATAPI Project Proposal (X3T9.2/93-xxx) []
  - 9.6 MMC Project Proposal (X3T9.2/93-xxx) []
10. Review of ATA-2 (X3T9.2/948D)
  - 10.1 Comments (X3T9.2/93-xxx) []
  - 10.2 Issues related to SFF-8011 (X3T9.2/93-xxx) []

11. Meeting Schedule

12. Adjournment

## **Results of Meeting**

### **1. Opening Remarks**

Steve Finch, the Chair, called the meeting to order at 2:00 p.m., Monday, December 8, 1993. He thanked Bob Dugan of IBM for hosting the meeting.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by X3T9.2 and would be conducted under the X3 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the X3T9.2 task group. The voting rules for the meeting are those of the parent committee, X3T9.2. These rules are: one vote per company; and any participating company member may vote.

The minutes of this meeting will be posted to the SCSI BBS and the SCSI Reflector and will be included in the next committee mailing.

### **2. Attendance and Membership**

Attendance at working group meetings does not count toward minimum attendance requirements for X3T9.2 membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

The following people attended the meeting:

## Meeting Attendees

Name	S	Organization	Electronic Mail Address
Mr. Richard Kalish		Adaptec	rkalish@rahul.net
Mr. David Skinner	P	Advanced Micro Devices	dave.skinner@amd.com
Mr. John Geldman	A	Cirrus Logic Inc.	johng@cirrus.com
Mr. Roger Wang	O	CMD Technology	
Mr. Lane Lee	O	Conner Peripherals	
Mr. Burt Wagner		Deadline Specialists	
Mr. Scott Pirdy	O	DEC	
Mr. I. Dal Allan	P	ENDL	2501752@mcimail.com
Mr. Robert Liu	P	Fujitsu Computer Products	
Mr. Steve King		Hewlett Packard	king@mail.boi.hp.com
Dr. Sam Karunanithi		Hitachi Micro Systems	
Mr. Robert Kembel	O	IBM Corp.	rkembel@vnet.ibm.com
Mr. Lawrence J. Lamers	P	Maxtor Corp.	larry_lamers@maxtor.com
Mr. Peter Brown		Oak Technology	brown@oaktech.com
Mr. J. Schaffner	O	Qlogic	j_schaffner@qlc.com
Mr. Hale Landis	A	Seagate Technology	Hale_Landis@notes.seagate.com
Mr. Gene Milligan	A	Seagate Technology	Gene_Milligan@notes.seagate.com
Mr. Brian Schott		Seagate Technology	Brian_Schott@notes.seagate.com
Mr. John Masiewicz		Seagate Technology	Masiewicz@notes.seagate.com
Mr. Stephen G. Finch	P	Silicon Systems, Inc.	5723283@mcimail.com
Mr. Dean Wallace	O	Infinity Microelectronics	
Mr. Tom Hanan	O	Western Digital	hanan_t@a1.wdc.com

Status Key: P - Principal  
 A - Alternate  
 O - Observer  
 L - Liaison  
 S,V - Visitor

### 3. Approval of Agenda

The proposed agenda was approved.

### 4. Document Distribution

X3T9.2/93-165r0 Local Bus Physical Interface Simulation Results  
 X3T9.2/93-157r2 Proposed 20 MB/s ATA Timing Extensions

### 5. ATA Working Group Goals and Methods

Steve Finch discussed his view on ATA and the working group. ATA(1) is done and off for publication as a standard. The immediate goal is to get ATA-2 in shape and ready for further processing. ATA-2 is fixing some problems in ATA(1), adding some features, and increasing the transfer rates. Follow-on ATA's should be looked at as coming on an annual basis.

Steve noted that there is a need to get the current information on ATA out to the world at large.

Steve will generate a rev 2 of ATA-2 that indicates it is under construction so that it does not look like a finalized document.

**6. Report on X3T9.2 ATA Working Group Meeting, October 26-27**

**7. Liason Reports**

**7.1 SFF ATAPI/SSWG (Hanan)**

Tom Hanan reported.

**7.2 Activities centered on 528 MB Limitations**

Hale Landis reported. Existing implementation problems with high capacity drives in the BIOS and software area has caused the development of a proposed SFF specification. A meeting is scheduled during Comdex to get industry input on the problems.

**8. General Working Group Items**

**8.1 Format Track Logical Block (X3T9.2/92-185) [Lamers]**

Drop it.

**8.2 ATA DMA Issues (X3T9.2/93-110r4) [Landis]**

John Geldman offered the following definition "DMA data phase is active anytime DMACK- is asserted".

The only way to interrupt a DMA transfer is with soft reset. Hale intends to propose this for all commands instead of writing the command register again.

Word 52 is intended as single-word DMA transfer cycle timing. Tom will develop a proposal.

Hale suggested adding a word for which level ATA is implemented. Also the IDENTIFY DRIVE command needs to be made mandatory.

If the READ DMA command completes without error the command block registers contain the address (CHS or LBA) of the last sector transferred.

If the READ DMA command encounters an error the command is terminated (DRQ is negated). The command block registers contain the address (CHS or LBA) of the sector where the first error occurred.

Transfer of data in error during a dma command was not resolved.

SET FEATURES command must be supported if multi-word DMA is supported.

The default mode for dma transfers at power on were not resolved.

If the WRITE DMA command completes without error the command block registers contain the address (CHS or LBA) of the last sector transferred.

If the WRITE DMA command encounters an error the command is terminated (DRQ is negated). The command block registers contain the address (CHS or LBA) of the sector where the first error occurred.

Command complete when BSY and DRQ are both zero.

Hale stated that the setup and initialize phases need to be reversed to prevent the DMA transfers from taking off. This is just the opposite of ATA-1. What needs to be done is have the drive selected before initializing the DMA channel.

Tom pointed out a potential problem when the host wants to abort the command after it is set up. The group expressed a concern with understanding this and ask Tom to document it.

### **8.3 Download Microcode (X3T9.2/93-xxx) [McGrath]**

Hale - customers will ask for it and implementation can be costly; exposure to virus; other processes may be needed to make the new code usefull.

Larry Lamers voiced a similar concerns, but admitted that it is almost inevitable that the feature will in ATA-2.

## **8.4 20 MB/s Issues (X3T9.2/93-xxx) []**

### **8.4.1 Interface Modeling (X3T9.2/93-165) [Wallace]**

See the minutes of the last wg mtg.

### **8.4.2 Transfer Timings (X3T9.2/93-157) [Geldman]**

John Geldman brought in a revised proposal. The flow control for PIO is still a major unresolved issue.

John stated that section 8 of the proposal was not updated to reflect the latest thinking due to time constraints. Also there is not a consensus on what it should be pending the outcome of the simulations.

The text description for t0 add the word minimum for clarification.

### **8.4.3 PIO Flow Control (X3T9.2/93-xxx) [Geldman]**

Jim McGrath stated that there is concern about being able to fabricate a part with the speeds needed to use IORDY. The issue was put off till December.

### **8.4.4 New Read Protocol (X3T9.2/93-xxx) [Geldman]**

## **9. New Business**

### **9.1 Power Management (X3T9.2/93-167) [Landis]**

Hale Landis made a presentation of a new concept for documenting the commands. This would result in a more structured and explicit document. The group was in favor of adopting this approach to documenting the commands.

**9.2 Shared Interrupts (X3T9.2/93-xxx) [Jesup]**

**9.3 Set Multiple Compliance (X3T9.2/93-xxx) [Jesup]**

**9.4 Better Information Setup & Boot Commands (X3T9.2/93-xxx) [Jesup/Landis]**

**9.5 ATAPI Project Proposal (X3T9.2/93-xxx) []**

**9.6 MMC Project Proposal (X3T9.2/93-xxx) []**

**10. Review of ATA-2 (X3T9.2/948D)**

**10.1 Comments (X3T9.2/93-168) [Masiewicz]**

Revised proposal submitted.

**10.2 Issues related to SFF-8011 (X3T9.2/93-xxx) []**

**11. Meeting Schedule**

The meetings that are planned as of this meeting are:

- December 8, 1993 - Milpitas, CA
- January 10, 1994 - San Diego, CA
- January 28, 1994 - Milpitas, CA

## **12. Adjournment**

The meeting was adjourned at 7:00 p.m. on Monday November 8, 1993.