PIO Mode 4 Handshake Flow Control 93-162r0

To: X3T9.2 Membership
Editor: John Geldman, Cirrus Logic
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Subject: Description of PIO Mode 4 REQ/ACK Handshake Flow Control

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The following document provides a written description of the PIO REQ/ACK Handshake flow control mechanism which has been discussed in several Local Bus Working Group meetings. At this time, there has not been a decision or even a consensus on using this mechanism (as opposed to extending the IORDY flow control mechanism).

General Description

This PIO Handshake protocol defines extensions to the ATA standard necessary to allow modern PC and IDE Peripheral designers to provide products with data transfer rates up to 22 megabytes per second.

This description includes suggested:
PIO Mode 4 transfer timings (from Multiword DMA Mode 2);
Identify Drive and Set Features Command Changes; and
Suggested protocol description.

PIO Mode 4 Transfer Timings

TABLE 1: New PIO Handshake Timing Parameters

	PIO Data Handshake timing parameters	Mode 4 nsec Min	Max
t0	Cycle time	**	
tD	DIOR-/DIOW-	50	
tE	DIOR- data access		30
tF	DIOR- data hold	5	
tG	DIOW- data setup	20	
tH	DIOW- data hold	5	
tI	DMACK to DIOR-/DIOW- setup	0	
tJ	DIOR-/DIOW- to DMACK hold	5	
tKr	DIOR- negated pulse width	25	
tKw	DIOW- negated pulse width	25	
tLr	DIOR- to DMREQ delay		30
tLw	DIOW- to DMREQ delay		30
tZ	DMACK- to tristate (2)		25

(0) The specifications in this chart only apply for transfers to the

Data Register. All other accesses should use the specifications in the chart for PIO Mode 3.

(1) tC and tFZ timings from the Multiword DMA Transfer Timing Table have been dropped.

(2) This parameter specifies the time from the negation edge of DMACK- to the time that the data bus is no longer driven by the device (tristate). The tZ parameter applies only at the end of a multiword PIO Handshake cycle, i.e., when DMACK is negated. The device may actively drive the data bus or may tristate the data bus while DMACK- is active from the first time that DIOR- is asserted until DMACK- is negated as long as tE and tF requirements are met.

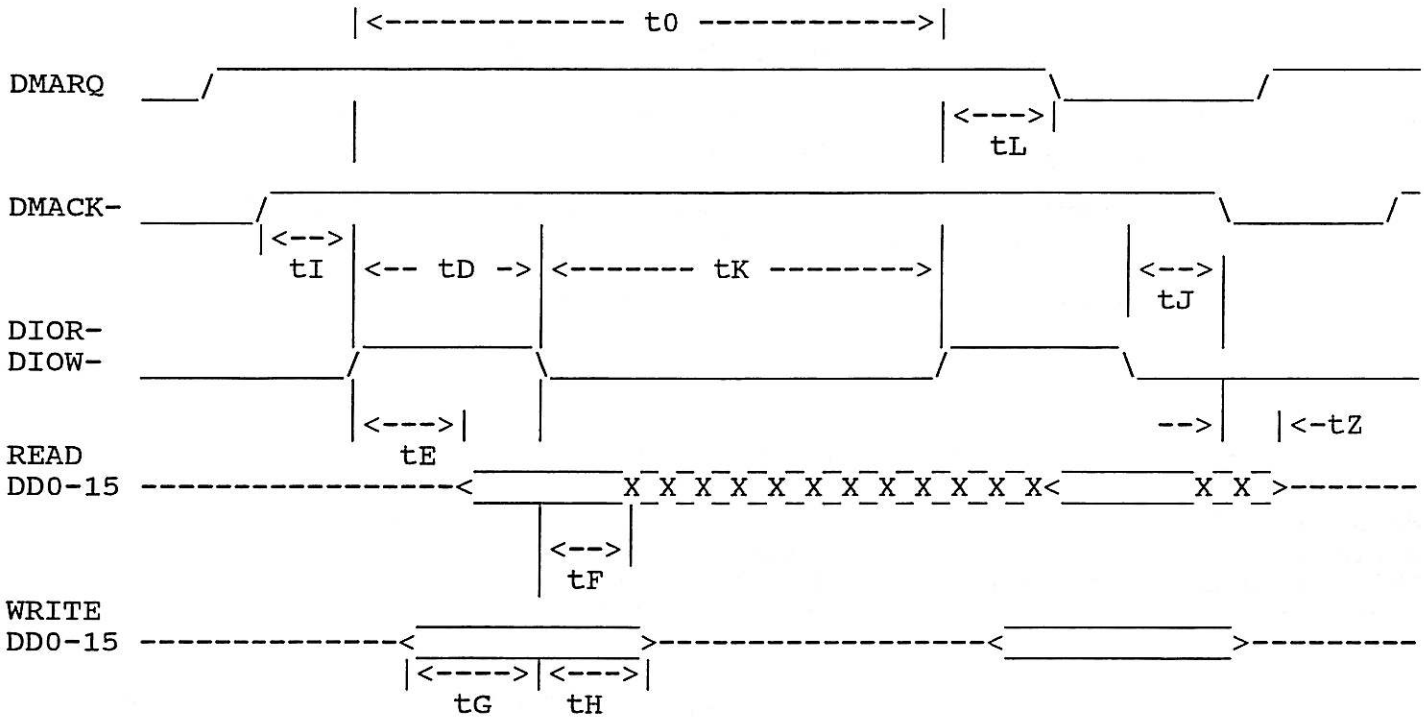


FIGURE 1: Mode 4 PIO Handshake Timing Diagram

Identify Drive and Set Features Command Changes

Two additional words have been added to the Identify Drive command. The first additional word indicates the minimum cycle time, in nanoseconds, supported by the device in PIO Mode 4.

Devices which support PIO mode 4 must support PIO Handshake flow control.

The second word specifies the manufacturer's recommended PIO Handshake cycle time.

TABLE 2: New Identify Drive Parameters

Word		Description
53	15-2	Reserved
	1	1 = the fields reported in words 64-70 are valid 0 = the fields reported in words 64-70 are not valid
	0	(as defined in ATA Standard)
64	15-8	Reserved
	7-0	Advanced PIO Transfer Modes Supported
69		Minimum Transfer Cycle Time per Word for PIO Mode 4
	15-0	Cycle Time in nanoseconds
70		Manufacturer's Recommended PIO Mode 4 Transfer Cycle Time
	15-0	Cycle Time in nanoseconds

Minimum Transfer Cycle Time Per Word for PIO Mode 4

Word 69 of the parameter information of the Identify Drive command is defined as the Minimum Transfer Cycle Time Per Word for PIO Mode 4. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing PIO Mode 4 transfers on a per word basis.

Devices which support PIO mode 4 must support PIO Handshake flow control.

For devices which support PIO Mode 4, the value in word 69 shall not be less than 90.

Any device which supports PIO Mode 4 must support this field.

If this field is supported, bit 1 of word 53 must be set.

If bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

Manufacturer's Recommended Transfer Cycle Time Per Word for PIO Mode 4

Word 70 of the parameter information of the Identify Drive command is defined as the Manufacturer's Recommended PIO Mode 4 Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector Read or Write commands over all locations on the media under nominal conditions. A cycle time less that this value may cause DMARQ to be negated at a rate which may reduce throughput, without data corruption.

The value in word 70 shall not be less than the value in word 69.

Any device which supports PIO Mode 4 must support this field.

If this field is supported, bit 1 of word 53 must be set.

If bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

Changes to the Set Features Command

The Set Features command is utilized to select the active PIO and DMA Modes. In the ATA standard, the Set Features command with the Set Transfer Mode parameter utilizes the Sector Count Register to specify which transfer parameter to change and the value to be implemented. The use of the term "Block Transfer" is herein changed to PIO Default Transfer Mode and redefined. The Sector Count Register values are changed to:

PIO Default Transfer Mode	00000 0nn
PIO Flow Control Transfer Mode x	00001 nnn
Single Word DMA Mode x	00010 nnn
Multiword DMA Mode x	00100 nnn
Reserved	01000 nnn

where "nn" or "nnn" is a valid mode number for the associated transfer type.

(Editor's note: It is intended that the reserved values be used for future specification of an alternative flow control mechanism.)

If a device does not support the mode specified, the device posts an Aborted Command error.

If a device supports this specification, and receives a Set Feature command with a Set Transfer Mode parameter and a Sector Count Register value of "00000 000", it shall set its default PIO transfer mode. If the value is "00000 001" and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

Suggested Protocol Overview

Commands can be grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if BSY=1, and should proceed no further unless and until BSY=0. For most commands, the host will also wait for DRDY=1 before proceeding. Those commands shown with DRDY=x can be executed when DRDY=0.

The PIO Mode 4 protocol with REQ/ACK Handshake is different from the other PIO protocols in that an intermediary is assumed. This intermediary is the bridge logic which allows the host to process the established PIO protocol, while the drive executes a slightly different protocol. In general, the INTRQ signal is produced by the drive and processed normally by the host, and the DMARQ signal is produced by the drive and processed by the bridge logic.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of ATA drives.

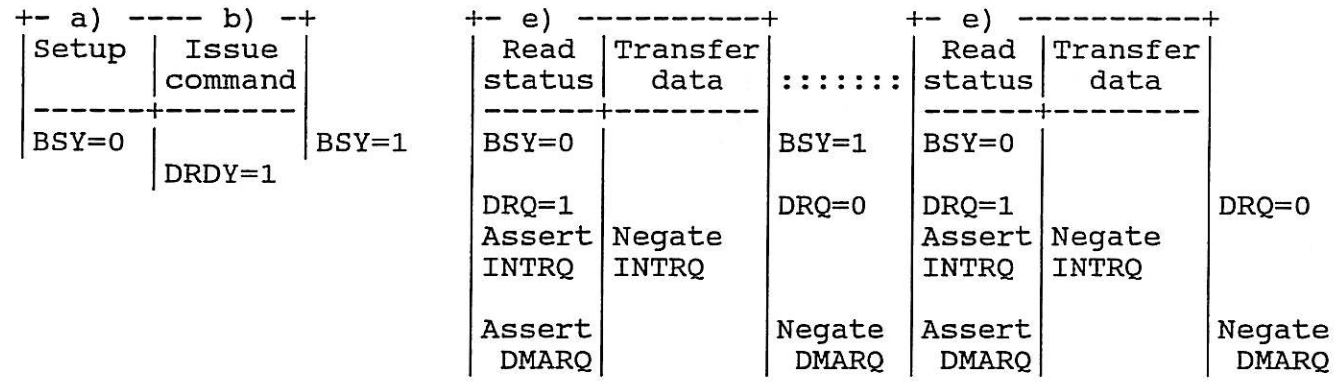
PIO data in commands

This class includes:
- Identify drive
- Read buffer
- Read long
- Read sector(s)

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

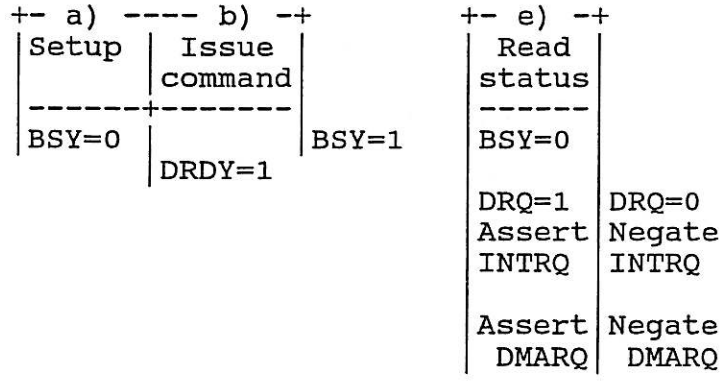
a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
b) The host writes the command code to the Command Register.
c) The drive sets BSY and prepares for data transfer.
d) When a sector of data is available, the drive sets DRQ and clears BSY prior to asserting INTRQ and DMARQ. This assertion should be simultaneous.
e) After detecting INTRQ, the host reads the Status Register, then reads one sector of data via the Data Register. In response to the Status Register being read, the drive negates INTRQ. The DMARQ and DACK signals are used to control flow using a demand protocol between the intermediary adapter and the drive. These signals are not passed to the host.
f) The drive clears DRQ and negates DMARQ. If transfer of another sector is required, the drive also sets BSY and the above sequence is repeated from d).

PIO read command



If Error Status is presented, the drive is prepared to transfer data, and it is at the host's discretion that the data is transferred.

PIO Read aborted command



Although DRQ=1, there is no data to be transferred under this condition.

PIO data out commands

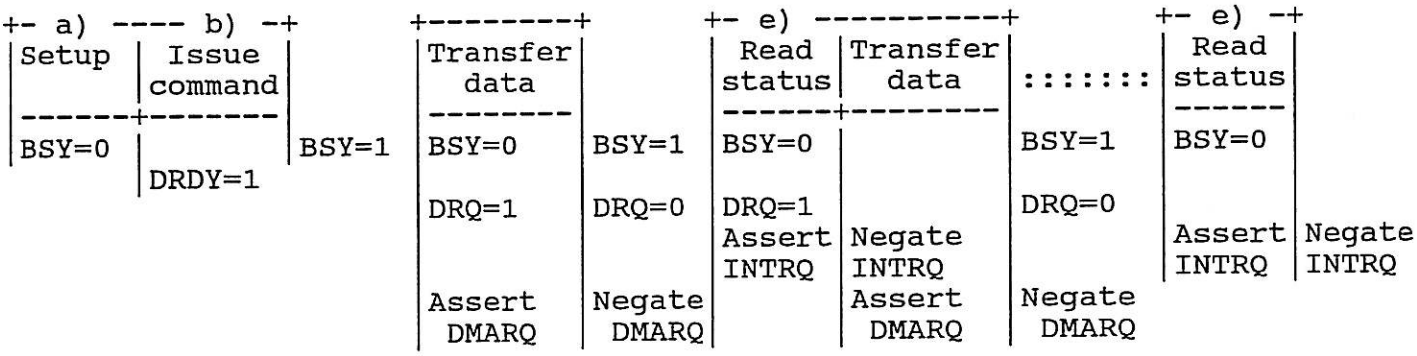
This class includes:
- Format
- Write buffer
- Write long
- Write sector(s)

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the drive to the host.

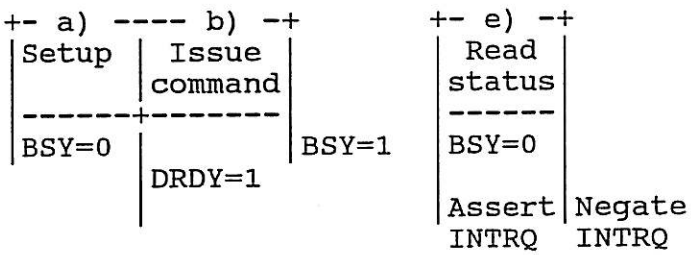
a) The host writes any required parameters to the Features, Sector

Count, Sector Number, Cylinder and Drive/Head registers.
b) The host writes the command code to the Command Register.
c) The drive sets DRQ and asserts DMARQ when it is ready to accept the first sector of data.
d) The host writes one sector of data via the Data Register.
e) The drive clears DRQ and sets BSY.
f) When the drive has completed processing of the sector, it clears BSY, asserts INTRQ, and negates DMARQ. If transfer of another sector is required, the drive also sets DRQ and re-asserts DMARQ.
g) After detecting INTRQ, the host reads the Status Register.
h) The drive clears the interrupt.
i) If transfer of another sector is required, the above sequence is repeated from d).

PIO write command



PIO write aborted command



Non-data commands

This class includes:
- Execute drive diagnostic (DRDY=x)
- Idle
- Initialize drive parameters (DRDY=x)

- Read power mode
- Read verify sector(s)
- Recalibrate
- Seek
- Set features
- Set multiple mode
- Standby

Execution of these commands involves no data transfer.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
b) The host writes the command code to the Command Register.
c) The drive sets BSY.
d) When the drive has completed processing, it clears BSY and asserts INTRQ.
g) The host reads the Status Register.
h) The drive negates INTRQ.

Miscellaneous commands

This class includes:
- Read multiple
- Sleep
- Write multiple
- Write same

The protocol for these commands is contained in the individual command descriptions.