93-157

93-157R2

To: X3T9.2 Membership

Editor: John Geldman, Cirrus Logic

Date: November 5, 1993

Subject: Proposed 20 MByte/Sec ATA Timing Extension

This document was originally published as 93-143r0. However, this number had already been assigned. The orginal revision of this document should be referred to as 93-157R0, and the current revsion should be referred to as 93-157R2.

The following document contains modified sections from the SFF Specification Draft on ATA Timing Extensions. These sections have been enhanced to include the higher 20 MByte/Sec bandwidth modes. The section documenting proposed receiver, capacitence, cable and termination specifications has had major revisions since the Rev 0 version of this document (Per the Sept. 29th meeting). In the Oct. 27th meeting these electrical specifications changed considerably again. The latest cabling environment is not stable not been captured in this revision. Also a new section was been added describing an enhanced PIO Data In protocol (Discussed in the Sept. 29th and Oct. 27th meetings).

This activity has moved from the Small Form Factor Committee (SFF) to a X3T9.2 SSWG. This group is still actively working on this document and implementor's are forewarned against use of this information until formally approved.

There seems to be general consensus on the new Multiword DMA Mode 2 timings. Also, there is continuing discussion on the appropriate flow control mechanism for PIO Mode 4. The two mechanisms under question are enhanced use of IORDY (20 nanosecond timing) and a new PIO REQ/ACK handshake mechanism. The timings for PIO Mode 4 using IORDY also seem to be stable.

The three main active discussion areas affecting this proposal are:

- IORDY vs PIO REQ/ACK flow control
- Electrical characteristics and cabling
- An improved PIO Data In protocol

The main changes in this version are editorial in nature:

- The word active was replaced with asserted
- The word inactive was replaced with negated
- In Table 1, values for t0 were added and note 0 to explain them
- In Figure 1, a dashed line was added to indicate that DMARQ does not have to be negated between words
- In Table 2, values for t0 were added and note 0 to explain them
- In Table 2, Tr was changed to Trd
- In Table 2, note 5 was added
- Figure 2 was modified to separate the events of the negation of IOCS16- and the assertion of DIOR-/DIOW-
- In Section 8.3, a reference to TTL was removed
- Section 9.0 was mildly wordsmithed
- An alternative flow for Section 9.1 was added

Comments are welcome. Editorial comments (spelling, grammar, punctuation) can be addressed directly to the editor. Any technical comments should be addressed to the ATA Working Group for discussion.

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6. New Timing Modes

In order to achieve higher data transfer rates new timing modes are defined: two for Multiword DMA data transfers and two for PIO data transfers.

6.1 Definition Of Cycle Time For New Timing Modes

For PIO Modes 0, 1 and 2, and Multiword DMA Mode 0, the timing parameters defined the operating characteristics that the device was required to support if it supported the associated mode. In particular, if the device supported PIO Mode 2, for example, then it was required to support a minimum cycle time of 240 nanoseconds (t0 for PIO Mode 2).

The use of IORDY is optional in the ATA standard. Because of this, devices reported support of the various PIO modes only if they could support the mode without use of IORDY. This was done to prevent problems between a device that could support a timing mode only if IORDY is used for flow control and a host which supports the same timing mode but without flow control . Thus a drive might report that it supported only lower transfer speeds, when in fact they could support a higher transfer rate if flow control was used.

A new word has been added to the Identify Drive command to indicate the minimum cycle time supported by the device in PIO mode without the use of IORDY as flow control. This word specifies the minimum cycle time, in nanoseconds, supported by the device in PIO Modes 3 and 4 when IORDY is not being used. The value contained in this word must always be greater than or equal to the minimum cycle time defined by the highest PIO Mode supported. E.g., a drive supporting PIO Mode 3 timing could not report a value less than 180 nanoseconds, the minimum cycle time defined for Mode 3 PIO Timings.

Investigation into methods of increasing the transfer rate of the ATA interface, a number of new transfer rates seemed to be desirable. PIO Mode 2 had a transfer rate of 8.33 megabytes per second. There seemed to be a need to support a transfer rate of 10 megabytes per second, 11 megabytes per second, etc. The problem got worse when DMA data rates were discussed. It appeared that many new timing modes would have to be added, and this was not acceptable.

Rather than adding a series of new modes, it was decided that simply by changing the definition of, or really the usage of, the cycle time parameter, t0, and the inclusion of additional information in the Identify Drive command, that it was possible to support a wide range of speed increments that could be easily identified by the host and reflect the maximum transfer capabilities of a particular implementation.

With the addition of PIO Mode 3, PIO Mode 4, Multiword DMA Mode 1 and Multiword DMA Mode 2, the definition of Cycle Time, t0, has been changed to the minimum cycle supported by this mode. The definition of the remaining timing parameters associated with the new modes is not changed. If a device supports one of a new modes it MUST meet the timing requirements for all timing specification associated with that mode with the possible exception of the Cycle Time. Remember that PIO Modes 0,1 and 2, and Multiword DMA Mode 0 must be compatible with the ATA Standard.

New words have been added to the Identify Drive command to indicate the minimum cycle time supported by the device in PIO Mode 3, PIO Mode 4, Multiword DMA Mode 1 and Multiword DMA Mode 2. These words specify the minimum cycle time, in nanoseconds, supported by the device in each associated Mode . The value contained in each of these words must always be greater than or equal to the minimum cycle time defined by the associated Mode. E.g., a drive supporting PIO Mode 3 timing could not report a value less than 180 nanoseconds, the minimum cycle time defined for Mode 3 PIO Timings.

Additional words were added for the new Multiword DMA Modes . These words specify the manufacturer's recommended Multiword DMA cycle time. This parameter addresses the needs of the host system in obtaining maximum performance. While a hardware implementation may be able to burst at a very high transfer rate, it may not be able to sustain this transfer rate over an entire transfer. The result might be that, if the maximum burst rate is utilized, a lower overall transfer rate would be experienced than if a slower transfer rate was used. By adjusting the transfer rate to that recommended by the manufacturer, performance under nominal conditions should be maximized.

It is expected that, if future PIO Modes or Multiword DMA Modes are added, that they will follow these new definitions.

6.2 New Multiword DMA Transfer Mode

New Multiword DMA Transfer Modes are defined and identified as Mode 1 and Mode 2. The timing parameters associated with Multiword DMA Transfer Mode 1 and Mode 2 are defined in Table 1. Peripherals reporting support for Multiword DMA Transfer Mode 1 must also support Multiword DMA Transfer Mode 0. Peripherals reporting support for Multiword DMA Transfer Mode 2 must also support Multiword DMA Transfer Mode 1 and Mode 0. Figure 1 shows the basic timing for Multiword DMA Transfers and is included to show the new timing parameter tZ.

The minimum value of t0 is specified by the device in word 65 of the Identify Drive information. Refer to section 7.1.6 for a description of word 65.

TABLE 1: New Multiword DMA Timing Parameters

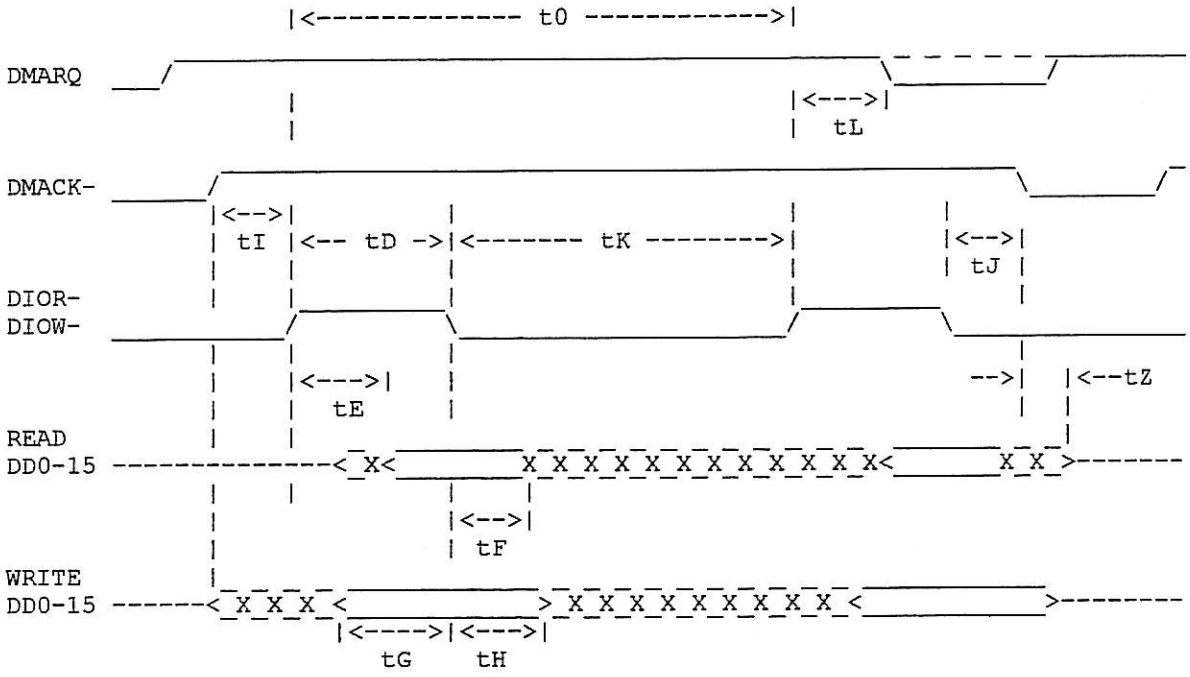
	Multiword DMA timing parameters	Mode 1 nsec		Mode 2 nsec	
		Min	Max	Min	Max
t0	Cycle time (0)	150		100	
tC	DMACK- to DMREQ delay		---		---
tD	DIOR-/DIOW- 16-bit	80		50	
tE	DIOR- data access		60		30
tF	DIOR- data hold	5		5	
tF	DIOR- data hold (1)		n/a		n/a
tG	DIOW- data setup	30		20	
tH	DIOW- data hold	15		5	
tI	DMACK to DIOR-/DIOW- setup	0		0	
tJ	DIOR-/DIOW- to DMACK hold	5		5	
tKr	DIOR- negated pulse width	50		25	
tKw	DIOW- negated pulse width	50		25	
tLr	DIOR- to DMREQ delay		40		30
tLw	DIOW- to DMREQ delay		40		30
tZ	DMACK- to tristate (2)		25		25

(0) Any device implementing this transfer mode must specify a Cycle time in the Identify Drive Data Structure (in word 65, Minimum Multiword DMA Transfer Cycle Time Per Word) which is greater than or equal to the cycle time in this table. Any device which implements this mode does NOT have to meet the cycle time in this table.
(1) Meaning of this parameter in the ATA standard was not clear. This specification states that this parameter is not applicable.
(2) New parameter specifies the time from the negation edge of DMACK- to the time that the data bus is no longer driven by the device (tristate). The tZ parameter applies only at the end of a Multiword DMA cycle, i.e., when DMACK is negated.

The device may actively drive the data bus or may tristate the data bus while DMACK- is asserted from the first time that DIOR- is asserted until DMACK- is negated as long as tE and tF requirements are met.

The host may actively drive the data bus or may tristate the data bus while DMACK- is asserted and the host intends to execute write operations, as long as tG and tH requirements are met.

FIGURE 1: Multiword DMA Timing Diagram



6.3 New PIO Transfer Mode

New PIO Transfer Modes are defined and identified as Mode 3 and Mode 4. The timing parameters associated with PIO Transfer Mode 3 and Mode 4 are defined in Table 2. Peripherals reporting support for PIO Transfer Mode 3 or Mode 4 must power up in a PIO Transfer Mode compatible with the existing ATA standard. Figure 2 shows the basic timing for PIO Transfers and is include to show the a new timing parameters t2i, t6Z and tR.

The minimum value of t0 is specified by the device in word 68 of the Identify Drive information. Refer to section 7.1.8 for a description of word 68.

Support of IORDY is mandatory when either PIO Mode 3 or Mode 4 is the current mode of operation.

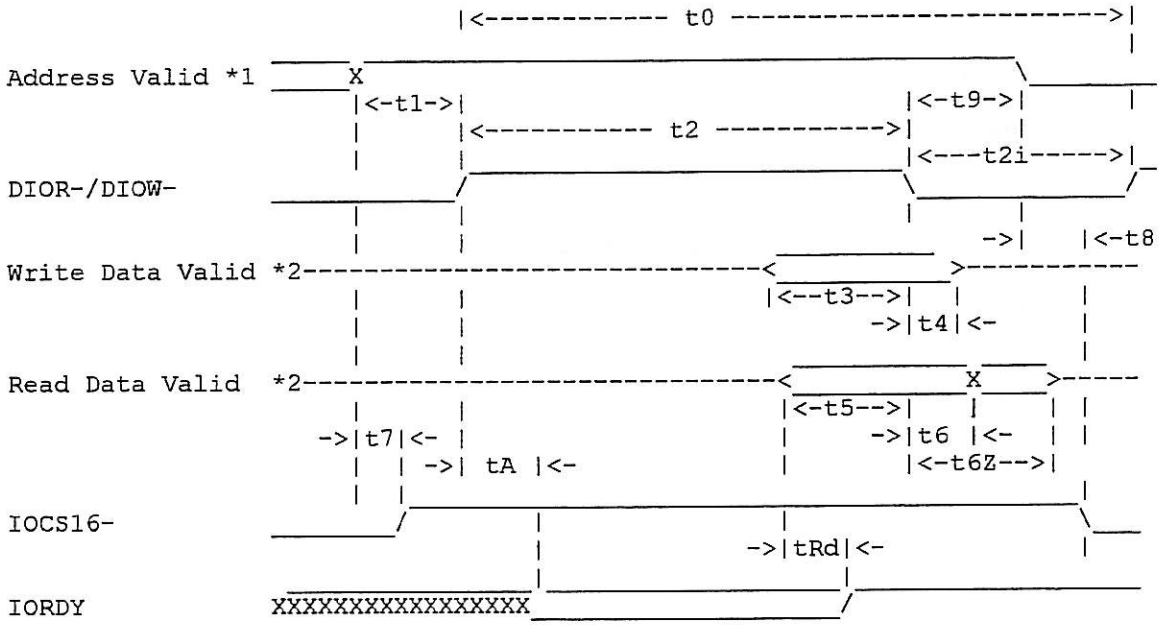
TABLE 2: New PIO Timing Parameters

	PIO timing parameters	Mode 3 nsec		Mode 4 nsec	
		Min	Max	Min	Max
t0	Cycle time (4) (0)	180		100	
t1	Address valid to DIOR-/DIOW- setup	30		20	
t2	DIOR-/DIOW- 16-bit (4)	80		50	
	Pulse width 8-bit (4)	80		50	
t2i	DIOR-/DIOW- recovery time (4)	70		25	
t3	DIOW- data setup	30		20	
t4	DIOW- data hold	10		5	
t5	DIOR- data setup	20		20	
t6	DIOR- data hold	5		5	
t6	DIOR- data hold (1)		n/a		n/a
t6Z	DIOR- data tristate (2)		30		30
t7	Addr valid to IOCS16- assertion (5)		30		30
t8	Addr invalid to IOCS16- negation (5)		30		25
t9	DIOR-/DIOW- to address valid hold	10		5	
tA	IORDY Setup time (3)	35		20	
tB	IORDY Pulse Width		1,250		1,250
tRd	Read Data Valid to IORDY asserted (if IORDY initially negated after tA)	0		0	

(0) Any device implementing this transfer mode must specify a Cycle time in the Identify Drive Data Structure (in word 68, Minimum PIO Transfer Cycle Time With Flow Control) which is greater than or equal to the cycle time in this table. Any device which implements this mode does NOT have to meet the cycle time in this table.
(1) Meaning of this parameter in the ATA standard was not clear. This specification states that this parameter is not applicable.
(2) New parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tristate).
(3) Delay from DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is negated then the host must wait until IORDY is asserted before the PIO cycle can be completed. If the device is not driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then t5 time must be met and tR time is not applicable. If the device is driving IORDY negated at the time tA after the activation of DIOR- or DIOW-, then tR time must be met and t5 time is not applicable.

(4) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. All three of the timing requirements (t0, t2 and t2i) must be met. The minimum total cycle time requirement, t0, is greater than the sum of t2 and t2i. This means that an host implementation can lengthen either or both of t2 or t2i to insure that t0 is met. A device implementation must support any legal host implementation.
(5) t7 and t8 apply only to 16-bit transfers.

FIGURE 2: PIO Timing Diagram



7. Command and Parameter Changes

In order to achieve the desired improvement in data transfer rates, changes are made to the parameters associated with two existing commands: the Identify Drive command and the Set Feature command.

7.1 Changes and Additions to Identify Drive Parameter Words

Changes are made to the parameter information returned to the host by the Identify Drive command. Four new parameter words have been defined within the parameter information, and two news bits are defined in an existing parameter word.

The following table outlines the changes and additions that are defined in the following sections.

TABLE 3: New Identify Drive Parameters

Word		Description
49		Capabilities
	12	Reserved (for pseudo DMA mode support)
	11	IORDY Supported
	10	IORDY can be disabled
53	15-2	Reserved
	1	1=the fields reported in words 64-70 are valid 0=the fields reported in words 64-70 are not valid
	0	(as defined in ATA Standard)
64	15-8	Reserved
	7-0	Advanced PIO Transfer Modes Supported
65		Minimum Multiword DMA Transfer Cycle Time Per Word
	15-0	Cycle time in nanoseconds
66		Manufacturer's Recommended Multiword DMA Transfer Cycle Time
	15-0	Cycle time in nanoseconds
67		Minimum PIO Transfer Cycle Time Without Flow Control
	15-0	Cycle Time in nanoseconds
68		Minimum PIO Transfer Cycle Time With IORDY Flow Control
	15-0	Cycle Time in nanoseconds
69		Reserved
70		Reserved

With the addition of Multiword DMA Transfer Mode 1, bits 9 and 1 of word 63 are defined to indicate Multiword DMA Transfer Mode 1 is active and Multiword DMA Transfer Mode 1 is supported, respectively.

7.1.1 IORDY Support

Bit 11 of word 49, the Capabilities word, is used to help determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This insures backward compatibility.

If a device supports PIO Mode 3, then this bit must be set.

7.1.2 IORDY Can Be Disabled

Bit 10 of word 49, the Capabilities word, is used to indicate a devices ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY.

7.1.3 Word 53, Bit 1: Field Validity

The existing word 53, bit 0 defines whether the fields contained in words 54 through 58 are guaranteed to be valid. Since this specification defines additional words within parameter information returned by the Identify Drive command, an additional bit, bit 1, is defined.

Bit 1 of word 53 will be set if the fields reported in words 64 through 70 are valid. This bit will be reset if the fields reported in words 64-70 are not valid.

Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, must set this bit and support the fields contained in words 64 through 70.

7.1.4 Flow Control PIO Transfer Modes Supported

Bits 7 through 0 of word 64 of the Identify Drive parameter information is defined as the Advanced PIO Data Transfer Supported Field. This field is bit significant. Any number of bits may be set in this field by the device to indicate which Advanced PIO Modes that it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future Advanced PIO Modes.
Bit 0, if set, indicates that the device supports PIO Mode 3.
Bit 1, if set, indicates that the device supports PIO Mode 4.

7.1.5 Minimum Multiword DMA Transfer Cycle Time Per Word

Word 65 of the parameter information of the Identify Drive command is defined as the Minimum Multiword DMA Transfer Cycle Time Per Word. This field defines, in nanoseconds, the minimum cycle time that the device can support when performing Multiword DMA transfers on a per word basis.

For devices which support Multiword DMA Mode 1, the value in word 65 shall not be less than 150.
For devices which support Multiword DMA Mode 2, the value in word 65 shall not be less than 100.

Any device which supports Multiword DMA Mode 1 or above must support this field.

If this field is supported, bit 1 of word 53 must be set.

If bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

7.1.6 Manufacturer's Recommended Multiword DMA Transfer Cycle Time

Word 66 of the parameter information of the Identify Drive command is defined as the Manufacturer's Recommended Multiword DMA Transfer Cycle Time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector Read DMA or Write DMA commands over all locations on the media under nominal conditions. A cycle time less that this value may cause DMARQ to be negated at a rate which may reduce throughput, without data corruption.

The value in word 66 shall not be less than the value in word 65.

Any device which supports Multiword DMA Mode 1 or above must support this field.

If this field is supported, bit 1 of word 53 must be set.

If bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

7.1.7 Minimum PIO Transfer Cycle Time Without Flow Control

Word 67 of the parameter information of the Identify Drive command is defined as the Minimum PIO Transfer Without Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

For devices which support PIO Mode 3, the value in word 67 shall not be less than 180.
For devices which support PIO Mode 4, the value in word 67 shall not be less than 100.

Any device which supports PIO Mode 3 or above must support this field.

Any device may support this field.

If this field is supported, Bit 1 of word 53 must be set.

If Bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

7.1.8 Minimum PIO Transfer Cycle Time With IORDY Flow Control

Word 68 of the parameter information of the Identify Drive command is defined as the Minimum PIO Transfer With IORDY Flow Control Cycle Time. This field defines, in nanoseconds, the minimum cycle time that the device can support while performing data transfers while utilizing IORDY flow control.

For devices which support PIO Mode 3, the value in word 68 shall not be less than 180.
For devices which support PIO Mode 4, the value in word 68 shall not be less than 100.

Any device which supports PIO Mode 3 or above must support this field.

Any device may support this field.

If this field is supported, Bit 1 of word 53 must be set.

If Bit 1 of word 53 is set and the device does not support this field, the device shall return a value of zero in this field.

7.1.9 Words 69 and 70

Words 69 and 70 are reserved for future definition.

(Editor's note: It is intended that this field be used for future specification of an alternative flow control mechanism.)

7.2. Changes to the Set Features Command

The Set Features command is utilized to select the active PIO and DMA Modes. In the ATA standard, the Set Features command with the Set Transfer Mode parameter utilizes the Sector Count Register to specify which transfer parameter to change and the value to be implemented. The use of the term "Block Transfer" is herein changed to PIO Default Transfer Mode and redefined. The Sector Count Register values are changed to:

PIO Default Transfer Mode	00000 00n
PIO Flow Control Transfer Mode x	00001 nnn
Single Word DMA Mode x	00010 nnn
Multiword DMA Mode x	00100 nnn
Reserved	01000 nnn

where "n" or "nnn" is a valid mode number for the associated transfer type.

(Editor's note: It is intended that the reserved values be used for future specification of an alternative flow control mechanism.)

If a device does not support the mode specified, the device posts an Aborted

Command error.

If a device supports this specification, and receives a Set Feature command with a Set Transfer Mode parameter and a Sector Count Register value of "00000 000", it shall set its default PIO transfer mode. If the value is "00000 001" and the device supports disabling of IORDY, then the device shall set its default PIO transfer mode and disable IORDY.

8. Electrical Considerations for 20 MByte/Sec Modes

The following paragraphs document proposed receiver, capacitance, cable and termination specifications for 20 MByte/Sec. transfer rates.

(Ed Note: Electrical simulations to indicate that these specifications are required, or that these specifications are sufficient for the 20 MByte/Sec. transfer rate have not been completed. This is not part of the specification at this time, but has been captured for documentation, discussion, and simulation support.)

8.1 Cable Specifications

Maximum Cable Length: 8 inches

3M Cable Type	Comments	Capacitance Max	Propagation Velocity
3365	unbalanced, today's typical	19.2 pF/ft	1.4 ns./ft
3517	balanced, without shield	19.1 pF/ft	1.5 ns./ft
3517	balanced, with shield	32.3 pF/ft	1.5 ns./ft

8.2 Load Capacitance Loads

The host capacitance (including IC, connector, termination, and PCB trace elements) shall not exceed 20 pF.

The drive capacitance (including IC, connector, termination, and PCB trace elements) shall not exceed 20 pF.

The produces a maximum capacitance per signal (for one host, two drives, and an eight inch cable) of 73 pF.

8.3 Receiver Input Specifications

The receivers input levels are defined as:

- Vih = 2.0V
- Vil = 0.8V

Input filtering is not required per this specification.

8.3 Termination

The following termination as shown in Figure 3 shall be placed on the drive for the following three signals driven from the host: DIOR-, DIOW-, and DACK-. Ra is 2.6 Kohm (+/- 5%). Rb is 4.0 Kohm (+/- 5%).

The termination as shown in Figure 3 shall be placed on the Bridge Logic for the following two signals driven from the drive: DMARQ and IORDY. Ra is 1.3 Kohm (+/- 5%). Rb is 2.0 Kohm (+/- 5%).

All signals, except PDIAG, DASP and CSEL, have an 51 ohm serial termination at the Bridge Logic. Note that any signals which are unbuffered to the system bus should have termination which may electrically affect the system bus.

FIGURE 3: Series Termination Schematic Diagram

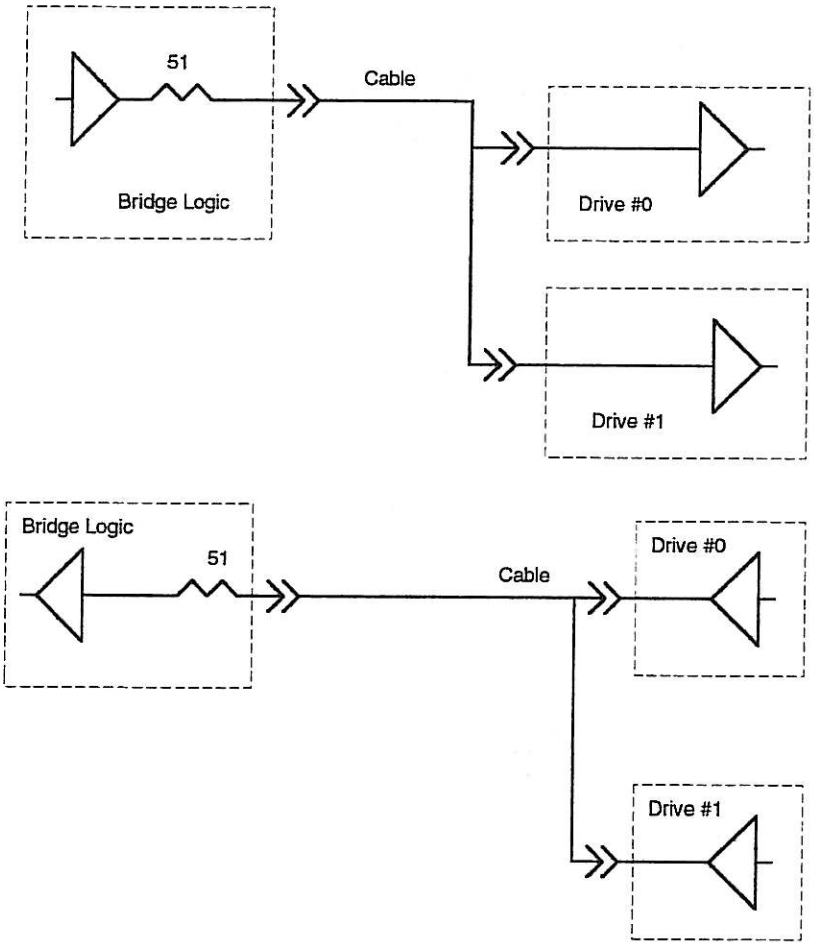


FIGURE 4: Host Driven Termination (DIOR-, DIOW-, and DACK-)

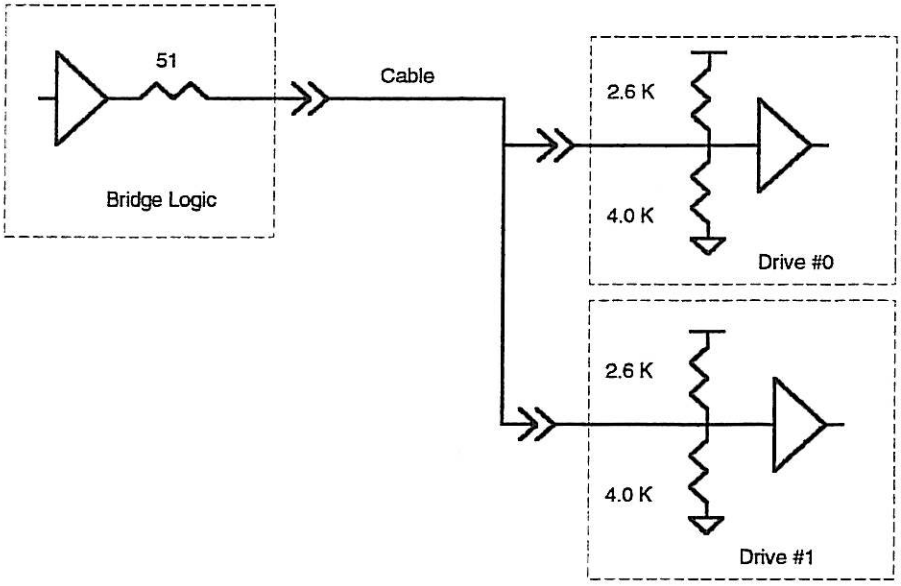
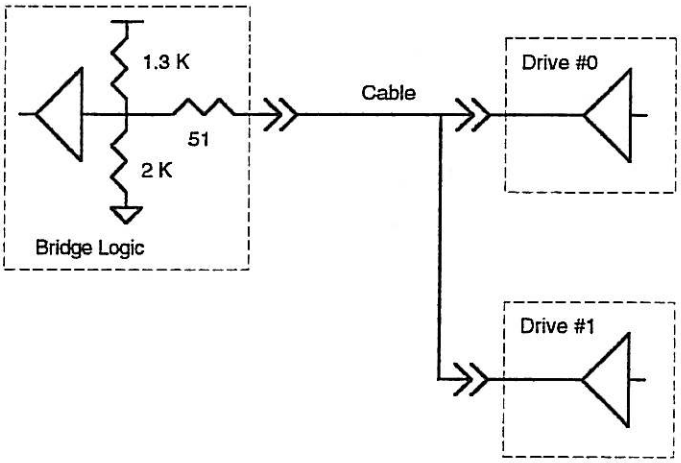


FIGURE 5: Drive Driven Termination (DMARQ and IORDY)



9.0 Enhanced PIO Data In Command Protocol

The Enhanced PIO Data In command protocol is an optional command protocol which provides additional error coverage for the data transferred from the drive to the host. This protocol adds an additional Status Register read after the final data transfer.

This final read of the Status Register provides the drive with the opportunity to indicate to the host that an error was detected within the drive during the previous data transfer. Some examples of a such errors are: a detected internal parity error during the transfer; a detected transfer data overflow; or a detected transfer data underflow. If an error is posted, the sector address in the task file should adjusted to point to involved sector.

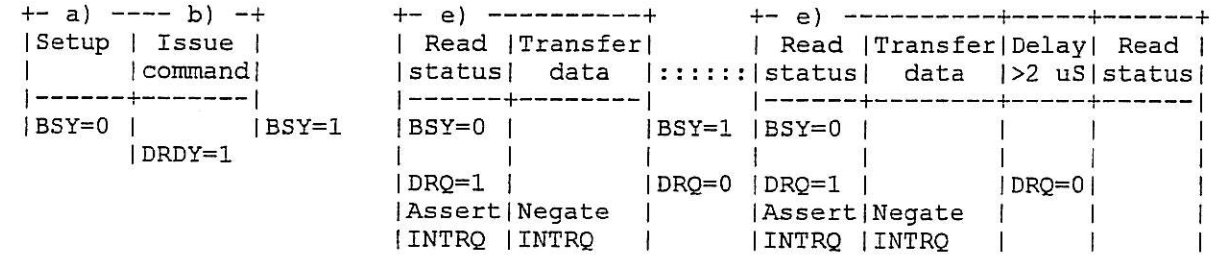
The PIO Data In command class includes the following commands:

- Identify drive
- Read buffer
- Read long
- Read sector(s)

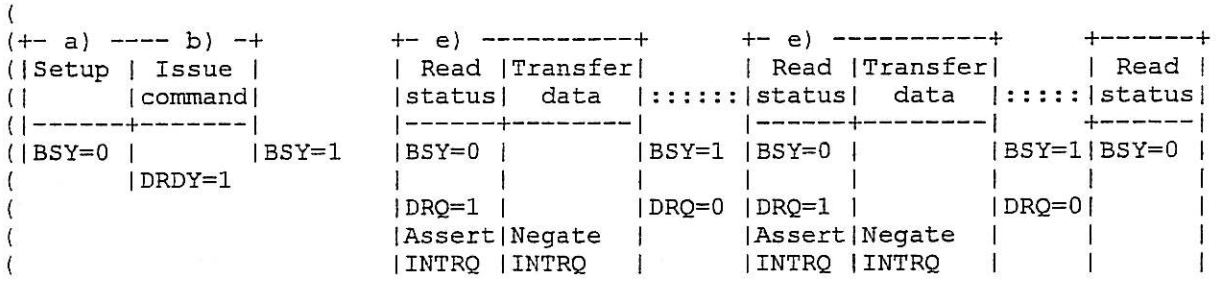
Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the drive to the host.

a) The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Drive/Head registers.
b) The host writes the command code to the Command Register.
c) The drive sets BSY and prepares for data transfer.
d) When a sector of data is available, the drive sets DRQ and clears BSY prior to asserting INTRQ.
e) After detecting INTRQ, the host reads the Status Register, then reads one sector of data via the Data Register. In response to the Status Register being read, the drive negates INTRQ.
f) The drive clears DRQ. If transfer of another sector is required, the drive also sets BSY and the above sequence is repeated from d). If transfer of another sector is not required, the drive will post valid status for the last sector/multiple transferred in the Status Register before clearing DRQ and within 2 microseconds of transferring the last word of data.
(Implementors note: Most hosts will not check DRQ in the Status Register after the transfer.

9.1 PIO read command example



(Oct. 27th alternative



If Error Status is presented in the status read before the data has been transferred, the drive will be prepared to transfer data, and it will be at the host's discretion that the data is transferred.

If Error Status is presented in the status read after the data has been transferred, any error recovery will be at the host's discretion.