TO: **John Lohmeyer, Chairman, X3T9.2 Committee (SCSI)**

From: **Dennis Pak (408)974-4874**
IEEE P1285 Liaison to X3T9.2/DADI
Apple Computer

Date: **July 23, 1993**

Subject: **P1285 Liaison Report for July 1993**

Scope

IEEE P1285 is a standards group organized to define a new interface for "high-latency", non-volatile memory elements such as rotating media and solid state memory. The group is targeting configurations where storage elements are small enough to be attached directly to the motherboard. The goals are to provide support for scheduling of data transfers spanning large numbers of units and to represent the traditional secondary storage elements as an extension to the system's main memory (memory-mapped).

Issues of concurrency, latency, bandwidth, extensibility, scalability are being addressed. The increasing demand for deterministic data transfers by real-time applications is being examined. Support is to be provided for scheduling data transfers in a predetermined manner in order to support time dependent applications.

The major features of P1285 are identified below:

- o Control and data space is memory mapped using P1212
- o One controller, multiple slaves model
- o Byte addressable, true memory mapped disk architecture
- o Inherent spindle synchronization support
- o Isochronous support
- o Live insertion/removal
- o Motherboard direct attach
- o Scalability in performance and cost

IEEE P1285 Project Status

The current activity involves defining the functional division between the memory unit (device) and the host/controller. New functions at the unit level and at the controller/host adapter level continue to be discussed and defined.

Several topics have been discussed recently.

The states of the interface finite state machine have been discussed in the context of IEEE 1212 and other CSR standards. The functioning of the interface while it is in these states has also been discussed.

In addition to the existing byte-oriented command format, a block-oriented format has been added for block-oriented devices. This new format allows reading/writing of one block of data.

The committee has also been looking at providing device dependent details through the interface. The current feeling is that the details provided should be very minimal, and that the interface should provide means for the system software to measure other parameters directly.

Discussions on a physical interface have started as a result of advice given at the May co-located meeting between P1285 and X3T9.2.

Upcoming Events

P1285 tentative meeting dates and locations:

August 8/5/93 @Bannon Engineering Building, Santa Clara University
September 9/2/93 @Apple Computer, 1 Infinite Loop, Cupertino, CA
October 10/7/93 @Bannon Engineering Building, Santa Clara University
November 11/4/93 @Apple Computer, 1 Infinite Loop, Cupertino, CA
December 12/2/93 @Bannon Engineering Building, Santa Clara University

These meetings are scheduled from 2:00-5:00 PM. There is a co-located meeting being planned for November. Please contact Martin Freeman at (415)354-0329 for exact date and location, or for additional information.