Date: April 30, 1993

X3T9.2/93-086r0
SFF/93s016r0

To: X3T9.2 and SFF Membership

From: Larry Lamers

Subject: Minutes of Joint ATA/SFF Working Group Meeting on Local Bus

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1. Opening Remarks

The meeting was convened 9:30 am on Wednesday, April 28, 1993 at the Crown Sterling Suites Hotel in Milpitas, CA. In all, 21 people from 12 companies attended.

The group extended its appreciation to Jim McGrath of Quantum for hosting the meeting.

This was a joint meeting of X3T9.2 ATA Working Group and Small Form Factor Specific Subject Working Group. The purpose of this meeting was to discuss extensions to AT Attachment interface that would allow for improved performance when operating with local bus adapters. It is not intended that these extensions operate in existing systems that do not support local bus adapters or have similar improved electronics.

2. Review of Agenda

Jim McGrath presented a proposed agenda. The agenda was accepted and amended as necessary. The content of these minutes reflects that agenda.

3. Attendance

The following persons were in attendance at the meeting.

Company	Contact	Phone	Fax
Adaptec	Richard Kalish	408 957-7169	408 957-7165*
	Al Pham	408 957-4804	408 262-2533*
	Yen Lin	408 945-8600	408 262-2533*
	Dave Wood	408 945-6753	408 957-7102*
Appian	Kenneth Curt	408 730-5406	408 730-5473
Cirrus Logic	John Geldman	510 226-2368	510 226-2150
	Nicos Syrimis	510 226-2153	510 226-2170
Conner	Steve Anderson	303 682-8320	303 772-0182*
Dallas Semi.	Louis Grantham	214 450-8110	214 450-3715*
	Michael Smith	214 450-0457	214 450-3715*
Digital	Bill Ham	508 841-2629	508 841-6100
Maxtor	Ron Roberts	408 432-3875	408 432-3773
	Larry Lamers	408 432-3889	408 432-3833
NationalSemi	Robbie Shergill	408 721-7959	408 721-7956
Quantum	Jim McGrath	408 894-4504	408 894-3208
	John Brooks	408 984-5871	408 894-3255
Seagate	Hale Landis	408 439-2443	408 438-4190
	Marvin Lum	408 439-2706	408 438-4846
Silicon Sys.	Steve Finch	714 573-6808	714 573-6914*
	Mike Scott	714 573-6613	714 573-6916*
WD	Tom Hanan	714 932-7472	714 932-7314

NOTE: Those persons noted with an asterisk following their facsimile numbers have requested a facsimile of the meeting minutes. Tom Hanan has agreed to do this.

4. Review of the Minutes of Previous Meeting

Tom Hanan reviewed the minutes of the previous minutes and the action items. It was noted that Tom had failed to distribute his proposal via the SFF reflector as promised. Also the folks that were supposed to get the minutes sent via facsimile did not receive them.

Quantum, Conner, and Silicon Systems requested they be added to the fax list.

A request was made to increase the right margin so as to get the document display in 80 columns.

The spelling of Seagate was incorrect.

With the noted additions and corrections the minutes were approved. A revised set of minutes will not be distributed.

5. Identification and Usage of High Performance modes and PIO Flow Control Mechanisms [Geldman] (93s008r2)

John Geldman presented a proposal that defines terms to use for discussion: (guaranteed sustainable cycle time, average sustainable cycle time, maximum sustainable cycle time, maximum burst cycle time).

He stated that a host that knows the transfer rates based on these cycle times and should be able to configure its drivers. Flow control is needed on the CPU-Bridge and Bridge-Drive interfaces to maximize transfer rates.

Predictive use of IOCHRDY is possible as a flow control mechanism. There is a 1.25 usecond specification on IOCHRDY that exists in the ISA bus definition.

John proposed decoupling the discussion on flow control and transfer modes. Systems can be built that do not use flow control mechanisms.

John proposed a SET FEATURE value to turn on flow control. The group felt that it needs a turn off for flow control as well as turn on.

The consensus was that the working group recommend flow control be required on the CPU-Bridge (see 93s014r0).

6. Higher Performance ATA Timing [Geldman] (SFF/93s-005r2)

John presented a table of modes and timing values. John proposed getting the IOCS16 signal out of Modes above 2 because everyone knows what to do with it. He suggested the use of a three state transceiver and disable it. There is a problem with signals adjacent to IOCS16 on cable due to ground bounce. The host adapter should bias IOCS16 to "asserted" with pseudo driver. Several corrections were made to his proposed multi-word DMA timings.

7. High Performance Shopping List & PIO Timing [Anderson] (SFF/93s-012r0)

Steve Anderson presented a proposal for PIO similar to Cirrus Logic proposal but with a more concise condensed table of mode information returned to host. T7 and T8 timings are tighter to allow a third vendor to qualify parts.

Consensus on two modes, programmable data transfer rate, min values specified in timing table.

8. Improved ATA Timing [Pham] (SFF/93s-013r0)

Al Phan proposed a 90 ns cycle time; mandatory sampling of IOCHRDY by adapter; and that a device may use IOCHRDY if it can not meet the cycle timing.

He also proposed changing the reference point of IOCHRDY if in local bus operation. Steve Finch pointed out a problem with this that breaks existing drives. Tightening up the timing to 20 ns seems problematical given the current install base. The reference is from address valid.

The question of how to handle two drives, one old and one new arose. Tom Hanan suggested that any master/slave detection should cause the adapter to not use the new IOCHRDY timing. Can the adapter figure out that the local bus drive exists?. This was not felt to be acceptable.

A mechanism to indicate to the drive that a local bus adapter is present using IOCHRDY, HCS1FX and HCS3FX asserted was proposed. This would require changing the adapter and the drive silicon.

If a drive is capable of generating IOCHRDY within 20 ns then no further mechanism is needed. If not then the adapter could indicate that it is local bus capable by asserting IOCHRDY, HCS1FX#, and HCS3FX# during reset. Based on detecting a local bus capable adapter the drive could generate IOCHRDY off address valid instead of IOR/IOW. In a master/slave situation the CPU would have to program the local bus adapter to the slowest cycle time indicated by the devices. If one of the devices did not support local bus adapters then the bus cycle time would be extended based on the cycle times.

9. Signal Quality Enhancement [Wallace] (SFF/93s004r1)

Dean Wallace was not present.

10. High Performance PIO Recommendations [Hanan] (SFF/93s015r0)

Tom Hanan presented yet another proposal for addressing the needs of the VESA folks.

A min cycle time word needs to be defined for each mode, sustained, burst, and DMA.

Tom agreed to include an annex to explain the relationship between the modes and cycle times. He will remove section 8 on overlapped commands. A number of other corrections were pointed out that need to be fixed. Tom is still some distance away from getting acceptance.

11. IOCHRDY Release

Steve Finch raised an issue on the delay of IOCHRDY released and data being valid for a read. It was suggested that this time be equal to t5. Steve will develop a written proposal.

12. Resolution of Flow Control

Jim McGrath stated that it is implicit that IOCHRDY is the flow control method for mode 3. He prefers the DREQ/DACK flow control because of the compatibility issues with IOCHRDY. Using two different flow control methods, one for mode 3 and another for mode 4, will cause customer confusion.

Does IOCHRDY need an enabling mechanism? Jim thinks so, since some systems behave badly when this signal is driven. Set Features could be used to enable; this requires a BIOS change.

A bit will be added to IDENTIFY DRIVE to reflect the state of IOCHRDY being used.

13. Resolution of PIO Timing

Jim McGrath put up the foil with the PIO timing values. It was agreed that there will be two modes. If the faster mode is supported the slower mode is assumed to be supported also.

Tom expressed concern that the existing cable (18-inches, not terminated) will not support cycle times of less than 180. 166 is possible - 150 is definitely not. Mode 3 is agreed to be a 180 ns cycle time.

Measured at the connector of the drive for Mode 3 (IOCHRDY flow control):
t1 = 30 ns min
t2 = 80 ns min
t2i = 70 ns min (tK)
t3 = 30 ns min
t4 = 10 ms min
t5 = 20 ns min
t6 = 5 ns min/30 ns max
t7 = 30 ns max
t8 = 25 ns max
t9 = 10 ns min
tA = 30 ns max
tB = 1250 ns max

For Mode 4 (requires REQ/ACK flow control):
t1 = 20 ns min
t2 = 50 ns min
t2i = 25 ns min (tK)
t3 = 20 ns min
t4 = 5 ms min
t5 = 20 ns min
t5i = t2-t5 30 ns max
t6 = 5 ns min/15 ns max
t7 = 30 ns max (decoupled)
t8 = 25 ns max (decoupled)
t9 = 5 ns min
tA = 20 ns max (decoupled)
tB = 1250 ns max

There was considerable debate over 90 vs 120 ns cycle time. There are significant signal quality issues with either. It is likely that more expensive cables will be required.

There was a debate over the t5i; should it be specified? Many felt the answer is yes because it is what is really measured and designed too. Unfortunately it is not specified in ATA.

Steve Finch requested that a discussion of rise time be added to the next agenda.

14. Time And Place of Next Meeting

It was agreed that the next joint meeting of this working group would be held at the Crown Sterling Suites, Milpitas, CA on June 30, 1992 starting at 9:30 am. The Crown Sterling Suites is located just West of I-680 on Highway 237 (Calveras Blvd). Call Jim McGrath at 408-894-4504 if you have any questions.

Please note that during the Sante Fe, NM week of meetings that the regularly scheduled SFF and ATA meetings will occur.

The proposed meeting schedule is as follows:

Event	Date	Time	Location/Contact
ATA Working Group	28-APR-93	09:00-16:00	Milpitas, CA
Disk Drive Working Group	17-MAY-93	14:00-17:00	Sante Fe, NM
ATA Working Group	26-MAY-93	09:00-16:00	Milpitas, CA
ATA Working Group	30-JUN-93	09:00-16:00	Milpitas, CA
Disk Drive Working Group	19-JUL-93	13:30-20:00	Bedford, NH
ATA Working Group	28-JUL-93	09:00-16:00	Milpitas, CA

15. Documents

Documents from this meeting are listed below.

Document Number	Description	Pages	Page
SFF/93s005R2	Higher Performance ATA PIO Modes Timing	2	
SFF/93s008R2	Flow Control Mechanisms	5	
SFF/93s012R0	High Performance Shopping List and PIO Timing Recommendations	5	
SFF/93s013R0	Improved ATA Timing to Support Local Bus	8	
SFF/93s014R0	ATA Local Bus Connection Model	3	
SFF/93s015R0	Local Bus Timing Proposal	6	
SFF/93s016R0	Minutes of SFF Local Bus Mtg 4/28/93		

16. Adjournment

The meeting adjourned at 4:30 p.m.