

# A NEW PERIPHERAL INTERFACE ??????

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RKR 03/93

**MAXTOR CORPORATION**  
SYSTEM ENGINEERING

215

X3T9.2/93-049 R1

# PERIPHERAL DEVICE INTERFACE

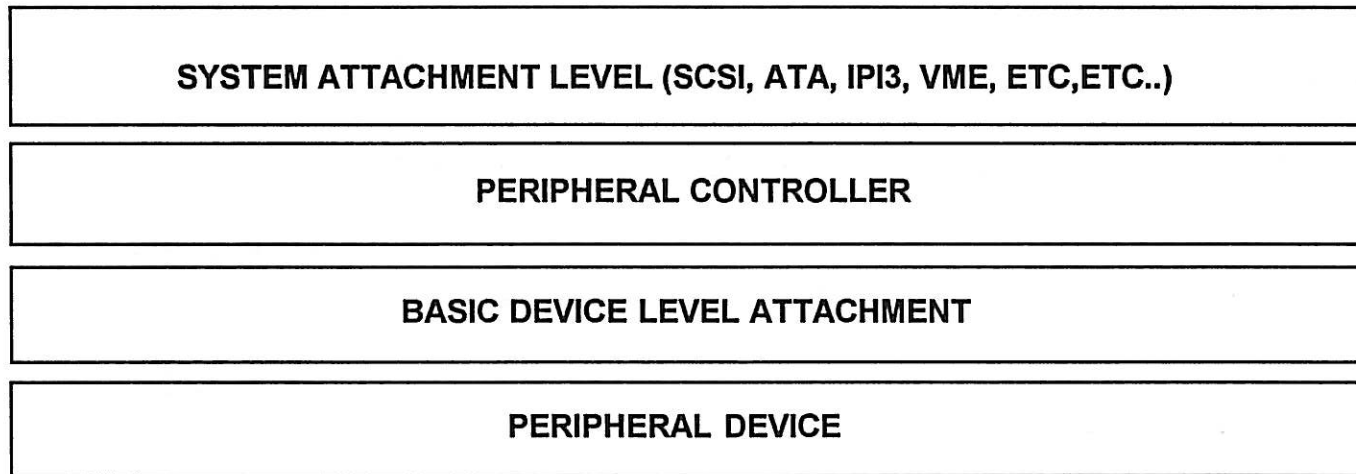
## ANOTHER INTERFACE !!!

### DESIGN GOALS

- LOW LEVEL ACCESS TO THE MEDIA... IF REQUIRED
- VARIABLE DATA TRANSFER RATES FOR PERFORMANCE VS COST TRADE-OFFS
- ALLOW VENDORS TO TAKE ADVANTAGE OF VOLUME PRODUCTION
- PROVIDE EASY IMPLEMENTATION OF ARRAYS OF DISKS
- PROVIDE SIMPLIFIED COMMAND STRUCTURES AND FLOW
- PROVIDE FOR MAXIMUM THROUGH-PUT
- PROVIDE FOR ERROR FREE TRANSFERS

# PERIPHERAL DEVICE INTERFACE

## ARCHITECTURAL MODEL



# PERIPHERAL DEVICE INTERFACE

## ARCHITECTURAL MODEL

### ATTRIBUTES OF LEVELS

PERIPHERAL CONTROLLER	PERIPHERAL DEVICE
SYSTEM INTERFACE CONTROLS	ALL SERVO CONTROLS
CACHE MEMORIES(IF REQUIRED)	ENCODER DECODER
CONTROLS MULTIPLE DEVICES(NO LIMITS)	READ/WRITE CIRCUITS
BUFFER AREAS	ECC ON THE FLY
SYSTEM SPECIFIC KNOWLEDGE	STORAGE MEDIA
	SPINDLE SYNC CKTS
	POWER CONTROLS

# PERIPHERAL DEVICE INTERFACE

## INFORMATION MOVEMENT PROTOCOL

### PERIPHERAL CONTROLLER

### PERIPHERAL DEVICE

4 COMMAND WORDS  
TRANSMITTED



4 COMMAND WORDS RCVD'D  
& DECODED

4 STATUS WORDS RCV'D



4 STATUS WORDS TRANSMITTED

WAIT FOR INTERRUPT  
(DO SOMETHING ELSE)

PERFORM SPECIFIED COMMAND

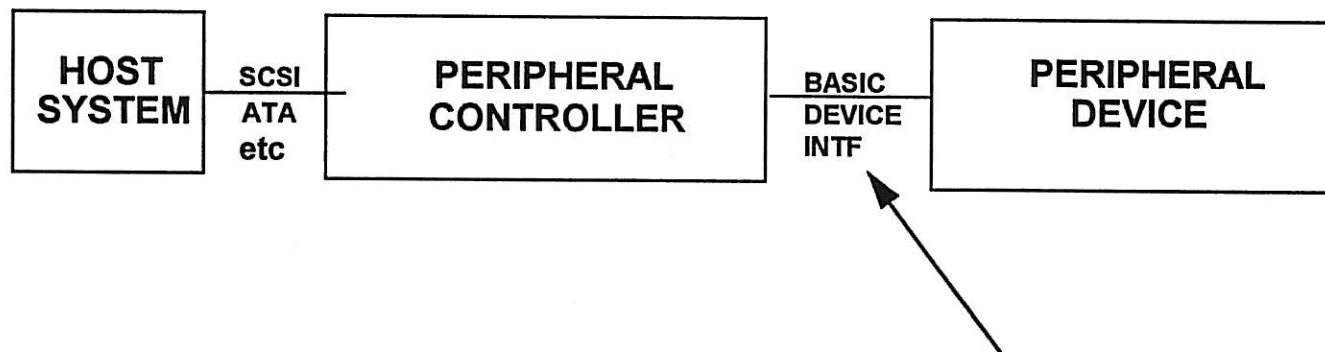
4 STATUS WORDS RCV'D



TASK COMPLETED TRANSMIT  
4 STATUS WORDS

# PERIPHERAL DEVICE INTERFACE

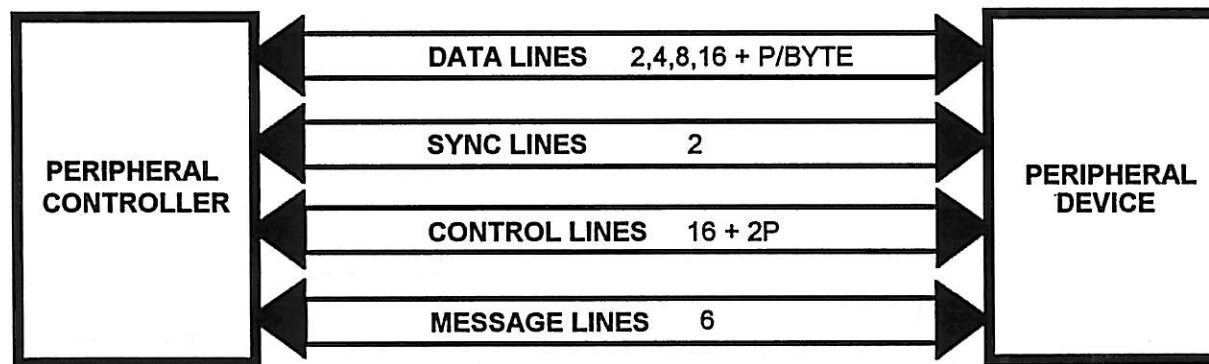
WHERE DOES IT FIT  
IN THE HIERARCHY OF THE SUBSYSTEM ??



TYPICAL PERIPHERAL SUB-SYSTEM

# PERIPHERAL DEVICE INTERFACE

## INTERFACE LINES



# PERIPHERAL DEVICE INTERFACE

## CONTROL SIGNALS

CONTROL SIGNALS ARE BI-DIRECTIONAL

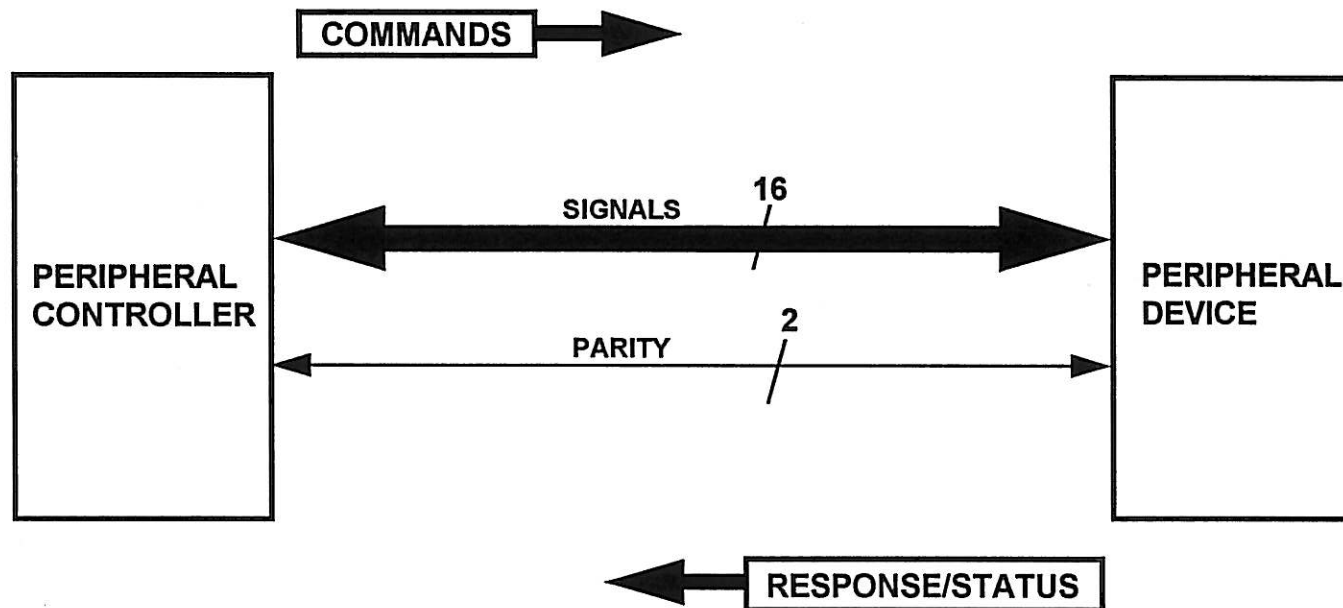
TRANSPORTS COMMAND DATA TO THE PERIPHERAL DEVICE

TRANSPORTS RESPONSE/SENSE DATA TO THE PERIPHERAL CONTROLLER



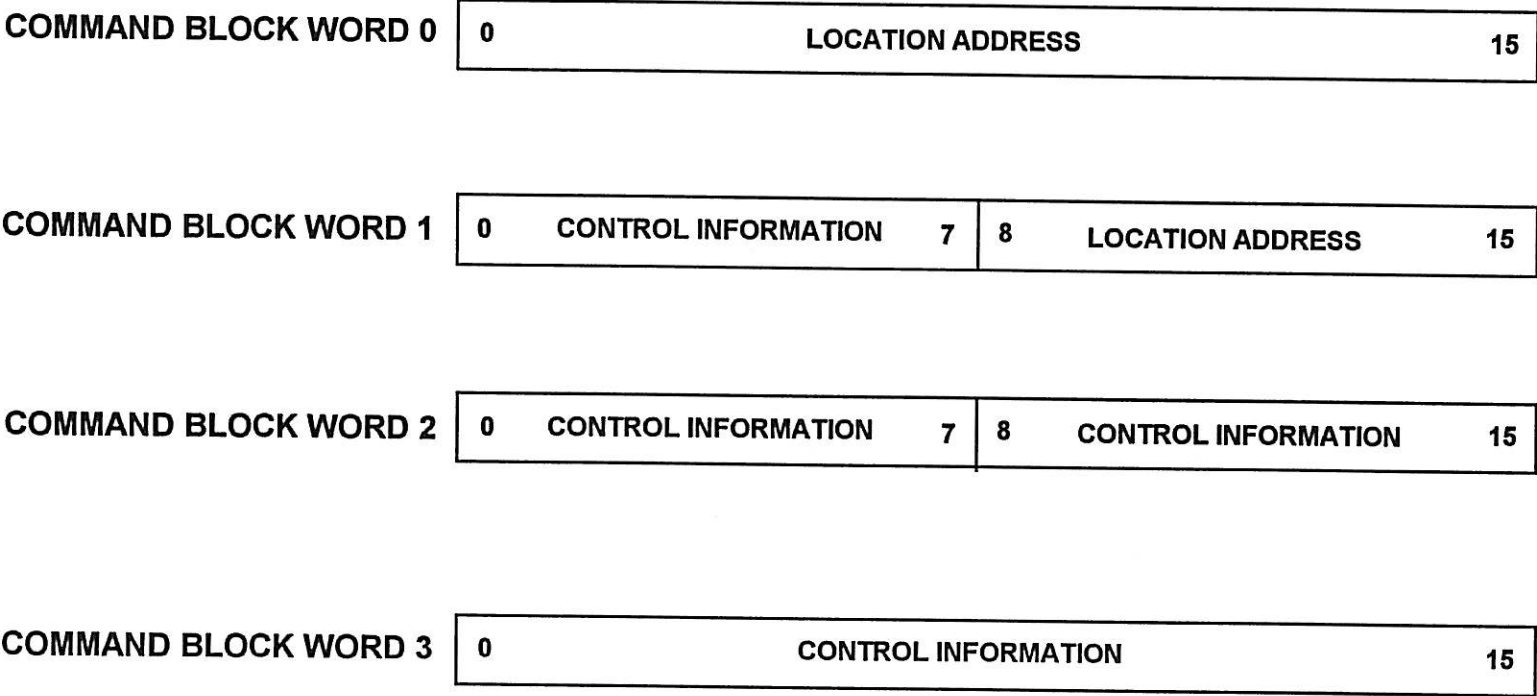
# PERIPHERAL DEVICE INTERFACE

## CONTROL SIGNAL FLOW



PERIPHERAL DEVICE INTERFACE

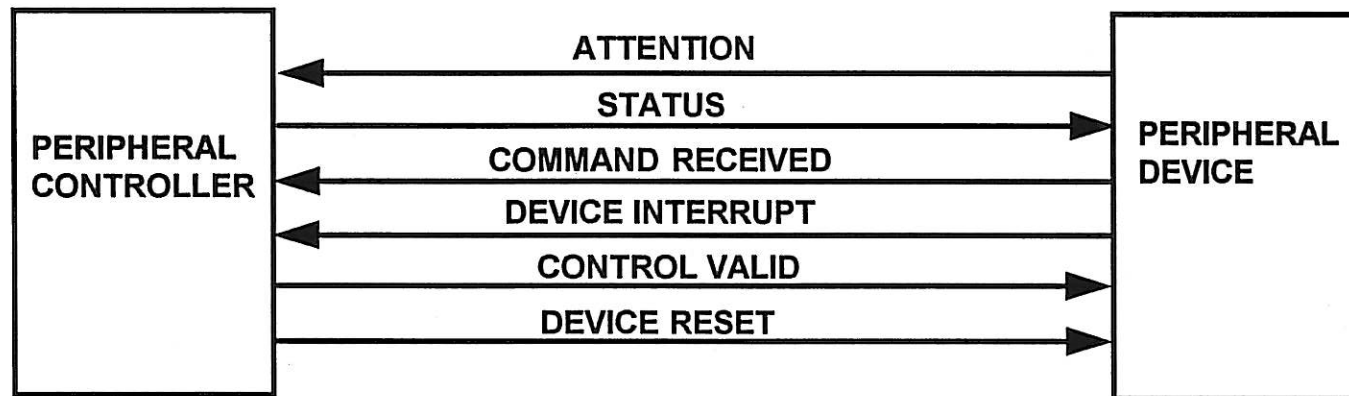
COMMAND BLOCK FORMAT



# PERIPHERAL DEVICE INTERFACE

## MESSAGE SIGNALS

MESSAGE SIGNALS COMMUNICATE EXACT MESSAGES BETWEEN THE PERIPHERAL CONTROLLER AND THE PERIPHERAL DEVICE



# PERIPHERAL DEVICE INTERFACE

## MESSAGE SIGNAL DEFINITIONS

ATTENTION	Asserted by peripheral device to request service.
STATUS	When asserted by controller request status from the device, when negated it indicates transfer of control information.
COMMAND RECEIVED	Asserted by device to indicate receipt of last word of control information. Remains asserted until completion of that command indicating device is in a busy state.
DEVICE INTERRUPT	Asserted by the device to execution of a command or completion of any request.
DEVICE RESET	Asserted by the controller to initialize the device.
CONTROL VALID	Asserted by the controller to indicate information is valid on the control lines.

# PERIPHERAL DEVICE INTERFACE

## DATA SIGNALS

DATA SIGNALS ARE BI-DIRECTIONAL

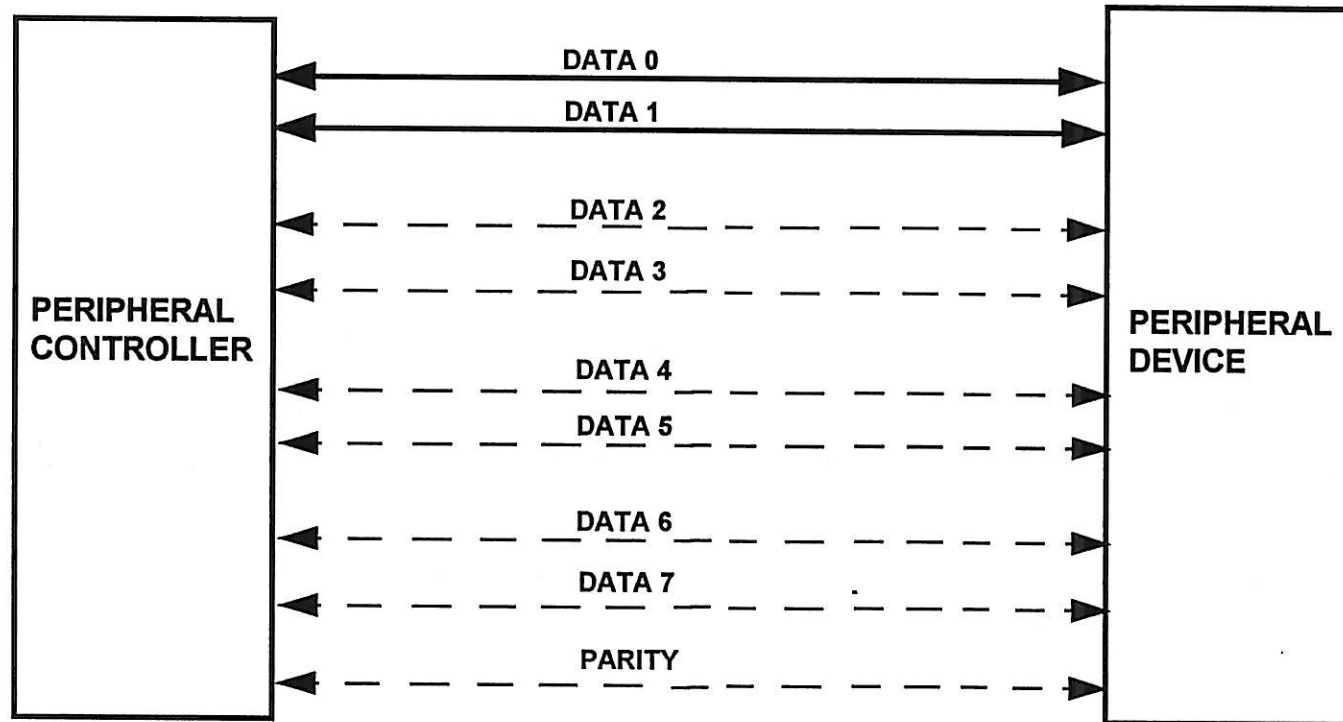
DATA SIGNALS MAY CONSIST OF 2, 4, OR 8 PHYSICAL LINES

IF 4 OR 8 PHYSICAL LINES ARE USED A PARITY BIT MUST ALSO BE USED

NUMBER OF DATA SIGNALS DETERMINED BY SYSTEM  
PERFORMANCE REQUIREMENTS

# PERIPHERAL DEVICE INTERFACE

## DATA SIGNALS



BI-DIRECTIONAL SIGNALS

PARITY IS OPTIONAL FOR 2 BIT TRANSFER  
MANDATORY ON 4 & 8 BIT TRANSFERS

# PERIPHERAL DEVICE INTERFACE

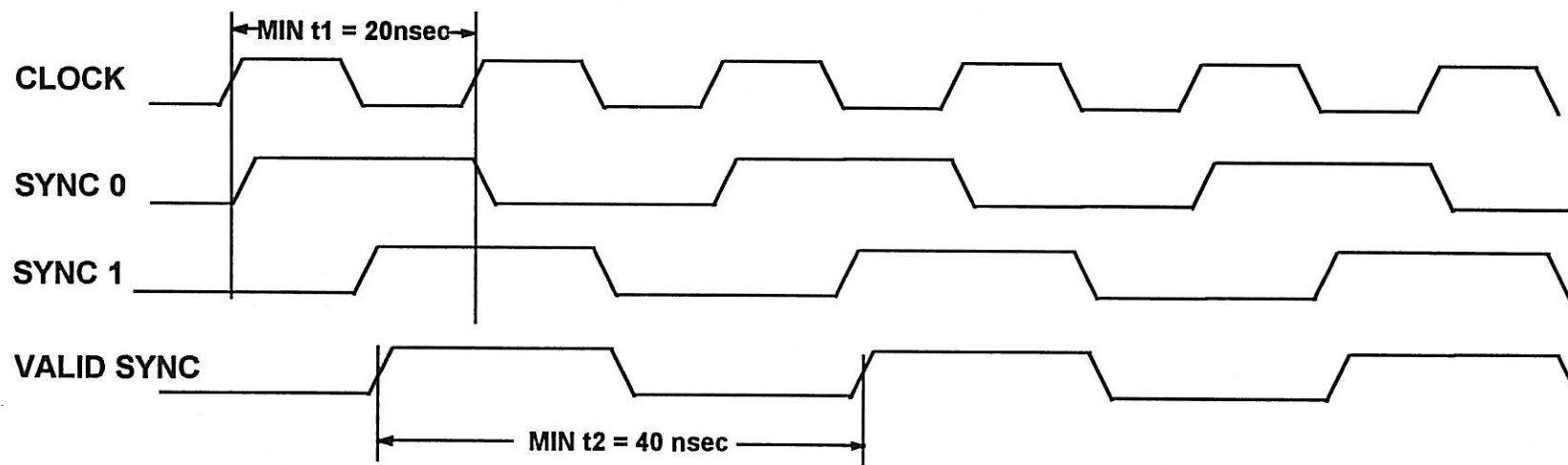
## SYNC SIGNALS

SYNC SIGNALS ARE BI-DIRECTIONAL

SYNC SIGNALS ARE USED IN CONJUNCTION WITH TRANSFER OF  
DATA, COMMAND, AND STATUS BETWEEN THE PERIPHERAL  
CONTROLLER AND THE PERIPHERAL DEVICE

## PERIPHERAL DEVICE INTERFACE

### SYNCRONIZATION



#### VALID SYNC SEQUENCE

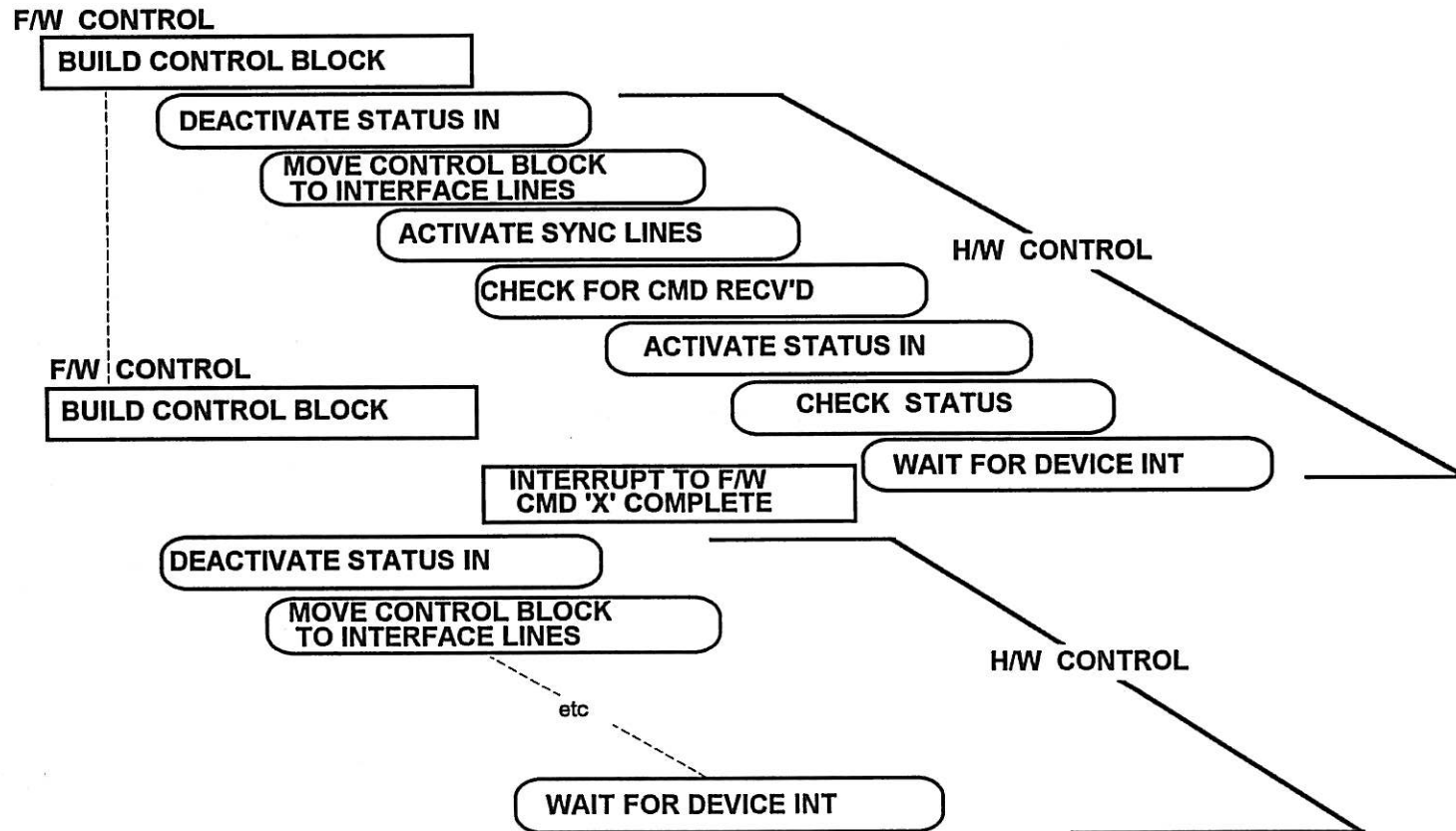
WHILE SYNC 0 IS ASSERTED, AND WHEN SYNC 1 IS ASSERTED, THE DURATION OF SYNC 1 BECOMES VALID SYNC TIME.

SYNC SIGNALS ARE SYNCRONIZED WITH THE CLOCK OF THE SENDING END OF THE INTERFACE.

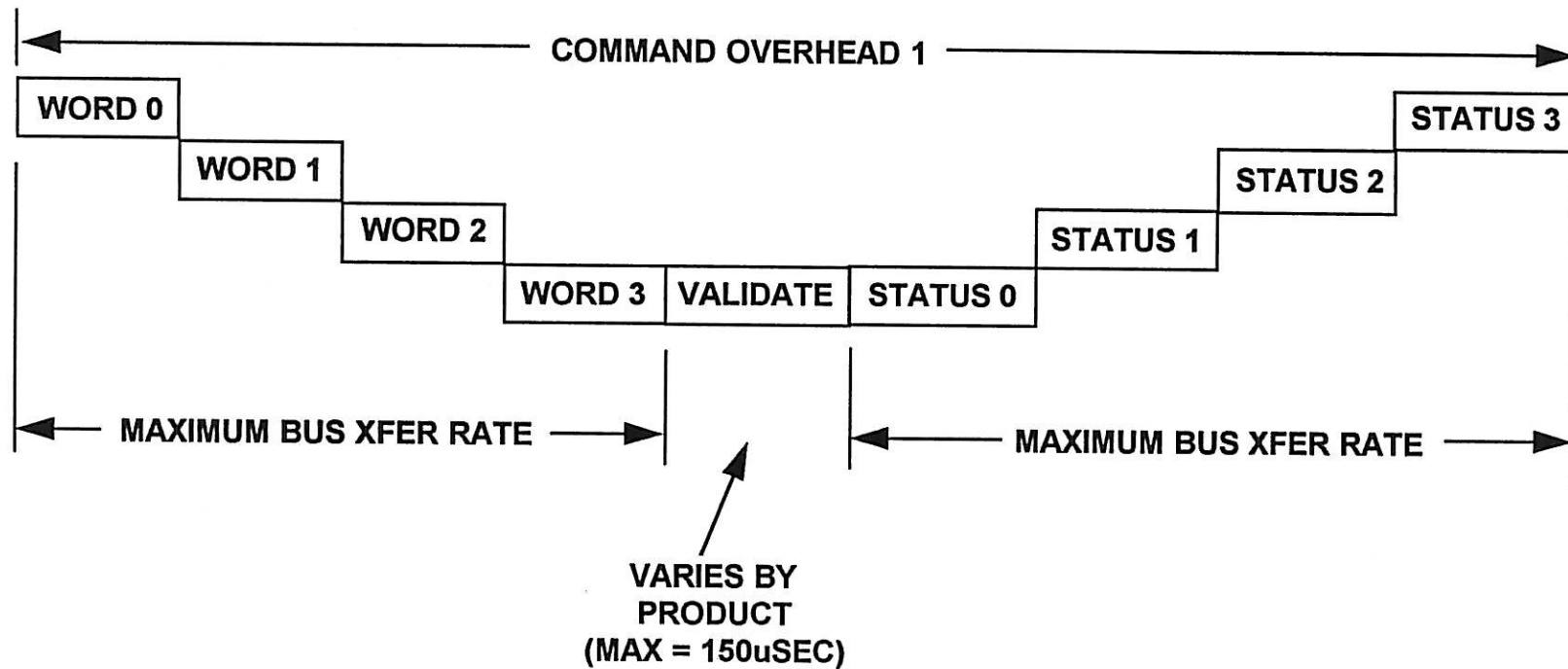


# PERIPHERAL DEVICE INTERFACE

## COMMAND BLOCK FLOW



# PERIPHERAL DEVICE INTERFACE TIMING CONSIDERATIONS



PREDICTABLE AND CONSISTENT LATENCY

# PERIPHERAL DEVICE INTERFACE

## TIMING SPECIFICATIONS

MAXIMUM CLOCK FREQUENCY

50 MHz

MAXIMUM TRANSFER RATES: (NON-BUFFERED)

2 BIT

12.5 MBytes/SEC

4 BIT

25.0 MBytes/SEC

8 BIT

50.0 MBytes/SEC

MAXIMUM COMMAND TRANSFER TIME

320 nsec

MAXIMUM COMMAND VALIDATION TIME

150 usec

MAXIMUM STATUS TRANSFER TIME

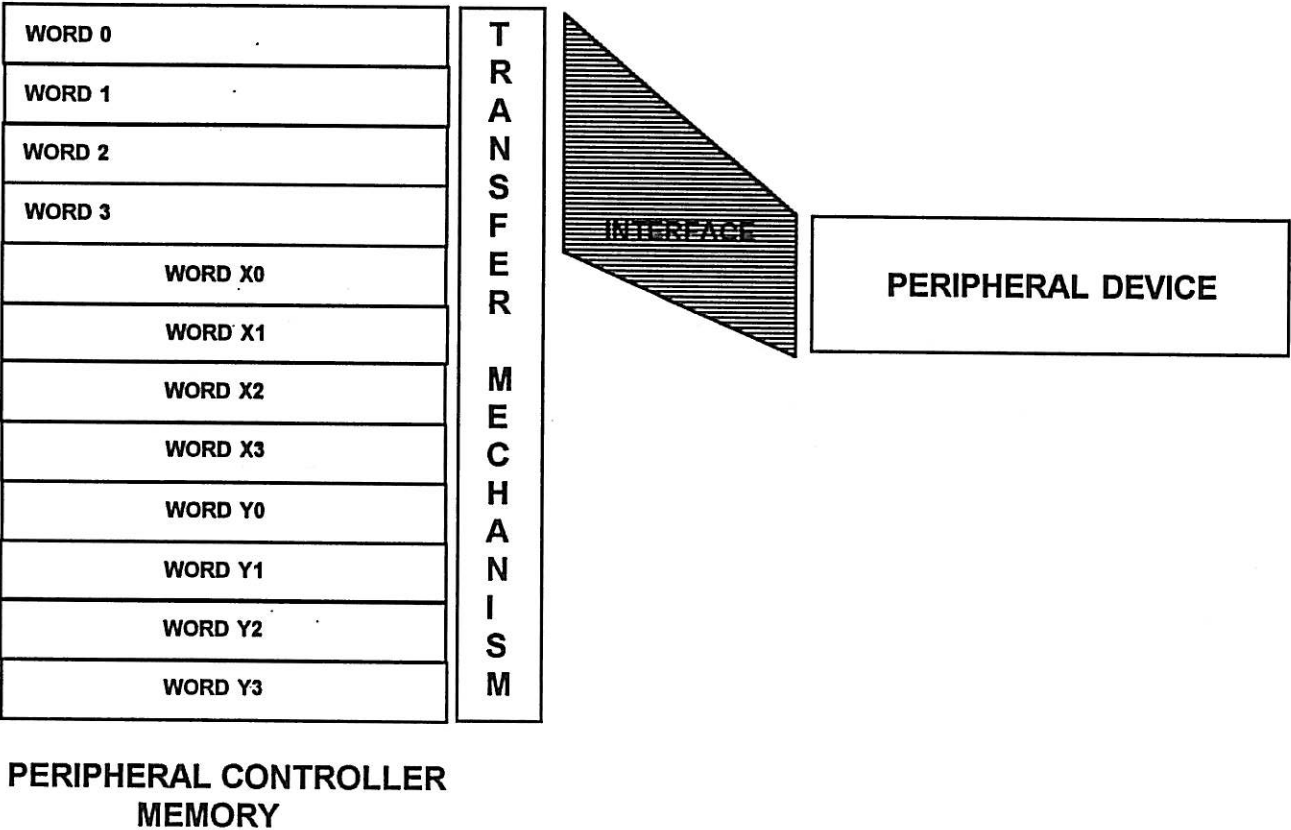
320 nsec

NOTE:

TIMING BASED ON A MAXIMUM MEDIA  
TRANSFER RATE OF 100MHz

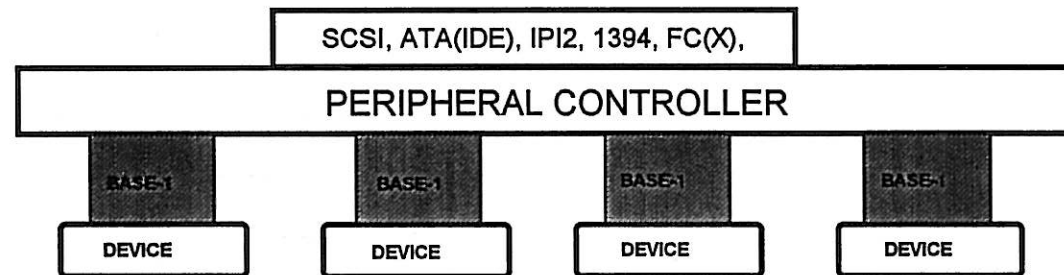
PERIPHERAL DEVICE INTERFACE

COMMAND RETRIEVAL



# PERIPHERAL DEVICE INTERFACE

## CONFIGURATION POSSIBILITIES



RADIAL CONNECTION

## **PERIPHERAL DEVICE INTERFACE**

### **ADVANTAGES OF INTERCONNECTION SCHEME**

- **PROVIDES LOW LEVEL ACCESS TO MEDIA (if required)**
- **SIMPLIFIES PERIPHERAL DEVICE FIRMWARE**
- **LESS COSTLY PERIPHERAL DEVICES**
- **EASE OF IMPLEMENTATION FOR ARRAYS OF DISKS (RAID's ??)**
- **PERIPHERAL GUIDED VS SYSTEM AFTER THOUGHT**
- **PERFORMANCE ORIENTED WITH LESS \$ THAN SCSI (PER SYSTEM)**