X3T9.2/93-8

Local Bus IDE Modes

Revision: 1.1
Date: 10/21/92

The ATA specification Rev 3.0 provides for three modes of timing for PIO in word 51 of the identify drive information. Bits 15-8 of word 51 defines three PIO timing modes which are contained in figure 11-1 and is reproduced here.

	PIO Timing Parameters		Mode 0 nsec	Mode 1 nsec	Mode 2 nsec
t0	Cycle Time	(Min)	600	383	240
t1	Address Valid to DIOR-/DIOW- Setup	(Min)	70	50	30
t2	DIOR-/DIOW- 16 bit	(Min)	165	125	100
	Pulse Width 8 bit	(Min)	290	290	290
t3	DIOW- Data Setup	(Min)	60	45	30
t4	DIOW- Data Hold	(Min)	30	20	15
t5	DIOR- Data Setup	(Min)	50	35	20
t6	DIOR- Data Hold	(Min)	5	5	5
t7	Addr Valid to IOCS16- Assertion	(Max)	90	50	40
t8	Addr Valid to IOCS16- Negation	(Max)	60	45	30
t9	DIOR-/DIOW- to Address Valid Hold	(Min)	20	15	10

Figure 11-1: PIO DATA TRANSFER TO/FROM DRIVE

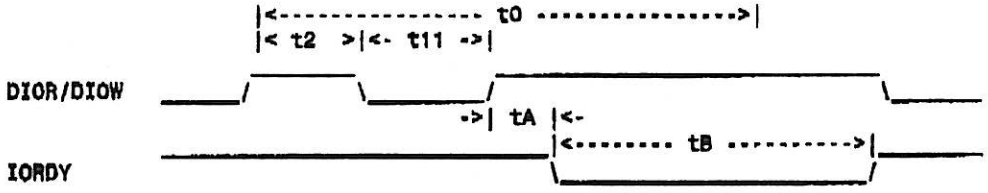
Local Bus allows a much more granular cycle timing then allowed for in these modes. We would like to use bits 7-0 of word 51 to further quantify the timing modes to allow the system timing to be tuned to what the drive can handle. This document will propose additional Sub-modes to allow for improved timing while maintaining compatibility with the modes already defined. A mode will also be defined for future use that will allow the drive to self pace the interface using IORDY.

Additional requirements for Local Bus support is the drive must not require the use IORDY as long as the system meets the timing mode as specified. Also all PIO accesses to the data port must be assumed to be 16 bits for sector data and 8 bits for ECC in a Read/Write Long command. This must be done since IOCS16- may be ignored. Also t2 should be the same for 8 bit and 16 bit data access for Local Bus support. If bits 7-0 of Word 51 is some value other than 00 or FFH it will be assumed that the drive supports Local Bus IDE and adheres to these restrictions. If bits 7-0 of Word 51 is 00 or FFH then it will be assumed there is no sub-Mode and the drive doesn't support Local Bus IDE. Timing t10 is a new timing specification for the read access time and defines the delay from IOR- active to data D15:0 valid.

Note: Cy 4:0 = 00000b is not allowed for PIO Sub-Mode 0 and Cy 4:0 = 11111b is not allowed for PIO Sub-Mode 7.

In addition to these modes, bit 15 of Word 51 will be defined as the Self Pacing bit. If this bit is a zero then the system must meet the timings and cycle time as defined by Word 51 bit 7:0 and IORDY can be ignored. If this bit is a one than the drive can support Self Pacing if the system honors IORDY. This allows the system to ignore the cycle time defined in Word 51 bit 4:0 as long as the minimum command inactive time t11 is meet. All other timing as defined by the Sub-Modes M2:1 of Word 51 bit 7:5 must be meet. The drive will issue IORDY following timing tA and tB of the ATA spec as shown in figure 11-2. If the drive can't currently handle the command it will ignore the command until it can accept it. This will allow the drive to vary the cycle time based on what it is currently doing, what track it is on, etc., maximizing the transfer rate from the drive and the system. This timing is shown in figure 11-2.1 below. The system will continue to drive DIOR- or DIOW- active while IORDY is inactive and will then de-assert DIOR- or DIOW- as soon as possible after IORDY is activated.

If the system can't support this mode by using IORDY it must continue to meet the minimum cycle timing as defined by Cy4:0 of Word 51. If this is done IORDY can be ignored and the drive will respond the same way as if bit 15 of Word 51 is zero.



Note: DIOR/DIOW is shown high active as in the ATA spec.

Figure 11-2.1

If you have any questions or comments on this proposal please contact:

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The definition of the PIO Sub-Mode will be as follows:

Word 51:

Bit	7	6	5	4	3	2	1	0
	M2	M1	M0	Cy4	Cy3	Cy2	Cy1	Cy0

M2:0 selects one of eight modes shown in the mode chart and Cy4:0 select a cycle time based on the cycle time chart.

The PIO Sub-modes are as follows:

Timing	Sub-Mode 0	Sub-Mode 1	Sub-Mode 2	Sub-Mode 3	Sub-Mode 4	Sub-Mode 5	Sub-Mode 6	Sub-Mode 7
t0	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart	See Cycle Timing Chart
t1	40	30	30	30	30	20	10	5
t2	140	120	100	90	80	80	60	50
t3	60	60	50	50	50	40	30	20
t4	20	20	20	20	15	15	10	10
t5	20	20	20	20	20	20	20	10
t6	5	5	5	5	5	5	5	5
t7	40	40	40	40	30	30	30	30
t8	40	40	40	40	30	30	30	30
t9	20	20	20	20	20	10	5	5
t10	120	100	80	70	60	60	40	40
t11	60	60	60	60	60	40	20	10

Cycle timing for PIO Sub-Modes 7-0 is as follows:

	Cy 2:0							
Cy 4:3	000	001	010	011	100	101	110	111
00	60	75	80	90	100	120	125	140
01	150	160	175	200	210	220	240	250
10	260	270	280	300	320	330	340	350
11	360	375	390	400	450	500	550	600