

TO: X3T9.2 SPI  
FROM: Bill Ham (DEC)  
SUBJECT: Requirement for Glitch Free Power Up/Down for  
All SCSI Bus Drivers  
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X3T9.2/92-097R0

BACKGROUND:

When SCSI driver chips are powered up or down a possibility exists that a bus glitch could occur during or immediately after the chip power transient. These glitches can introduce errors onto the bus if the bus is active and therefore prevent both device power cycling and hot plugging. Virtually all modern SCSI drivers are guaranteed by their manufacturers to be free of these glitches. It is the intent here to add this feature as a requirement to the SCSI-3 standard.

Both the single ended and differential alternatives are included.

The glitch free operation can only be guaranteed if the power transient to the chip is fast enough. Therefore a minimum time is specified for the power transient.

PROPOSED MODIFICATIONS:

Add to Section 6.1.1 -- Single Ended Output Characteristics

All single ended SCSI bus drivers (both passive and active) are required to maintain the high impedance state during chip power up/down transients faster than 5 milliseconds (10% to 90%). This high impedance state shall be maintained until the driver is purposefully asserted by its input.

Add to Section 6.2.1 -- Differential Output Characteristics

All differential SCSI bus drivers are required to maintain the high impedance state during chip power up/down transients faster than 5 milliseconds (10% to 90%). This high impedance state shall be maintained until the driver is purposefully asserted by its input.