X3T9.2/92-10
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PCMCIA IDE
Host Interface
Implimentation Guide

Scope

This guide provides PCMCIA host system designers with specific implementation examples addressing key interface and compatibility issues. The guide assumes that the reader has a working understanding of the X3T9.2 ATA 3.0 and PCMCIA 2.0 interface standards

Overview

The PCMCIA IDE interface is based upon the existing 40 and 50 pin ATA IDE interface protocol. The command protocol for both the PCMCIA and ATA IDE interface standards are identical. The PCMCIA IDE interface differs only in the implementation of the physical and electrical protocols. I.E. the physical connector, pinouts and signal polarities

Physical Protocol

Physically the PCMCIA IDE interface will conform to PCMCIA type III specifications. As such the interface uses a 68pin PCMCIA connector for the host interface

While the width and length of Type III PCMCIA modules are identical to the Type I and Type II specifications, the Maximum height of Type III modules is still under review. The current favorites are between 10.5mm and 11mm

In addition PCMCIA IDE modules require thinner 2mm guide rails to accommodate industry standard 50.8mm HDAs

See PCMCIA Physical section for additional requirements

Electrical Protocol

The PCMCIA IDE electrical interface retains a one to one signal relationship with the signals defined by the ATA IDE standard. This allows the use of existing ATA based IDE drive interface silicon with only minor internal or external signal conditioning. Driver characteristics for each signal are assumed to meet PCMCIA 5v requirements.

Signal Descriptions

The following table shows how the ATA interface signals are mapped onto the PCMCIA interface. Note that highlighted signals are simply looped back from existing PCMCIA signals generated by the host.

Pin	PCMCIA Signal	I/O	ATA Signal	Pin	PCMCIA Signal	I/O	ATA Signal
1	GND		GND	35	GND		GND
2	D3	I/O	DD3	36	CD1-	I	<GND>
3	D4	I/O	DD4	37	D11	I/O	DD11
4	D5	I/O	DD5	38	D12	I/O	DD12
5	D6	I/O	DD6	39	D13	I/O	DD13
6	D7	I/O	DD7	40	D14	I/O	DD14
7	CE1-	O	CS1FX-	41	D15	I/O	DD15
8	A10	O		42	CE2-	O	
9	OE-	O		43	RFSH	O	
10	A11	O		44	IORD-	O	DIOR-
11	A9	O	CS3FX-	45	IOWR-	O	DIOW-
12	A8	O		46	A17	O	
13	A13	O		47	A18	O	
14	A14	O		48	A19	O	
15	WE-	O		49	A20	O	
16	IREQ-	I	INTRQ	50	A21	O	
17	VCC		VCC	51	VCC		VCC
18	VPP1			52	VPP2		
19	A16	O		53	A22	O	
20	A15	O		54	A23	O	
21	A12	O		55	A24	O	
22	A7	O		56	A25	O	
23	A6	O		57	RFU		
24	A5	O		58	RESET	O	RESET-
25	A4	O		59	WAIT-	I	IORDY
26	A3	O		60	INPACK-	I	<CE1->
27	A2	O	DA2	61	REG-	O	
28	A1	O	DA1	62	SPKR-	I	
29	A0	O	DA0	63	STSCHG	I	
30	D0	I/O	DD0	64	D8	I/O	DD8
31	D1	I/O	DD1	65	D9	I/O	DD9
32	D2	I/O	DD2	66	D10	I/O	DD10
33	IOIS16-	I	IOCS16-	67	CD2-	I	<GND>
34	GND		GND	68	GND		GND

GND, [Pin 1,34,35,68]

These four power supply signals provide the signal ground path for the PCMCIA IDE host interface signals and VCC supply.

D0 - D15 [Pin 30, 31,32, 2, 3, 4, 5, 6, 64, 65, 66, 37, 38, 39, 40, 41]

These 16 data bus I/O signals interface directly to the corresponding 16 IDE data bus signals.

CE1- [Pin 7]

This signal is generated by the PCMCIA host and is used by the PCMCIA IDE drive to qualify I/O bus cycles intended for the drive. It is the Host systems responsibility to qualify this signal so as to prevent assertion of CE1- during memory or register bus cycles.

CE1- and A9 are considered the logical replacements for CS1FX- and CS3FX-, per the ATA standard all timing including that of IOCS16 is relative to the assertion these signals.

In order to support existing BIOS drivers and diagnostic programs, CE1- generation should be limited to I/O bus cycles which occur at the existing defacto standard primary or secondary IDE drive addresses.

A9 [Pin 11]

This signal is generated by the host system in accordance with the address of the bus cycle in progress. A9 is used by the PCMCIA IDE drive to decode between the Control and Command register blocks. Note that PCMCIA IDE drives decode this signal so as to retain compatibility with the existing AT IDE drive interface standard.

IREQ- [Pin 16]

This signal is generated by the PCMCIA IDE drive and retains the same function as INTRQ as defined within the ATA specification. The polarity of this signal is inverted from its definition in the ATA specification. I.E. the PCMCIA interface requires a low true interrupt. The PCMCIA IDE drive is responsible for performing this inversion.

VCC [Pin 17, 51]

These power supply signals provide operating current to the drive. Since the PCMCIA specification limits current flow for each pin to 1/2 amp, PCMCIA IDE drives are limited to 1 amp maximum draw on VCC.

IOIS16- [Pin 33]

This signal is generated by the PCMCIA IDE drive and retains the same function as IOCS16- as defined within the ATA specification. Since IOIS16- is generated from CE1-, A9, A2, A1 and A0, IOIS16- will not be generated until after CE1- is asserted.

CD1, CD2 [Pin 36, 67]

These low true signals are grounded by the PCMCIA IDE drive to indicate when the drive is installed in the card slot. See the PCMCIA specification for additional information regarding the function of these pins.

IORD- [Pin 44]

This low true signal is generated by the host system and retain the same function as DIOR-, as defined within the ATA specification.

IOWR- [Pin 45]

This low true signal is generated by the host system and retain the same function as DIOW-, as defined within the ATA specification.

RESET [Pin 58]

This signal is generated by the host system and retains the same function as RESET , as defined within the ATA specification. The polarity of this signal is inverted from its definition in the ATA specification. I.E. the PCMCIA interface provides a high true reset. The PCMCIA IDE drive is responsible for performing this inversion.

WAIT- [Pin 59]

This low true signal is generated by the PCMCIA IDE drive and retains the same function as IORDY, as defined within the ATA specification. The function of this signal is to delay I/O cycles allowing drives with slow host interfaces to work reliably with faster host systems.

INPACK- [Pin 59]

This low true signal is generated by the PCMCIA IDE drive by lopping back CE1-. The function of this signal is to enable host system buffers specific to each card. See the PCMCIA specification for further definition of this signal and its use.

CE1-, OE- , WE-, VPP1, VPP2, A3-A8, A10 - A25, RFSH, RFU, REG-, SPKR-, STSCHG

These signals are not used by PCMCIA IDE drives. Assertion of these signals will be ignored by PCMCIA IDE compatible drives.

Configuring PCMCIA Host Systems for PCMCIA IDE Drives

Automatically configuring a PCMCIA Host System to support PCMCIA IDE drives requires that both PCMCIA IDE drive identification and ATA compatibility issues be addressed.

Identifying PCMCIA IDE Drives

Since some PCMCIA IDE drives will not initially support the PCMCIA attribute registers, PCMCIA host systems must identify these drives using the existing AT IDE identification sequence. This sequence is compatible with existing BIOS and operating system drivers.

The sequence used by these existing drivers require that the PCMCIA IDE register blocks retain functional and address compatibility with the ATA IDE specification.

Identification Sequence:

0) Program Card Slot CE1- Address Range to 1F0 - 3F7.
1) Loop Until 1F7H (Status) Bit 7 (Drive Busy) not set.
2) I/O Write 55H to 1F4H (Cylinder Low).
3) I/O Write AAH to 1F5H (Cylinder High).
4) I/O Read 1F4 (Cylinder Low).
5) IF I/O Read = 55H then Card_Type = IDE.

Once the PCMCIA host system has identified that a card slot contains a PCMCIA IDE drive it should proceed with the normal ATA initialization of the drive. If the card fails the IDE Identification Sequence then the PCMCIA host system should assume that a non IDE PCMCIA card is installed and use the PCMCIA card initialization protocol.