The Dip

1. The problem:

The picture shown in Figure 1, page 1 represents a much to often observed waveform of a SCSI signal line during deassertion. Similarly Figure 2, page 2 describes the waveform of a typical SCSI signal line during assertion. It is not uncommon for this non monotonic transition ("the dip") to traverse twice the receiver decision threshold thus causing a false trigger.

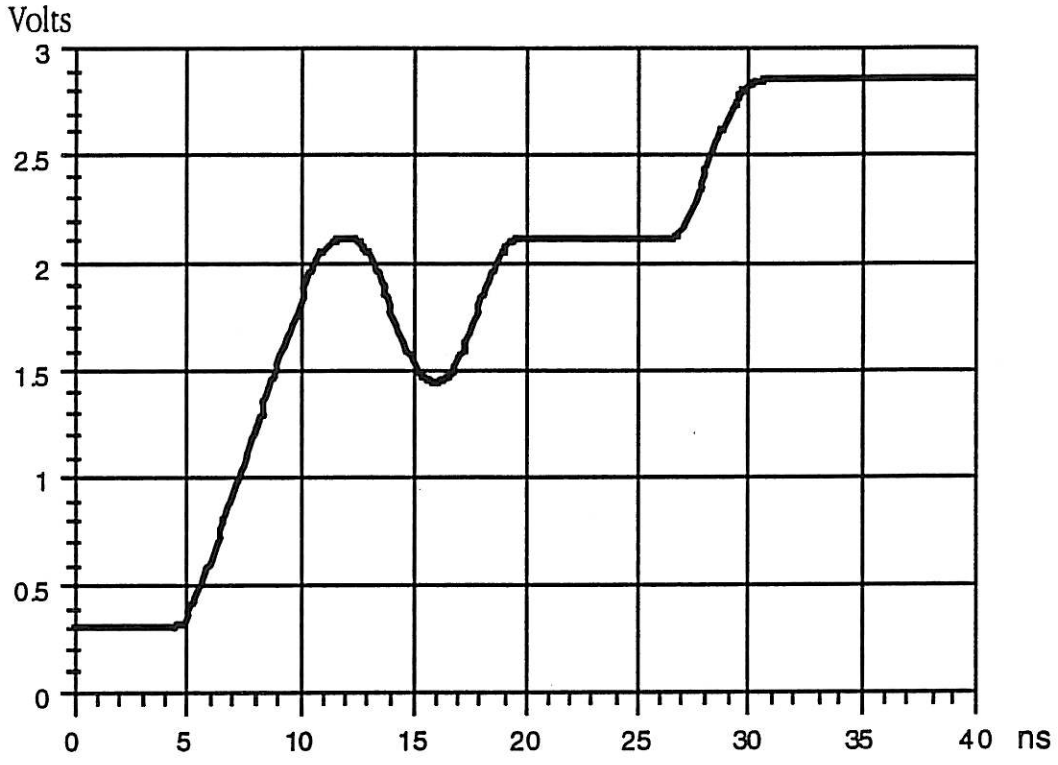

Figure 1: Typical SCSI signal line deassertion waveform.

Often this type of waveform is attributed to crosstalk, "ground bounce" or unidentified "noise". Both experimental measurements and theoretical analysis have shown that "the dip" can be associated with the presence of a significant lumped capacitive load on the SCSI bus. This capacitance reflects back the high frequency energy components of the incident wave creating the non monotonic transition.

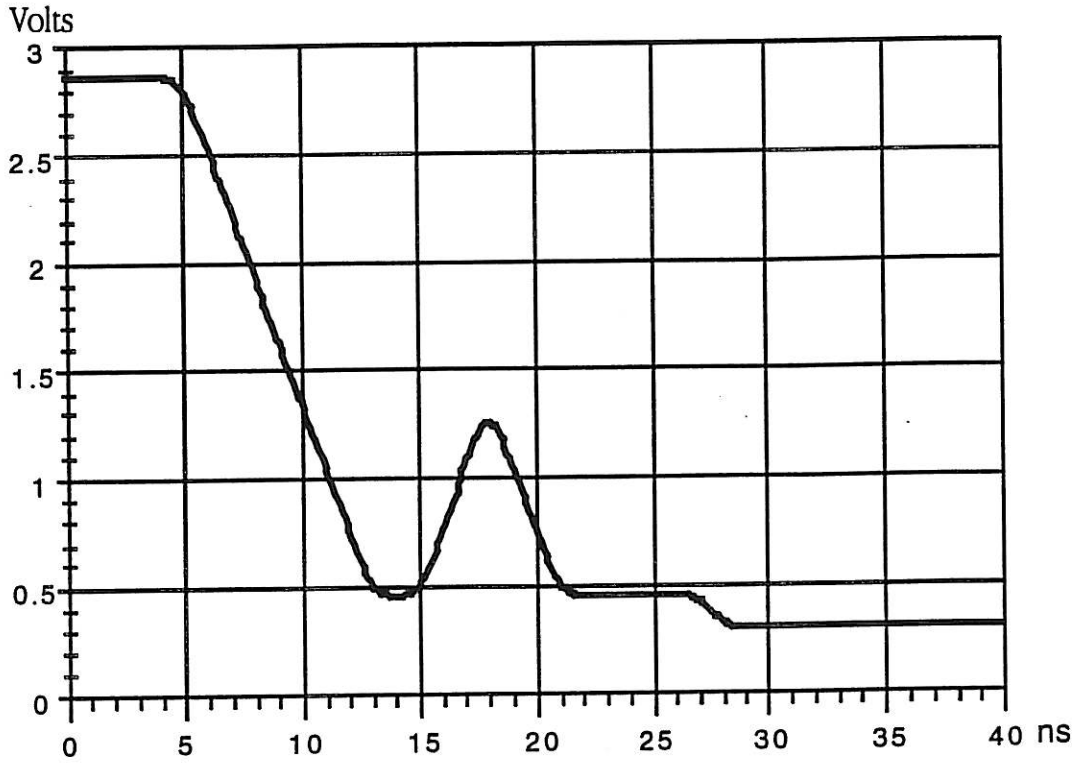

Figure 2: Typical SCSI signal line deassertion waveform.

As "the dip" is one of the major problems of the SCSI physical channel, it is very important to attempt to minimize its amplitude. The present drive for high single ended impedance cables , while trying to improve the amplitude of the initial deassertion step, has as a side effect an increase in the amplitude of "the dip".

While fully supporting the effort for introducing high impedance SCSI cables, this paper tries to identify additional parameters that have to be controlled in order to guarantee a fully functional physical channel for the SCSI bus.

Over the last few years digital techniques have been developed which guarantee receiver immunity to non monotonic transitions by redundant sampling. These techniques have proven very effective and a large number of the SCSI systems on the market rely upon them. Unfortunately these techniques are vendor and technology dependent. Any change to a SCSI controller I.C. requires lengthy reevaluations in order to ensure that the black magic of the "glitch eater" has not been altered.

In the same time, as the transaction speed on the bus increases, fewer and fewer nanoseconds can be wasted eating glitches.

The goal of this paper is to propose a quantitative measure of the amplitude of "the dip" as well as to define acceptable domains for the edge transition rate, the maximum lumped capacitive load per node and the cable single ended characteristic impedance.

2. The edge:

The cable characteristic impedance together with the node load capacitance act as a low pass filter. The relation between the time constant of this filter and the signal edge transition time determine the best model for the signal edge. The low-pass filter will reflect the incident energy at frequencies outside its pass-band and transmit the rest.

It can be shown that the time constant of the low pass filter formed by a the transmission line and a tap load capacitance is:

$$\tau = 2.2 * \frac{Z_0}{2} * C_0$$

where:

τ = low-pass filter time constant.
Z_0 = SCSI cable single ended characteristic impedance.
C_0 = SCSI node lumped load capacitance value.

For normal cables with a characteristic impedance between 60 Ω and 120 Ω and for a node load capacitance between 15 pF and 25 pF the time constant varies between 1 ns and 4 ns. The expected range for the signal edge transition time is between 2 ns and 10 ns.

If the incident wave transition time is significantly faster than the low pass filter time constant the maximum amplitude of the reflected wave will depend almost exclusively upon the incident edge maximum rate of change (max dV/dt) . On the other side, the amplitude of the reflection generated by an edge much slower than the filter time constant is negligible.

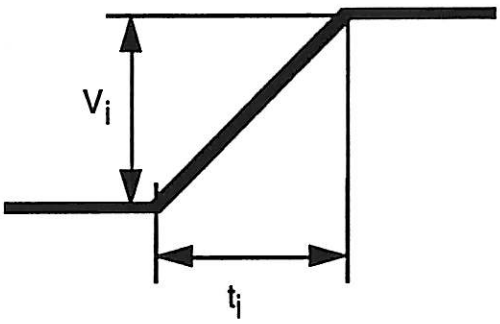

Figure 3.

In this specific case, because the incident edge transition time is comparable with the low pass filter time constant, a more detailed analysis is necessary. It should take into account the duration of the edge transition as well as its average slope. The average edge slope can confortably replace the maximum rate of change.

Assuming that the maximum edge slope is of little significance given the relation between time constants I am going to use a very simple linear model for the signal edge as shown in Figure 3, page 3. The incident wave transition time t_i represents the SCSI signal transition time between 10% and 90% while the incident wave amplitude V_i represents the SCSI signal edge amplitude.

3. The capacitance:

The signal line load capacitance as considered here is the lumped capacitance measured at the bus connector of a SCSI device. It includes the connector/connectors capacitance, the PCB trace capacitance, the SCSI I.C. driver/receiver capacitance and the effect of various internal stubs and associated "nasties". This capacitance does not include any section of the bus itself in the case of feed-through devices.

Assuming only reasonable size internal stubs this capacitance can be measured using a standard impedance bridge at a test frequency of 10 MHz. Particular attention should be given to the DC bias voltage which should be varied between 0.4 V and 2.85 V in search for the maximum capacitance value.

4. The reflection:

This calculation assumes an incident edge as defined in section 2 traveling on a transmission line of characteristic impedance Z_0 and reaching a lumped capacitive tap of value C_0 as shown in Figure 4, page 5.

Under these circumstances the maximum amplitude of the reflected wave is given by:

$$V_r = -\frac{V_i}{t_i} * \frac{C_0 * Z_0}{2} * \left(1 - e^{-\frac{2*t_i}{C_0*Z_0}}\right)$$

where:

V_r = amplitude of the reflected wave.

V_i = amplitude of incident wave.

t_i = transition time (10% to 90%) of incident wave.

Z_0 = SCSI cable single ended characteristic impedance.

C_0 = SCSI node lumped load capacitance value.

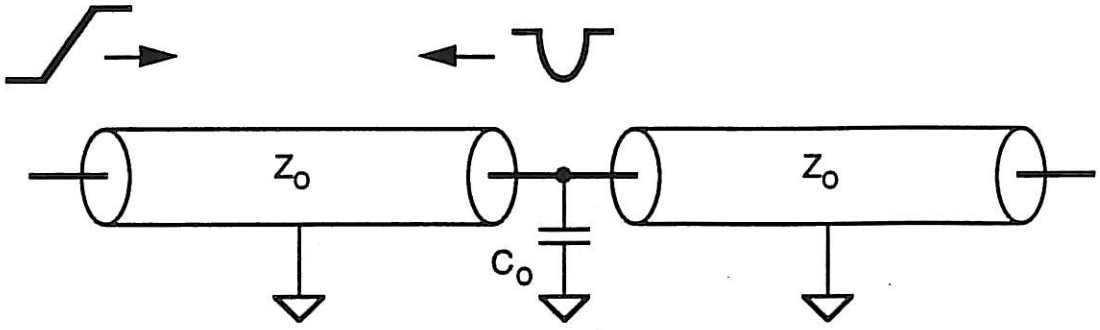

Figure 4.

The time tw_r in which the reflected wave amplitude will drop to less than 10% of its maximum amplitude is given by:

$$tw_r = t_i + 1.1 * C_0 * Z_0$$

Practically it is quite common to find a configuration in which two identical primary reflections of this type will add up. Such a configuration is shown in Figure 5, page 5. This scenario for the addition of multiple primary reflections is valid only during deassertion.

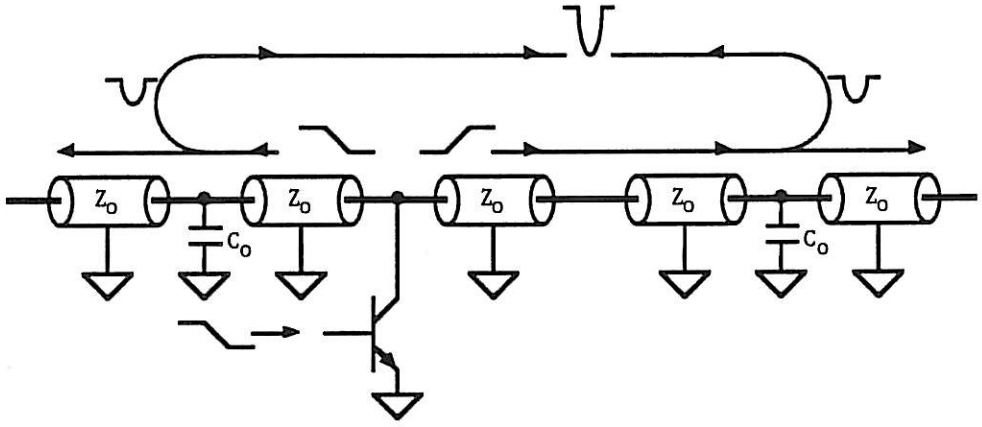

Figure 5.

For this reason, neglecting all secondary reflections, the worst case amplitude of the reflected wave for signal deassertion should be calculated at least as:

$$V_r = -\frac{V_i}{t_i} * C_0 * Z_0 * \left(1 - e^{-\frac{2*t_i}{C_0*Z_0}}\right)$$

5. The numbers:

5.1. Assertion edge:

The amplitude of the reflected wave created by a signal assertion is:

$$V_r = V_{ol} + \frac{V_{oh} - V_{ol}}{t_i} * \frac{C_0 * Z_0}{2} * \left(1 - e^{-\frac{2*t_i}{C_0 * Z_0}}\right)$$

where:

V_r = amplitude of the reflected wave.

V_{ol} =output voltage of an asserted driver immediately following assertion.

V_{oh} = output voltage of a deasserted driver in steady state which is the steady state voltage level on a deasserted SCSI signal line as determined by the bus termination.

t_i = transition time (10% to 90%) of the assertion edge.

Z_0 = SCSI cable single ended characteristic impedance.

C_0 = SCSI node lumped load capacitance value.

The amplitude of the incident wave is independent (in the first approximation) of the cable characteristic impedance. Few steps to control and reduce the amplitude of the reflected wave are:

- reduce the node load capacitance C_0
- reduce the assertion edge amplitude V_i by controlling the steady -state voltage level on a deasserted SCSI signal line.
- increase the assertion edge transition time t_i.
- reduce (!!!) the cable single ended characteristic impedance Z_0.

5.1.1. Average SCSI 2 implementation:

For a careful implementation of a SCSI 2 physical channel:

- the steady state voltage level on a deasserted SCSI signal line is 2.85 V.
- the V_{ol} voltage level immediately following the assertion is 0.5 V.
- the single ended cable characteristic impedance is 100 Ω.
- the node load capacitance is between 5 pF and 30 pF.
- the assertion edge transition time is between 2 ns and 12 ns.

Under these conditions the amplitude of the reflected wave produced by the addition of two primary reflections is calculated in Table 1, page 7 and plotted in Figure 6, page 7.

$t_i \backslash C_0$	5	7.5	10	12.5	15	17.5	20	22.5	25	27.5	30	pF
2	0.79	0.94	1.09	1.23	1.38	1.53	1.67	1.82	1.97	2.12	2.26	
3	0.70	0.79	0.89	0.99	1.09	1.19	1.28	1.38	1.48	1.58	1.67	
4	0.65	0.72	0.79	0.87	0.94	1.01	1.09	1.16	1.23	1.31	1.38	
5	0.62	0.68	0.73	0.79	0.85	0.91	0.97	1.03	1.09	1.15	1.20	
6	0.60	0.65	0.70	0.74	0.79	0.84	0.89	0.94	0.99	1.04	1.09	
7	0.58	0.63	0.67	0.71	0.75	0.79	0.84	0.88	0.92	0.96	1.00	
8	0.57	0.61	0.65	0.68	0.72	0.76	0.79	0.83	0.87	0.90	0.94	
9	0.57	0.60	0.63	0.66	0.70	0.73	0.76	0.79	0.83	0.86	0.89	
10	0.56	0.59	0.62	0.65	0.68	0.71	0.73	0.76	0.79	0.82	0.85	
11	0.55	0.58	0.61	0.63	0.66	0.69	0.71	0.74	0.77	0.79	0.82	
12	0.55	0.57	0.60	0.62	0.65	0.67	0.70	0.72	0.74	0.77	0.79	
ns												

Table 1: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the assertion transition time (10% to 90%) in ns.

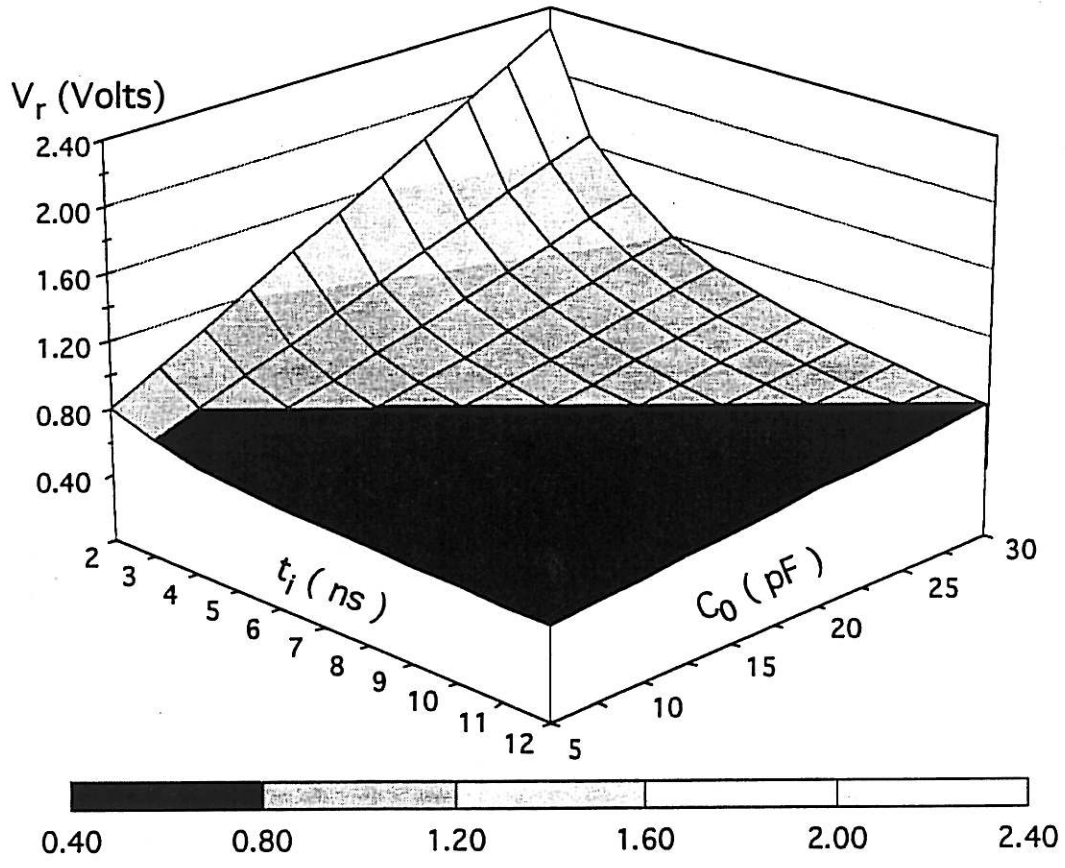

Figure 6.

It can be notices than even in this quite reasonable implementation the amplitude of the reflected wave is very high and sometimes well above the minimum receiver decision threshold of 0.8 V.

5.1.2. Worst case SCSI 2 implementation:

This involves a rather extreme but not impossible SCSI configuration with a maximum TERMPWR voltage, a worst case passive terminator and a high impedance ribbon cable bus. Therefore:

- the steady state voltage level on a deasserted SCSI signal line is 3.27 V.
- the Vol voltage level immediately following the assertion is 0.5 V.
- the single ended cable characteristic impedance is 125 Ω.
- the node load capacitance is between 5 pF and 30 pF.
- the assertion edge transition time is between 2 ns and 12 ns.

The amplitude of the reflected wave generated by a signal assertion is calculated in Table 2, page 8 and shown in Figure 7, page 9.

$t_i \backslash C_0$	5	7.5	10	12.5	15	17.5	20	22.5	25	27.5	30	pF
2	0.93	1.15	1.37	1.58	1.80	2.01	2.23	2.45	2.66	2.88	3.10	
3	0.79	0.93	1.08	1.22	1.37	1.51	1.65	1.80	1.94	2.09	2.23	
4	0.72	0.82	0.93	1.04	1.15	1.26	1.37	1.47	1.58	1.69	1.80	
5	0.67	0.76	0.85	0.93	1.02	1.11	1.19	1.28	1.37	1.45	1.54	
6	0.64	0.72	0.79	0.86	0.93	1.00	1.08	1.15	1.22	1.29	1.37	
7	0.62	0.69	0.75	0.81	0.87	0.93	0.99	1.06	1.12	1.18	1.24	
8	0.61	0.66	0.72	0.77	0.82	0.88	0.93	0.99	1.04	1.10	1.15	
9	0.60	0.64	0.69	0.74	0.79	0.84	0.88	0.93	0.98	1.03	1.08	
10	0.59	0.63	0.67	0.72	0.76	0.80	0.85	0.89	0.93	0.98	1.02	
11	0.58	0.62	0.66	0.70	0.74	0.78	0.81	0.85	0.89	0.93	0.97	
12	0.57	0.61	0.64	0.68	0.72	0.75	0.79	0.82	0.86	0.90	0.93	
ns												

Table 2: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the assertion transition time (10% to 90%) in ns.

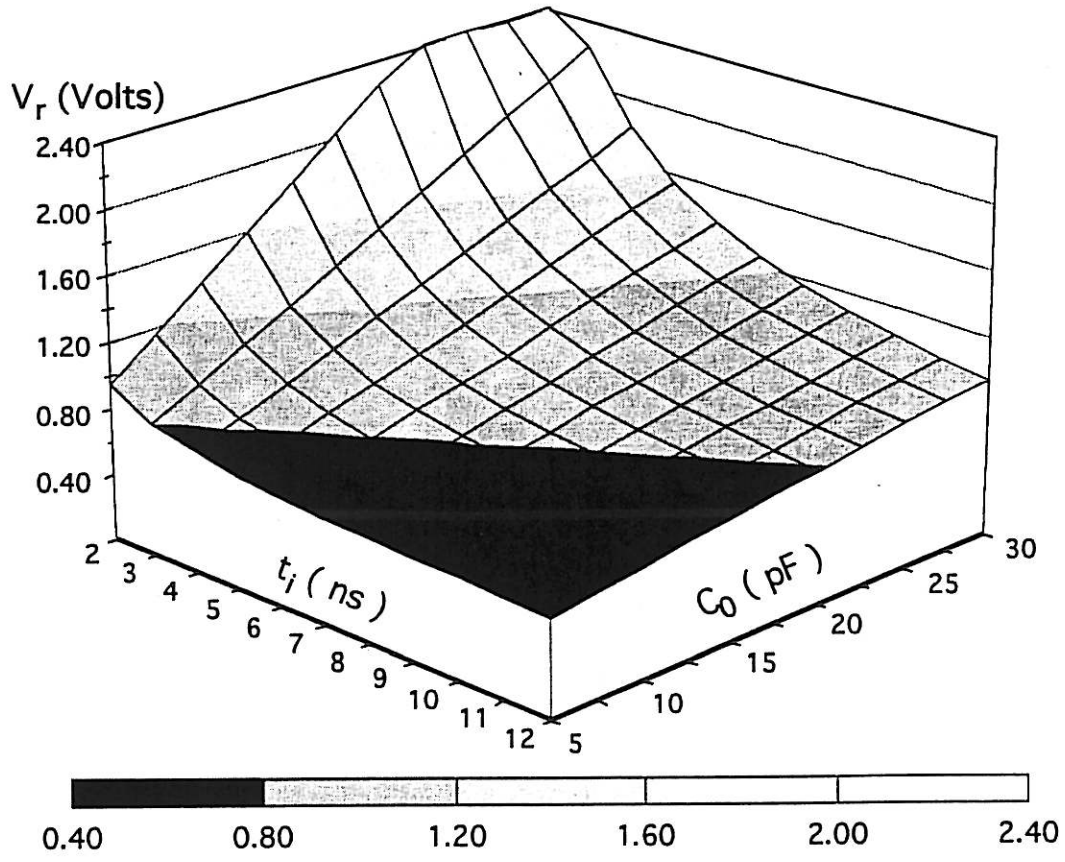

Figure 7.

5.1.3. Average SCSI 1 implementation:

For comparison, a SCSI 1 implementation of average quality is also analyzed. Thus:

- the steady state voltage level on a deasserted SCSI signal line is 2.85 V.
- the Vol voltage level immediately following the assertion is 0.5 V.
- the single ended cable characteristic impedance is 75 Ω.
- the node load capacitance is between 10 pF and 100 pF.
- the assertion edge transition time is between 2 ns and 12 ns.

The amplitude of the reflected wave generated by a signal assertion is calculated in Table 3, page 10 and shown in Figure 8, page 10.

$t_i \backslash C_0$	10	20	30	40	50	60	70	80	90	100	110	pF
2	0.94	1.38	1.82	2.26	2.70	3.14	3.58	4.02	4.47	4.91	5.35	
3	0.79	1.09	1.38	1.67	1.97	2.26	2.56	2.85	3.14	3.44	3.73	
4	0.72	0.94	1.16	1.38	1.60	1.82	2.04	2.26	2.48	2.70	2.92	
5	0.68	0.85	1.03	1.20	1.38	1.56	1.73	1.91	2.09	2.26	2.44	
6	0.65	0.79	0.94	1.09	1.23	1.38	1.53	1.67	1.82	1.97	2.12	
7	0.63	0.75	0.88	1.00	1.13	1.26	1.38	1.51	1.63	1.76	1.88	
8	0.61	0.72	0.83	0.94	1.05	1.16	1.27	1.38	1.49	1.60	1.71	
9	0.60	0.70	0.79	0.89	0.99	1.09	1.19	1.28	1.38	1.48	1.58	
10	0.59	0.68	0.76	0.85	0.94	1.03	1.12	1.20	1.29	1.38	1.47	
11	0.58	0.66	0.74	0.82	0.90	0.98	1.06	1.14	1.22	1.30	1.38	
12	0.57	0.65	0.72	0.79	0.87	0.94	1.01	1.09	1.16	1.23	1.31	
ns												

Table 3: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the assertion transition time (10% to 90%) in ns.

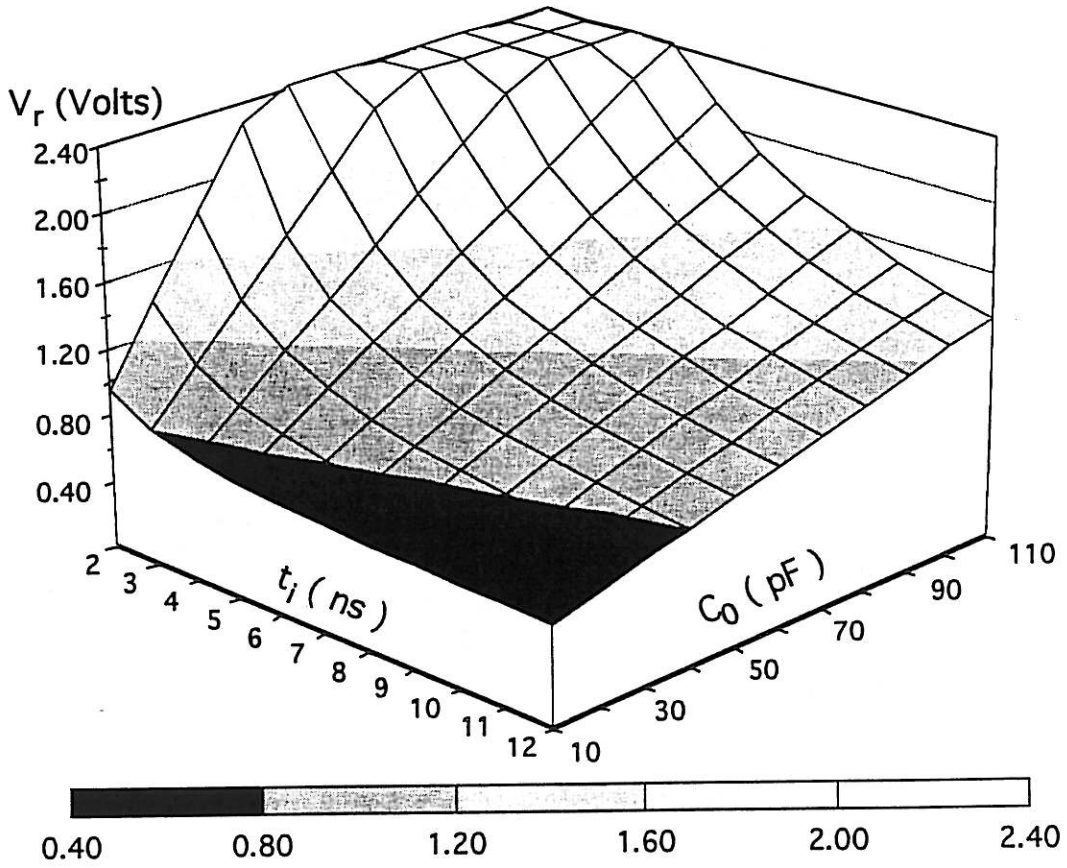

Figure 8.

5.2. Deassertion edge:

For the signal deassertion analysis the amplitude of the reflected wave should be modified and referenced to ground. In this case the goal will be to maximize the minimum amplitude of the reflected wave.

Assuming a SCSI driver far from both bus terminations (at least 12 inches) the amplitude of the initial deassertion step V_i is given by:

$$V_i = I_t * \frac{Z_0}{2}$$

where:

V_i = amplitude of the initial deassertion step and amplitude of incident wave .

I_t =steady state current through the asserted driver (provided by the two terminations).

Z_0 = SCSI cable single ended characteristic impedance.

The worst case situation for deassertion from the point of view of a minimum amplitude reflected wave is the combination of two primary reflections (see Figure 5, page 5). Thus the minimum amplitude of the reflected wave can be written as::

$$V_r = I_t * \frac{Z_0}{2} * \left(1 - \frac{C_0 * Z_0}{t_i} * \left(1 - e^{-\frac{2*t_i}{C_0 * Z_0}}\right)\right) + V_{ol}$$

Few ways to accomplish the maximum reflection wave amplitude objective are:

- reduce the node load capacitance C_0
- maximize the steady state current through the asserted driver I_t.
- increase the deassertion edge transition time t_i.

5.2.1. Average SCSI 2 implementation:

Using the same careful SCSI 2 implementation as at 5.1.1 the assumptions are :

- the steady state current through an asserted driver is 44.8 mA.
- the Vol voltage level previous to deassertion is 0.3 V.
- the single ended cable characteristic impedance is 100 Ω.
- the node load capacitance is between 5 pF and 30 pF.
- the deassertion edge transition time is between 2 ns and 12 ns.

$t_i \backslash C_0$	5	7.5	10	12.5	15	17.5	20	22.5	25	27.5	30	pF
2	1.98	1.70	1.44	1.20	0.98	0.78	0.60	0.45	0.31	0.18	0.07	
3	2.17	1.98	1.80	1.61	1.44	1.28	1.12	0.98	0.84	0.72	0.60	
4	2.26	2.12	1.98	1.84	1.70	1.57	1.44	1.32	1.20	1.08	0.98	
5	2.32	2.20	2.09	1.98	1.87	1.76	1.65	1.54	1.44	1.34	1.24	
6	2.35	2.26	2.17	2.07	1.98	1.89	1.80	1.70	1.61	1.53	1.44	
7	2.38	2.30	2.22	2.14	2.06	1.98	1.90	1.82	1.74	1.67	1.59	
8	2.40	2.33	2.26	2.19	2.12	2.05	1.98	1.91	1.84	1.77	1.70	
9	2.42	2.35	2.29	2.23	2.17	2.10	2.04	1.98	1.92	1.86	1.80	
10	2.43	2.37	2.32	2.26	2.20	2.15	2.09	2.04	1.98	1.92	1.87	
11	2.44	2.39	2.34	2.29	2.23	2.18	2.13	2.08	2.03	1.98	1.93	
12	2.45	2.40	2.35	2.31	2.26	2.21	2.17	2.12	2.07	2.03	1.98	
ns												

Table 4: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the deassertion transition time (10% to 90%) in ns.

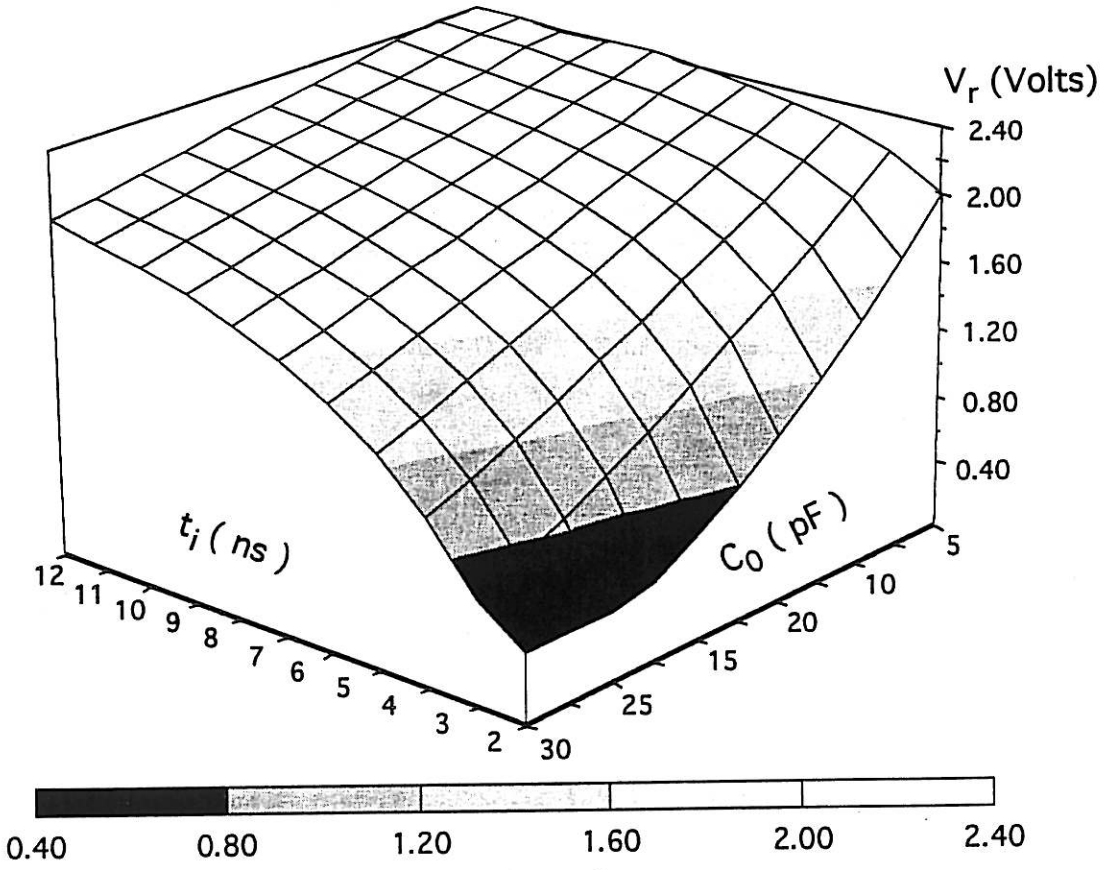

Figure 9.

Under these conditions the amplitude of the reflected wave produced by the addition of two primary reflections is calculated in Table 4, page 12 and plotted in Figure 9, page 12.

Another dimension of the problem that should be explored is the dependency between the minimum amplitude of the reflected wave and the cable characteristic impedance.

For this analysis I assume a node load capacitance of 25 pF. Considering a cable impedance range of 60 Ω to 110 Ω the minimum amplitude of the reflected wave is calculated as a function of cable impedance and as a function of the deassertion edge transition time The results are presented in Table 5, page 13.

$t_i \backslash Z_0$	60	65	70	75	80	85	90	95	100	105	110	Ω
2	0.71	0.67	0.64	0.59	0.54	0.49	0.43	0.37	0.31	0.24	0.17	
3	0.98	0.99	0.98	0.97	0.96	0.94	0.91	0.88	0.84	0.80	0.76	
4	1.14	1.17	1.19	1.20	1.21	1.22	1.21	1.21	1.20	1.18	1.16	
5	1.24	1.28	1.32	1.35	1.38	1.40	1.42	1.43	1.44	1.44	1.44	
6	1.31	1.36	1.41	1.46	1.50	1.53	1.56	1.59	1.61	1.63	1.65	
7	1.36	1.42	1.48	1.53	1.58	1.63	1.67	1.71	1.74	1.77	1.80	
8	1.39	1.46	1.53	1.59	1.64	1.70	1.75	1.80	1.84	1.88	1.92	
9	1.42	1.49	1.56	1.63	1.69	1.75	1.81	1.87	1.92	1.97	2.01	
10	1.44	1.52	1.59	1.67	1.73	1.80	1.86	1.92	1.98	2.03	2.09	
11	1.46	1.54	1.62	1.69	1.77	1.84	1.90	1.97	2.03	2.09	2.15	
12	1.48	1.56	1.64	1.72	1.79	1.87	1.94	2.01	2.07	2.14	2.20	
ns												

Table 5: Reflected wave amplitude in Volts as a function of the cable characteristic impedance in Ω and of the deassertion transition time (10% to 90%) in ns.

It can be immediately noticed that for fast transition times the optimum cable characteristic impedance is around 85Ω to 90Ω. This is true only for relative high node capacitance values. A decrease by 10 pF of the node capacitance value will increase the optimum cable impedance above 110 Ω.

A plot of these data points is shown in Figure 10, page 14.

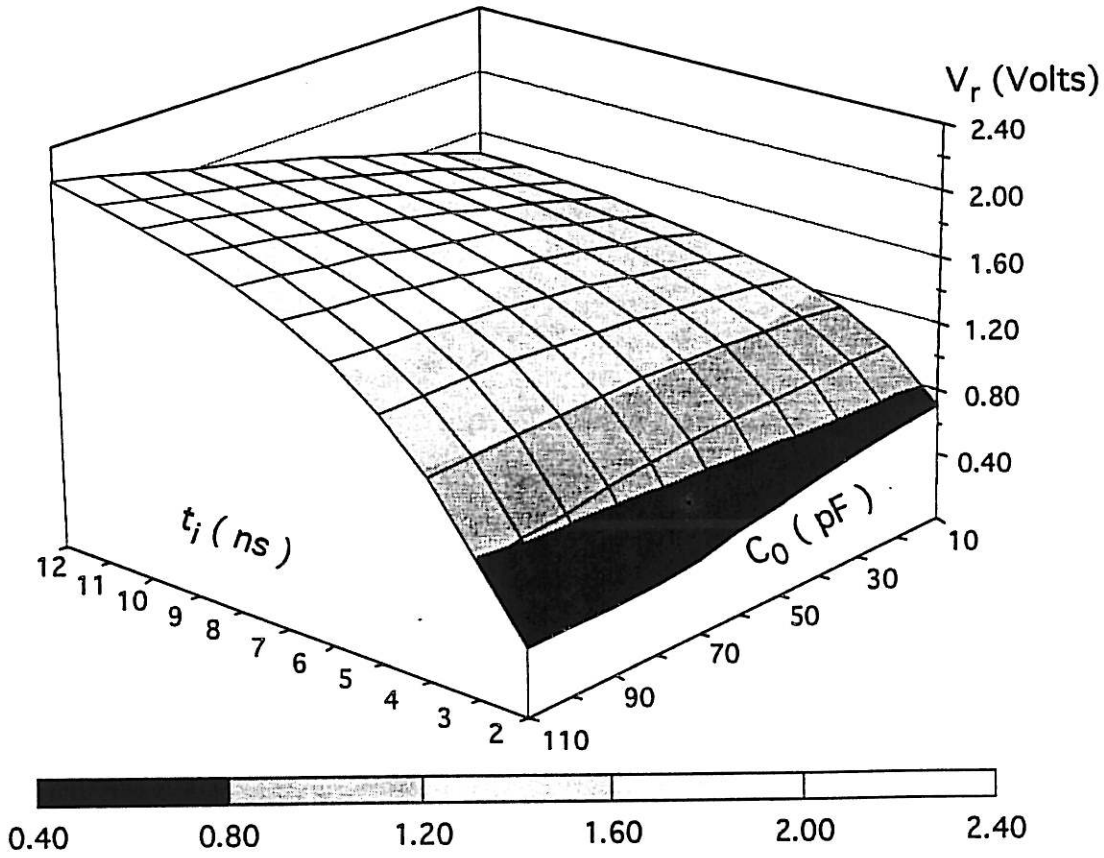

Figure 10.

5.2.2. Worst case SCSI 2 implementation:

As before this analysis assumes a rather extreme but not impossible SCSI configuration with maximum TERMPWR voltage and a worst case passive terminator. Thus:

- the steady state current through an asserted driver is 32 mA.
- the Vol voltage level previous to deassertion is 0.3 V.
- the single ended cable characteristic impedance is 100 Ω.
- the node load capacitance is between 5 pF and 30 pF.
- the deassertion edge transition time is between 2 ns and 12 ns.

The amplitude of the reflected wave generated by a signal deassertion is calculated in Table 6, page 15 and shown in Figure 11, page 15.

$t_i \backslash C_0$	5	7.5	10	12.5	15	17.5	20	22.5	25	27.5	30	pF
2	1.50	1.30	1.11	0.94	0.78	0.64	0.52	0.40	0.30	0.21	0.13	
3	1.63	1.50	1.37	1.24	1.11	1.00	0.89	0.78	0.69	0.60	0.52	
4	1.70	1.60	1.50	1.40	1.30	1.21	1.11	1.03	0.94	0.86	0.78	
5	1.74	1.66	1.58	1.50	1.42	1.34	1.26	1.19	1.11	1.04	0.97	
6	1.77	1.70	1.63	1.57	1.50	1.43	1.37	1.30	1.24	1.18	1.11	
7	1.79	1.73	1.67	1.61	1.56	1.50	1.44	1.39	1.33	1.28	1.22	
8	1.80	1.75	1.70	1.65	1.60	1.55	1.50	1.45	1.40	1.35	1.30	
9	1.81	1.77	1.72	1.68	1.63	1.59	1.54	1.50	1.46	1.41	1.37	
10	1.82	1.78	1.74	1.70	1.66	1.62	1.58	1.54	1.50	1.46	1.42	
11	1.83	1.79	1.75	1.72	1.68	1.65	1.61	1.57	1.54	1.50	1.46	
12	1.83	1.80	1.77	1.73	1.70	1.67	1.63	1.60	1.57	1.53	1.50	
ns												

Table 6: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the deassertion transition time (10% to 90%) in ns.

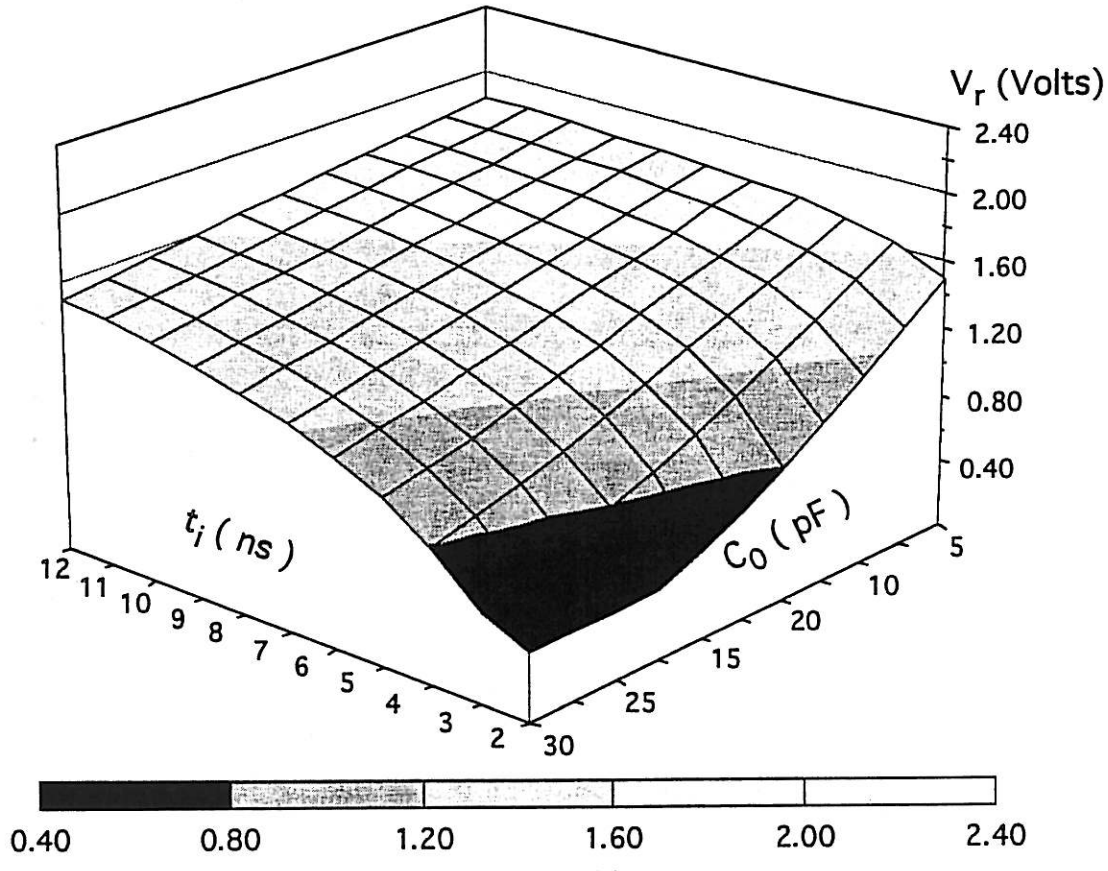

Figure 11.

5.2.3. Average SCSI 1 implementation:

The assumptions for this analysis are;

- the steady state current through an asserted driver is 35 mA.
- the Vol voltage level previous to deassertion is 0.3 V.
- the single ended cable characteristic impedance is 75 Ω.
- the node load capacitance is between 10 pF and 100 pF.
- the deassertion edge transition time is between 2 ns and 12 ns.

The amplitude of the reflected wave generated by a signal assertion is calculated in Table 7, page 16 and shown in Figure 12, page 17.

$t_i \backslash C_0$	10	20	30	40	50	60	70	80	90	100	110	pF
2	1.12	0.70	0.39	0.16	0.00	-0.13	-0.22	-0.30	-0.37	-0.42	-0.47	
3	1.28	0.97	0.70	0.48	0.30	0.16	0.05	-0.05	-0.13	-0.19	-0.25	
4	1.37	1.12	0.90	0.70	0.53	0.39	0.27	0.16	0.07	0.00	-0.07	
5	1.42	1.22	1.03	0.85	0.70	0.56	0.44	0.33	0.24	0.16	0.09	
6	1.45	1.28	1.12	0.97	0.83	0.70	0.58	0.48	0.39	0.30	0.23	
7	1.47	1.33	1.19	1.06	0.93	0.81	0.70	0.60	0.51	0.42	0.35	
8	1.49	1.37	1.24	1.12	1.01	0.90	0.79	0.70	0.61	0.53	0.45	
9	1.50	1.39	1.28	1.18	1.07	0.97	0.87	0.78	0.70	0.62	0.55	
10	1.51	1.42	1.32	1.22	1.12	1.03	0.94	0.85	0.77	0.70	0.63	
11	1.52	1.43	1.34	1.25	1.17	1.08	1.00	0.91	0.84	0.77	0.70	
12	1.53	1.45	1.37	1.28	1.20	1.12	1.04	0.97	0.90	0.83	0.76	
ns												

Table 7: Reflected wave amplitude in Volts as a function of the node load capacitance in pF and of the deassertion transition time (10% to 90%) in ns.

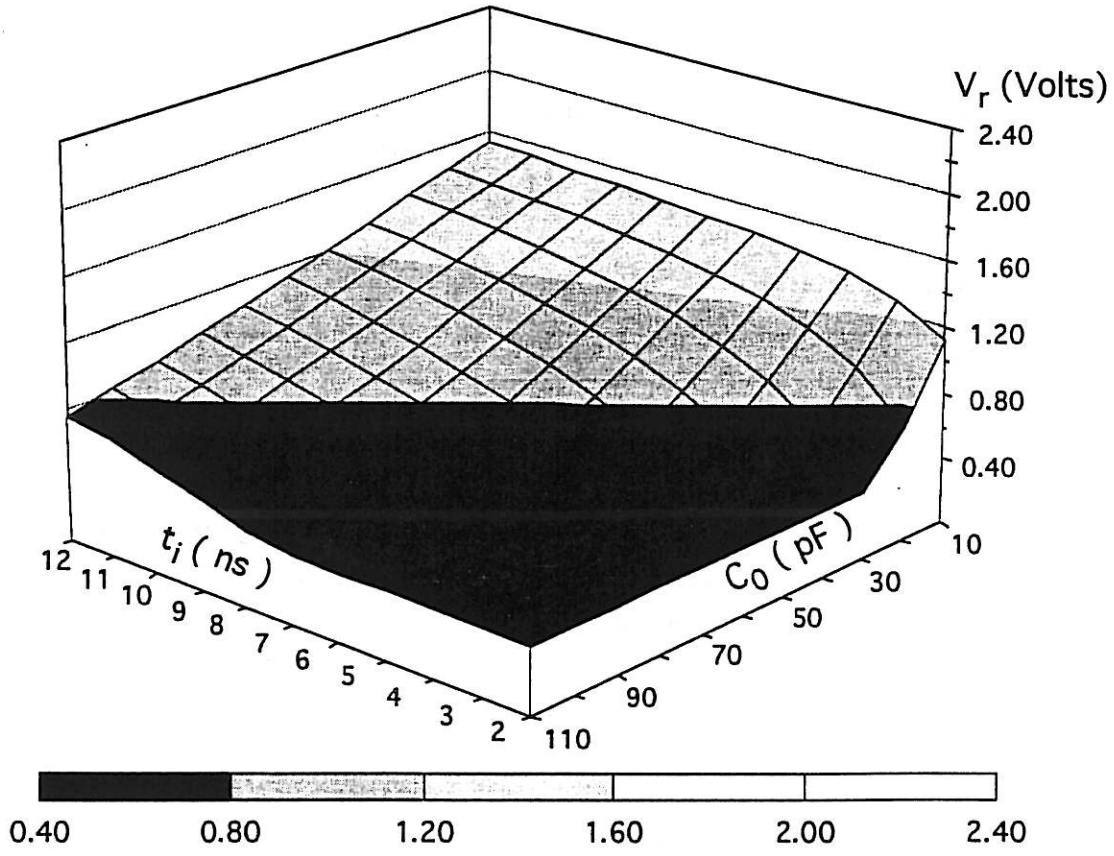

Figure 12.

6. Conclusions:

6.1. Driver edge transition time:

The driver transition time is the primary mean by which the amplitude of "the dip" can be controlled and reduced. From the above data guaranteed minimum rise and fall times of at least 9 ns can significantly improve the reliability of the SCSI physical channel. Under this circumstance, in a reasonable SCSI implementation "the dip" will remain outside the receiver decision threshold.

On a closely related issue the driver transition time should be specified for its specific utilization conditions (e. g. driving the tap of a transmission line with a characteristic impedance between 75Ω and 110 Ω and a load capacitance between 10 pF and 20 pF).

6.2. Termination:

It has been shown that for assertion it is important to maintain a relative low steady state voltage on the deasserted line. Similarly, for deassertion it is important to maximize the steady state current supplied by the termination to an asserted driver.

The clear recommendation is the use of a regulated termination that can maintain an accurate Thevenin equivalent voltage independent of the TERMPWR voltage. In the same time it is highly desirable the use of a termination that can supply the maximum specified current to a deasserted driver independent of Vol.

Considering the termination options available today the "alternative 2" type is the clear winner. In the same time it should be emphasized that the tolerance of the output voltage of the regulator present in this terminator is of great importance and should be kept to a minimum. The same is true for the tolerance of the terminating resistors.

6.3. Node load capacitance:

The above discussion has shown that the node load capacitance is the reason for "the dip". It is clear that minimizing its value will reduce the amplitude of "the dip".

Experimental measurements have shown that there are a number of well designed SCSI devices on the market with load capacitance values below 15 pF . I believe the SCSI physical channel specification should require a node load capacitance below 20 pF measured at the device connection point to the bus..

It is often the case that capacitors are added (yes ADDED ???) to the SCSI bus in order to fix EMI problems. Significantly more effective and clearly less damaging is the addition of high loss ferrite beads in series with the signal line taps (not on the bus itself). They have the benefit of both reducing the edge transition time and canceling some of the node load capacitance.

Additional information should also be added describing the measurement method for this capacitance. For devices that offer easy access to their connection point to the bus the capacitance can be measured using a standard impedance bridge at 10 MHz. If the SCSI bus can not be disconnected from the device for the purpose of this measurement (the bus is routed through the device) a TDR test can be used.

6.4. Cable characteristic impedance:

Depending upon the edge transition time an increase in cable impedance may increase or decrease the size of "the dip" during deassertion. A high impedance cable increases the size of "the dip" during assertion.

It is clear that higher is not necessarily better in the case of cable impedance. I believe the cable single ended impedance should be limited to a range between 80Ω and 100 Ω. The use of high impedance ribbon cables should be discouraged unless the edge rates can be maintained very slow and/or the node load capacitance can be reduced significantly.