X3T9.2/91-198

SCSI-3 Working Group Recommendations
Emulex Corporation; Nov 13, 1991

Recommendations to the SCSI-3 working group for consideration into SCSI-3 Parallel Interface (SPI)

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SCOPE

This paper address several technical considerations of the proposed SCSI-3 specification. The objective of these suggestions is to improve the overall useability of the spec for both system implementors and device designers. On the final two pages specific recommendations are made for consideration by the committee for inclusion into the specification. Where applicable, comments are directed to specific paragraph numbers as outlined in the working draft specification X3T9.2/91-10 rev 1a, dated June 20, 1991.

CABLE RECOMMENDATIONS: (Section 5.2)

The full performance and reliability of the bus will be difficult to reach unless higher performance and tighter tolerance cables are specified. Many simulations and tests have confirmed the importance of both actual cable impedance (as opposed to manufactures specs) and the use of mixed impedance cables in large SCSI systems.

The SCSI-3 spec should include at least a recommendation as to cable impedance and measuring technique. The spec should include a range say 80-100 ohms that can be achieved with practical cables. The loss characteristics (Db/meter @ a specified frequency) and DC resistance should be included. The spec may include reference to specific manufacturers' cables that meet the recommendation.

SINGLE-ENDED ALTERNATIVE: section 6.1

Several terminations schemes and improvements have been used effectively in SCSI-2 and proposed for SCSI-3. Most of the suggested improvements are designed to overcome implementation difficulties encountered in practical system configurations. Specifically these are:

Wide variation in cable impedance.
Low impedance of commonly used low-cost flat ribbon cables.
Mismatch of termination resistance to cable impedance
Insufficient quiescent assertion current.

Wide receiver and input and hysteresis tolerances.
Practical difficulties of regulating termpower voltages.
Stub and capacitive loading effects.
Process variations typical of CMOS interface chips.

Due to a number of technical, economic, and compatibility reasons, the spec will likely continue to have a number of compromises. There is, however, an opportunity to tighten certain parameters of the termination scheme to improve margins and therefor performance and reliability.

Specifically the termination resistance and tolerance should be reduced to better match practical cables and maximize margins. Practical cables in the 80-100 Ohm range would suggest a nominal resistance around 90 Ohms. This would cause compatibility problems with earlier SCSI implementations primarily in the area of driver I_{ol} and max termpower. A reasonable compromise might be:

Termination Thevinin resistance 110 Ohms +/- 2%
Termination Thevinin voltage 2.85 +/-5%

These resistances and voltages are referenced to the termination ends of the cable. The use of the Thevinin definitions will allow for the following electrical equivalent (except for total termination power) implementations.

1) Pull up- pull down resistors to termpower or a local V_{dd} supply (providing resistor and voltage tolerance can be maintained). The suggested 187/267 to +5V/GND closely approximates the above Thevinin values.

2) Single 110 Ohm resistor to a regulated Thevinin source. This is essentially the Boulay terminator. It is important for the spec to require the regulated voltage to operate at least in some part of the 2nd quadrant where it must sink current. This is necessary to accommodate active negations schemes while maintaining the termination voltage regulation. This could be specified as a function of number of lines terminated. For example a sink capability of 9ma/termination would maintain Voltage regulation up to an active negation level of 3.85V.

3) Termination schemes using clamping diodes to V_{term} and Gnd to reduce ringing.

The use of Other non-linear terminations schemes while improving signal fidelity at the line ends do little to improve the amplitude and noise margin of the initial assertive wave. Even with the 110 Ohms to 2.85 Volts the line current is insufficient to transmit a

full 2.5v pulse on lines of less than 94 Ohms. The following simple calculation shows this:

Assume: V_{term} = 2.85, R_{term}=110 Ohms, V_{ol}=.5v

Calc $I_{driver\ quiescent}$ = 2x(2.85-.5)/110)=42.7 ma

If initial wave = 2.5 V = $V_{ol}+I_{driver\ quiescent} * Z_{line}/2$

Z_{line} = 2*(2.5-.5)/.0427 = 94 Ohms

The spec should recommend adequate high and low frequency bypassing of the terminator. This should include distributed high frequency chip or disc capacitors (typically .01 to .1uf) close to the resistor's "cold" end along with 1-10uf bypassing at the voltage source. Where terminations are not made to a low impedance ground plane it is imperative to treat the routing and connections of the return line with the same "respect" given to the active line.

EDGE RATE CONTROL:

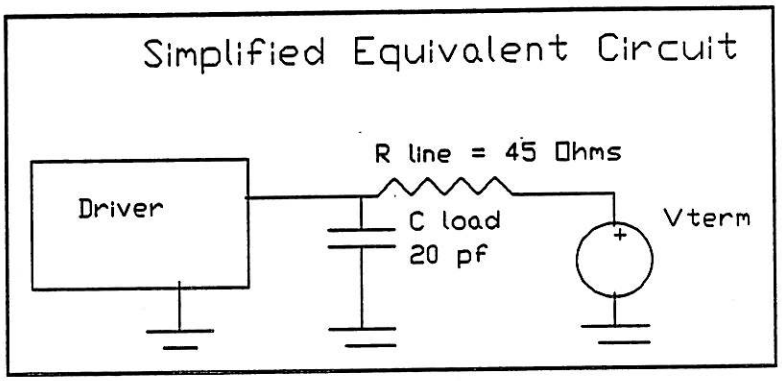
The high edge rates possible with modern IC technology coupled with the relatively large currents used in the bus contribute to crosstalk and ground bounce which can substantially degrade noise margins. This is particularly true when single interface chips are required to drive 8 or 16 bit data busses along with control signals.

By controlling the edge rates through appropriate design techniques noise margin can be improved. This was the concept and major reason for success for the MECL 10K logic family.

Although edge rate specs are usually described in terms of volts/nanosecond (which can be easily observed and measured) equally important is the current edge rate limit, di/dt max. Excessive di/dt operating through bonding, package and PC inductance causes ground and Vdd bounce which further degrade system noise margin. Measuring edge current rates can be difficult since introducing the measurement probe can easily modify the circuit inductance and corrupt the measurement. SPICE simulations allow one way of predicting edge currents when the driver environment is modeled correctly to include parasitic inductance and capacitance. There are a number of well known implementation techniques to control driver turn on turn off characteristics.

Since the SCSI driver looks into a transmission line, a simplified resistive equivalent can be used as "test circuit" for measuring or simulating edge currents and voltages. An appropriate model would

be a resistor value equal to half the nominal cable impedance (not necessarily half the value of the termination resistor!) to a voltage source equal to the quiescent termination voltage. A parasitic capacitance of say 20pf can be added to Gnd to accommodate practical considerations such as connectors or scope probe capacitance. This works up to the equivalent circuit shown in Fig 1.



Of course the other parasitic parts of the driver circuit (lead and package inductance, via and bond wire resistance, distributed drain and pad capacitance etc) will have to be included for accurate SPICE modeling. Based a circuit similar to the above the driver should be specified for the following parameters:

		Min	Max
Driver assertion:	Voltage edge rate;	-.25V/ns	-.5V/ns
	Current di/dt: (+ in to driver)		15ma/ns
Driver Negation: (Including active negation)	Voltage edge rate:	+.25V/ns	+.5V/ns
	Current di/dt		-15ma/ns

Note: The above numbers are preliminary and should be confirmed by analysis and simulation of drivers using the above test circuit.

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SINGLE ENDED OUTPUT CHARACTERISTICS (including active negation)

There is a basic discrepancy in the V_{ol} @ I_{ol} spec and the nominal line impedance and quiescent line voltage.

The spec calls for a V_{ol} of 0 to .5 v @ I_{ol}=+48ma (sinking). This is approximately what the *steady state* (DC) assertive current is with the 110 Ohm terminators to 2.85V.

If we assume a nominal line impedance of say, 90 Ohms, and a quiescent (de-asserted) voltage of 2.85V the *initial* assertion current for a driver would be:

$$I_{assertion} = 2*(V_{line}-V_{ol})/Z_{line}$$

$$I_{assertion} = 2*(2.85-.5)/90=52 \text{ ma}$$

For lower line impedances, lower V_{ol}, or higher V_{term} the current will be higher. Note that the initial assertive current is *independent* of the terminating resistor. This current will be maintained until the reflected wave is received back at the driver (up to 2*Line length depending upon driver location).

The end result is that if a driver were marginal (barely met the DC spec) the initial assertive wave could be higher than the desired .5 volts and noise margin would be reduced. In practice, few devices are near the spec due to necessary over-design so the initial wave is close to or below .5V. The SCSI spec should reference this point (at least as an implementors note) if for no other reason than to provide information to chip designers to allow adequate design margin. The worst case assertive current would be at minimum cable impedance and max quiescent termination voltage.

For a +5% high termination voltage and a 60 Ohm cable:

$$I_{assertion\ max} = 2*((1.05*2.85)-.5)/60 = 83\text{ma}$$

The driver should be able to handle this transient assertion current at a V_{ol} of no more than .5v to maintain adequate active low noise margin. The normal transient nature of this current and typical low duty cycle will diminish the negative effect of electro migration but this effect should be considered for reliability reasons. The main point here is to insure not only driver transistors but interconnection, bonding and package inductance are designed to handle these peak transient current without excessive voltage "bumps" to V_{dd} or V_{ss}.

ACTIVE DE-ASSERTION

One of the techniques sometimes used to reduce some of the effects of mismatch is the use of active high drive to assist the passive pullup of the terminator (and charged line). In practice since the current in a typical line is below the level required to reach the final de-assertive level of 2.85v the additional current must be supplied from the driver. Some simple calculations determine the required current to boost the de-assertive level:

Assumptions: Initial quiescent termination voltage 2.85
Termination resistance 110 Ohms
Line impedance 90 Ohms

Assertive current @ .5V, V_{ol};

$I_{assertive\_steady\_state}$ = 2*(2.85-.5)/110=44ma

Initial De-asserted level= .5+(.044*90/2)=2.48V

Additional current required from driver to reach 2.85V;
I_{driver}= 2*(2.85-2.48)/90= 8.2ma (source)

The driver would be required to source this current at an output V_{oh} of 2.85v.

The difficulty with a specification of this type is in the practicality of accurately limiting either the driver on current or the driver pull-up voltage. If too much additional current is injected into the line there will be excessive reflection (unless termination clamp diodes are provided) from the under-terminated line. In severe cases (where the terminator is accidentally left off) the reflected wave could exceed local V_{dd} and possibly trigger latchup. The final difficulty is in the specification and limiting of the maximum amount of time the driver active current sourcing should continue. This time is a function of the electrical length of the cable and the location of the driver both variants of topology.

A reasonable alternative specification would be to spec an upper current limit as a function of V_{oh}. Correctly specified, drivers not using active de-assertion would comply with the spec (although with reduce noise margin).

SINGLE ENDED INPUT CHARACTERISTICS (Section 6.1.2)

One area that can offer some significant improvement while not compromising much compatibility is in tightening the receiver specification in the area of V_{ih}, V_{il} and hysteresis. The current spec allows the input threshold of anywhere from .8 to 2.0 volts with a minimum hysteresis of 200mv. By tightening the input threshold range to say 1.0 to 1.8v and requiring minimum hysteresis of 300 to 400 mv a significant improvement in noise margin is insured. This is probably closer to what actual receivers are achieving and is possible with modern CMOS design techniques.

SPECIFIC RECOMMENDATIONS FOR CONSIDERATION

5.2 Cable Requirements

Include or reference a technique for measuring both single ended and differential cable impedance, loss factor and DC resistance.

Limit the range (at least as a requirement for fast synchronous transmission) of acceptable single ended impedance of 80-100 Ohms.

Specify the DC resistance in mOhms/ meter, wire gauge, or equivalent cross section.

Specify the high frequency loss characteristics as db/ meter @ a specific frequency.

Considering limiting the max cable length to 3 meters when using the high speed synchronous mode with single ended cable.

6.1 Single-Ended alternatives

Modify the terminator specification to read:

The bus shall be terminated at each end with a Thevinin equivalent resistance of 110 Ohms +/-2% and a Thevinin equivalent voltage of 2.85v +/-5%. The Thevinin equivalent voltage source must be able to source 25ma and sink 9ma for each terminator.

Diode clamps to prevent ringing are permitted provide they do not conduct more than .5ma over the range .5 to 2.5 v.

All terminators should be well bypassed with high frequency (low inductance) capacitors of .01 to .1 uf close to the "cold" end of the termination resistor. The Termination power or equivalent Thevinin voltage should receive additional bypassing of 1 to 10 uf.

6.1.1 Single-Ended Output Characteristics

Expand the V_{ol}, V_{oh} driver specification to include:

Vol D.C. 0 to .5v @ I_{ol} = 48ma (sink) signal assertion.

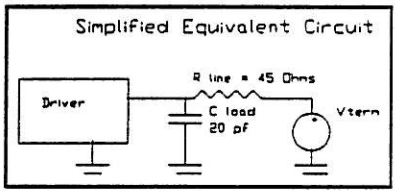
Add to spec or include as implementors note:
Drivers are subject to elevated transient sink currents when operating in systems with cable impedances <94 Ohms.

V_{ol} Transient, 0 to .5V @ Ioltransient = 80 ma sink for up to 40ns after initial edge assertion.

V_{oh} D.C. All devices shall operate over am Output voltage range of 0 to 5.25V. I_{oh} shall be kept less than 8ma (source) over the range 0 to 2.85V and less than 2ma from 2.85 to 5.25v. Open collector or open drain devices will meet this specification.

Devices using active negation (sourcing I_{oh}) should have provisions for reducing the I_{oh} to <+/-50ua after the data transfer is completed.

Driver voltage slew rates shall be maintained in the range +/-.25 to .5 V/ns when connected to the following equivalent test circuit.



6.1.2 Single-Ended Input Characteristics

Modify the spec to read:

V_{il-} (low going threshold voltage) = 1.0V minimum
V_{ih+} (high going threshold voltage) =1.8V maximum
Input hysteresis (V_{ih+} - V_{il-}) = 300mv minimum
I_{il} (Low-level input current) V_{il}= .5V; -.4 to 0.0 ma
I_{ih} (High level input current) V_{ih}= 2.7V; 0.0 to .1ma
Maximum input capacitance; 35 pf measured at the device connector, driver disabled, power on.