SCSI active deassertion

1. The problem:

The active deassertion driver, by forcing a minimum voltage step on a poorly terminated bus, may generate reflected waves of significant amplitude. The problem may occur when a SCSI bus is terminated with a resistance significantly higher than the bus characteristic impedance. In such a situation, the rising edge generated by the active deassertion, upon reaching the end of the bus, will return as a higher amplitude reflection. In case of an open bus the reflected voltage may reach twice the amplitude of the initial active deassertion edge .

In a simplistic worst case analysis a maximum active deassertion signal of 5 V DC will return as a reflected wave of 10 V if the bus is left unterminated. If the maximum amplitude of the returning wave is not controlled it may create reliability problems for the receivers connected to the bus. The failure mode of primary concern in overvoltage breakdown. It is not uncommon for a 5V CMOS digital process used today in implementing SCSI controllers to have an oxide minimum breakdown voltage of 10V.

In a consumer product environment it is quite common to encounter an unterminated bus or a misplaced terminator which leaves a segment of the bus practically unterminated. While an unterminated SCSI bus does not need to be functional, such a configuration should not have any negative impact upon the life span of the components connected to the bus. The new SCSI controllers can be designed to withstand such signals but, given the large number of SCSI devices already in use, it is quite difficult to predict the reliability impact of high voltage reflection upon previous manufactured controllers.

The goal of this paper it to define an acceptable area of operation in the I-V plane for an active deassertion driver such as to limit the maximum amplitude of the reflected wave while maintaining a sufficiently high initial deassertion step.

2. The assumptions:

The validity of the following assumptions can be the subject of lengthy debates. I selected them only as reference points for the analysis presented at point 3.

2.1. For both present and future SCSI drivers it is safe to assume that an input voltage of 6V DC maximum can be safely tolerated without significant long term reliability implications.

2.2. The minimum characteristic impedance of a SCSI cable that shall be reasonably accommodated for back compatibility reasons is 60 Ω.

2.3. The maximum characteristic impedance of a SCSI cable that shall be reasonably accommodated for back compatibility reasons is 125Ω.

2.4. The bus shall tolerate the absence of terminations with no reliability impact.

2.5. The bus shall operate within the specified voltage levels with a passive 220Ω / 330Ω ±5% terminator and a minimum TERMPWR voltage of 3.6 V. This represents the worst case terminator that will maintain the DC voltage on a deasserted bus above the specified 2.0 V limit.

2.6. The minimum acceptable initial deassertion step is 2.4 V.

3. The solutions:

The next three paragraphs will attempt to analyze three distinct models for an active deassertion driver. They are clearly only simplified theoretical models but they can be used to define a domain of validity in the I-V plane for a real implementation of an active deassertion driver as discussed at 3.4.

3.1. Ideal voltage source active deassertion driver:

This model assumes an ideal voltage source (zero output impedance) V_h followed by an ideal switch SW_h. This configuration is described in Figure 1, page 2. The equivalent lumped element circuit at the point of deassertion, at the beginning of deassertion, is shown in Figure 2, page 3.

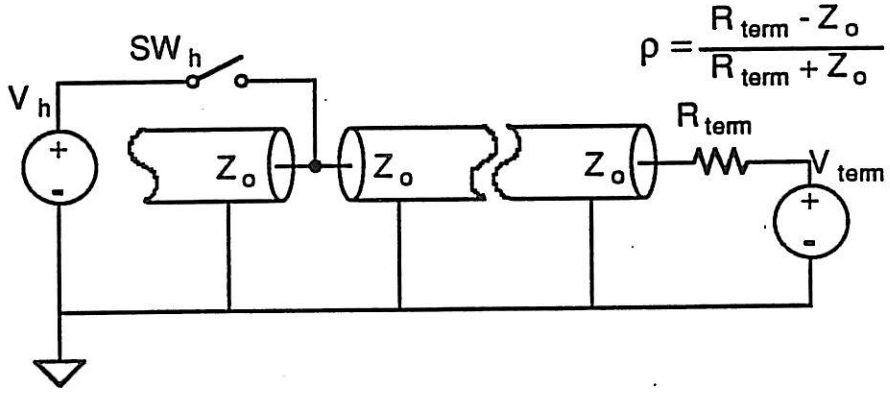

Figure 1

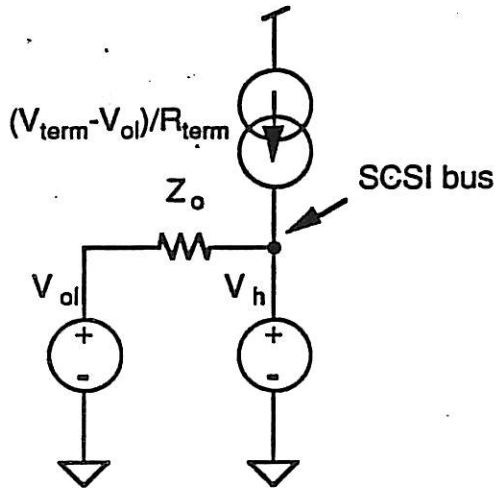

Figure 2

The amplitude of the reflected wave is given by:

$$V_r = (V_h - V_{ol}) * (1 + \rho) + V_{ol}$$

where:

V_r = amplitude of the reflected wave.

V_h = voltage clamp value for the active deassertion driver.

V_{ol} = voltage on the bus prior to deassertion.

ρ = bus termination reflection coefficient.

The worst case conditions for maximum V_r are: $\rho = 1$ and $V_{ol} = 0$ thus $V_r = 2 * V_h$.

Under the assumption $V_r \leq 6$ V it results $V_h \leq 3$ V.

In order to provide an initial voltage level of at least 2.4 V it is necessary to impose the condition: $V_h \geq 2.4$ V.

The V_h range for this model is: $2.4\text{ V} \leq V_h \leq 3.0\text{ V}$.

3.2. Ideal current source active deassertion driver:

This model considers an ideal current source (infinite output impedance) I_h followed by an ideal switch SW_h as shown in Figure 3, page 4. The equivalent lumped element circuit at the

point of deassertion, at the beginning of deassertion, is shown in Figure 4, page 4.

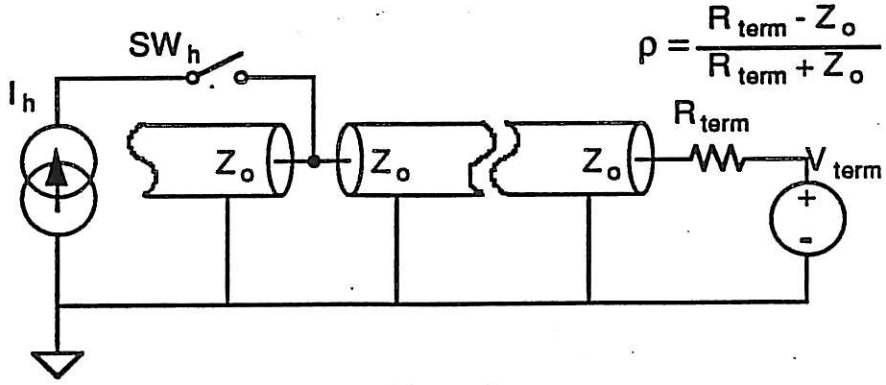

Figure 3

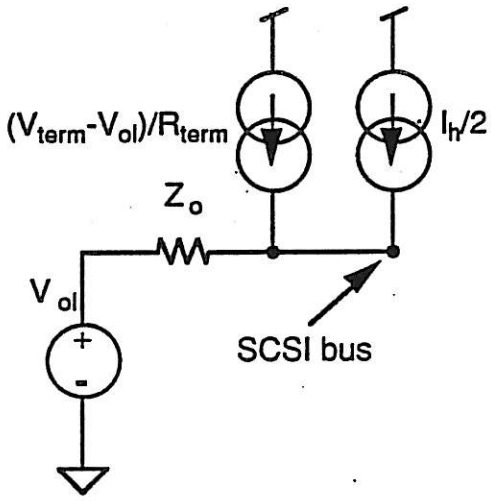

Figure 4

The amplitude of the reflected wave is given by:

$$V_r = \left(\frac{V_{term} - V_{ol}}{R_{term}} + \frac{I_h}{2} \right) * Z_o * (1 + \rho) + V_{ol}$$

or

$$V_r = 2 * \left(\frac{V_{term}}{R_{term}} + \frac{I_h}{2} \right) * \frac{Z_o * R_{term}}{Z_o + R_{term}} + V_{ol} * \left(1 - \frac{2 * Z_o}{Z_o + R_{term}} \right)$$

and the amplitude of the initial voltage level on the bus immediately following the deassertion is given by:

$$V_{oh} = \left(\frac{V_{term} - V_{ol}}{R_{term}} + \frac{I_h}{2} \right) * Z_o + V_{ol}$$

where:

V_r = amplitude of the reflected wave.
I_h = constant current value for the active deassertion driver.
Z_o = bus characteristic impedance.
V_{ol} = voltage on the bus prior to deassertion.
ρ = bus termination reflection coefficient.
V_{oh} = voltage on the bus immediately following the active deassertion.
V_{term} = Thevenin equivalent terminator voltage.
R_{term} = Thevenin equivalent terminator resistance.

While not immediately obvious, it can be shown that, from the point of view of a maximum V_r, the worst case conditions are: $V_{ol} = 0.5$ V, $Z_o = 125\ \Omega$ and a worst case terminator of 220 Ω - 5% / 330 Ω + 5% and $V_{TERMPWR} = 5.25$ V thus: $V_r = I_h * 63.81 + 3.21$.

Under the assumption $V_r \leq 6$ V it results $I_h \leq 32$ mA.

For minimum V_{oh} the worst case conditions are: $V_{ol} = 0$, $Z_o = 60\ \Omega$ and a worst case terminator of 220 Ω + 5% / 330 Ω - 5% and $V_{TERMPWR} = 3.60$ V thus: $V_{oh} = I_h * 30 + 0.94$.

Under the assumption $V_{oh} \geq 2.4$ V it results $I_h \geq 36$ mA.

The obvious conclusion of this analysis is that, under the assumptions defined at point 2 a ideal current source can not be used for active deassertion .

3.3. Finite output resistance voltage source active deassertion driver:

This model assumes a voltage source V_h with a finite constant output resistance R_h and an ideal switch SW_h as shown in Figure 5, page 6. The equivalent lumped element circuit at the point of deassertion, at the beginning of deassertion, is shown in Figure 6 page 6.

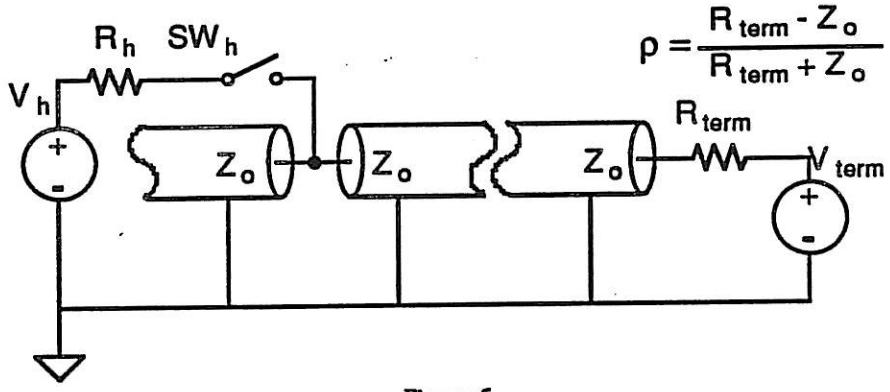

Figure 5

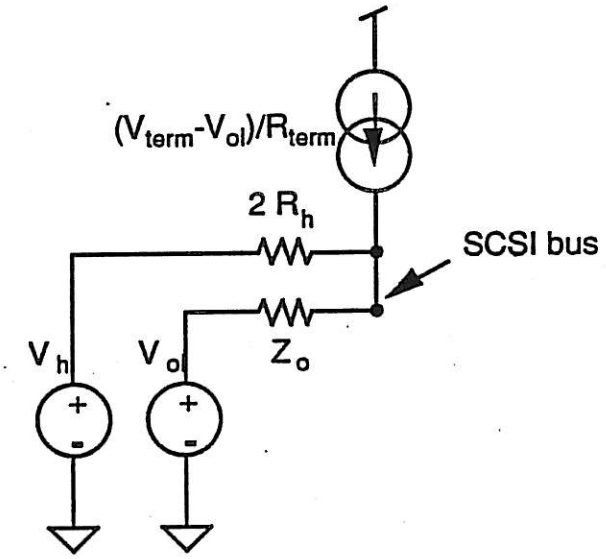

Figure 6

The amplitude of the reflected wave is given by:

$$V_r = \left(\frac{V_h - V_{ol}}{2 * R_h} + \frac{V_{term} - V_{ol}}{R_{term}} \right) * \frac{2 * R_h * Z_o}{2 * R_h + Z_o} * (1 + \rho) + V_{ol}$$

or

$$V_r = 2 * \left(\frac{V_h}{2 * R_h} + \frac{V_{term}}{R_{term}} \right) * \frac{R_{term}}{R_{term} + Z_o} * \frac{2 * R_h * Z_o}{2 * R_h + Z_o}$$

$$+ V_{ol} * \left(1 - \frac{R_{term} + 2 * R_h}{R_{term} + Z_o} * \frac{2 * Z_o}{2 * R_h + Z_o} \right)$$

and the amplitude of the initial voltage level on the bus immediately following the deassertion is given by:

$$V_{oh} = \left(\frac{V_h - V_{ol}}{2 * R_h} + \frac{V_{term} - V_{ol}}{R_{term}} \right) * \frac{2 * R_h * Z_o}{2 * R_h + Z_o} + V_{ol}$$

or

$$V_{oh} = \left(\frac{V_h}{2 * R_h} + \frac{V_{term}}{R_{term}} \right) * \frac{2 * R_h * Z_o}{2 * R_h + Z_o}$$

$$+ V_{ol} * \left(1 - \frac{2 * R_h + R_{term}}{2 * R_h + Z_o} * \frac{Z_o}{R_{term}} \right)$$

where:

V_r = amplitude of the reflected wave.
V_h = voltage value for the active deassertion driver.
R_h = output impedance value for the active deassertion driver.
Z_o = bus characteristic impedance.
V_{ol} = voltage on the bus prior to deassertion.
ρ = bus termination reflection coefficient.
V_{oh} = voltage on the bus immediately following the active deassertion.
V_{term} = Thevenin equivalent terminator voltage.
R_{term} = Thevenin equivalent terminator resistance.

Within our problem domain, it can be shown that, from the point of view of a maximum V_r, the worst case conditions are: $V_{ol} = 0$, $Z_o = 125\,\Omega$ and $\rho = 1$ ($R_{term} = \infty$) thus:
$V_r = V_r = V_h / (0.5 + R_h / 250)$.

Under the assumption $V_r \leq 6$ V it results $R_h \geq 41.66 * (V_h - 3)\ \Omega$.

For minimum V_{oh} the worst case conditions are: $V_{ol} = 0$, $Z_o = 60\,\Omega$ and a worst case terminator of $220\,\Omega + 5\% / 330\,\Omega - 5\%$ and $V_{TERMPWR} = 3.60$ V thus:
$V_{oh} = V_r = 30\,V_h / (30 + R_h) + 0.94\,R_h / (30 + R_h)$

Under the assumption $V_{oh} \geq 2.4$ V it results $R_h \leq 20.55*(V_h-2.40)\ \Omega$

The R_h range for this model is:

$$41.66 * (V_h - 3)\ \Omega. \leq R_h \leq 20.55*(V_h-2.40)\ \Omega$$

The maximum voltage V_h for which the above relation still has a solution is 3.58 V and corresponds to a resistor $R_h = 24\ \Omega$.

3.4. Output impedance domain for an active deassertion driver.

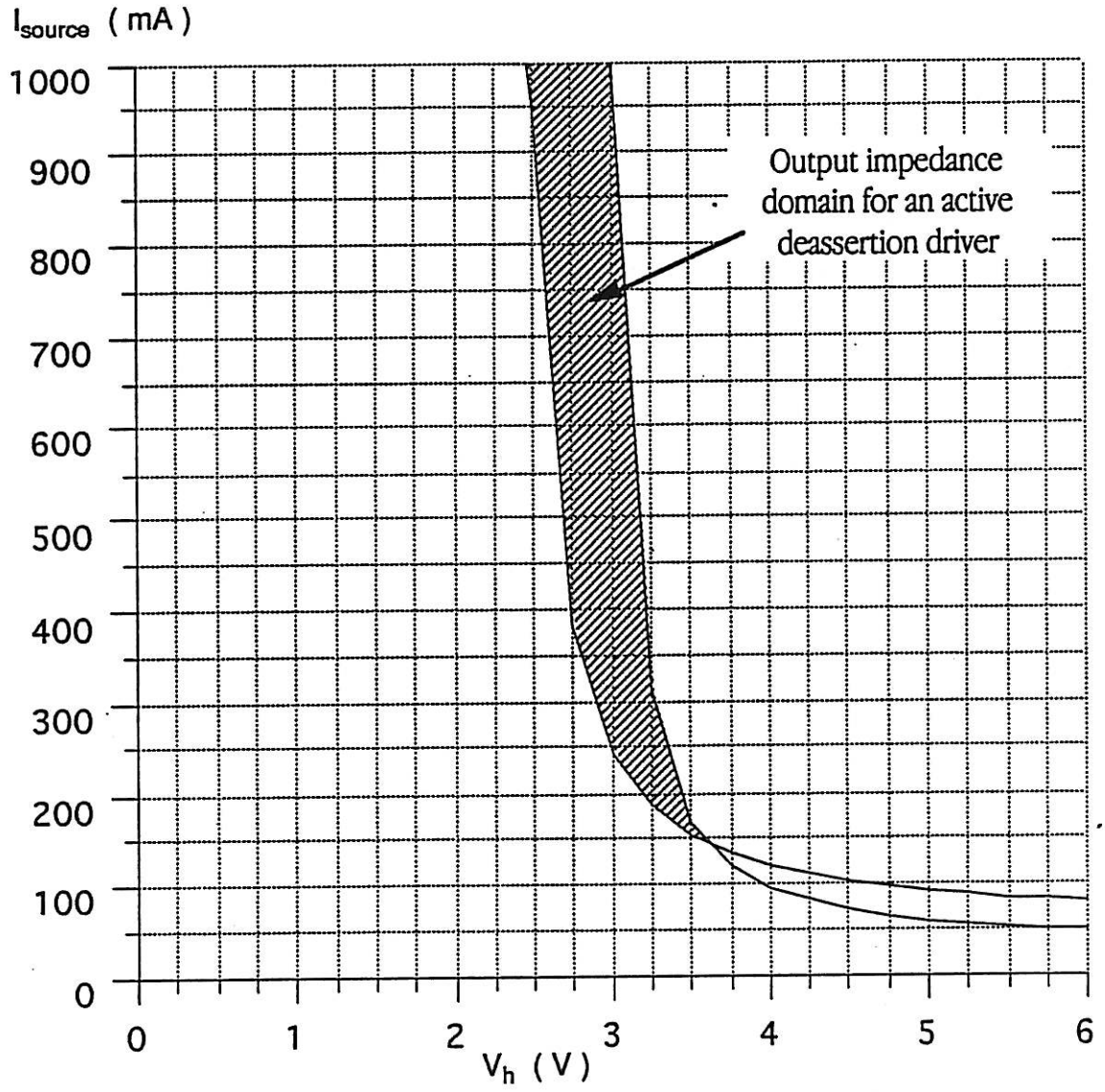

Figure 7

By combining the results derived in the previous three sections the range of acceptable output impedances for an active deassertion driver can be plotted in the I-V plane as shown in Figure 7, page 8.

From this analysis it can be concluded that the active deassertion driver should be implemented as a voltage driver with a limited maximum output range. As an example the output voltage of a driver with a 10 Ω output impedance should be limited between 2.88 V and 3.24 V.

In order to maximize the tolerance of the output voltage range the output impedance of the driver should be minimum.