MEMORY CARD OVERVIEW

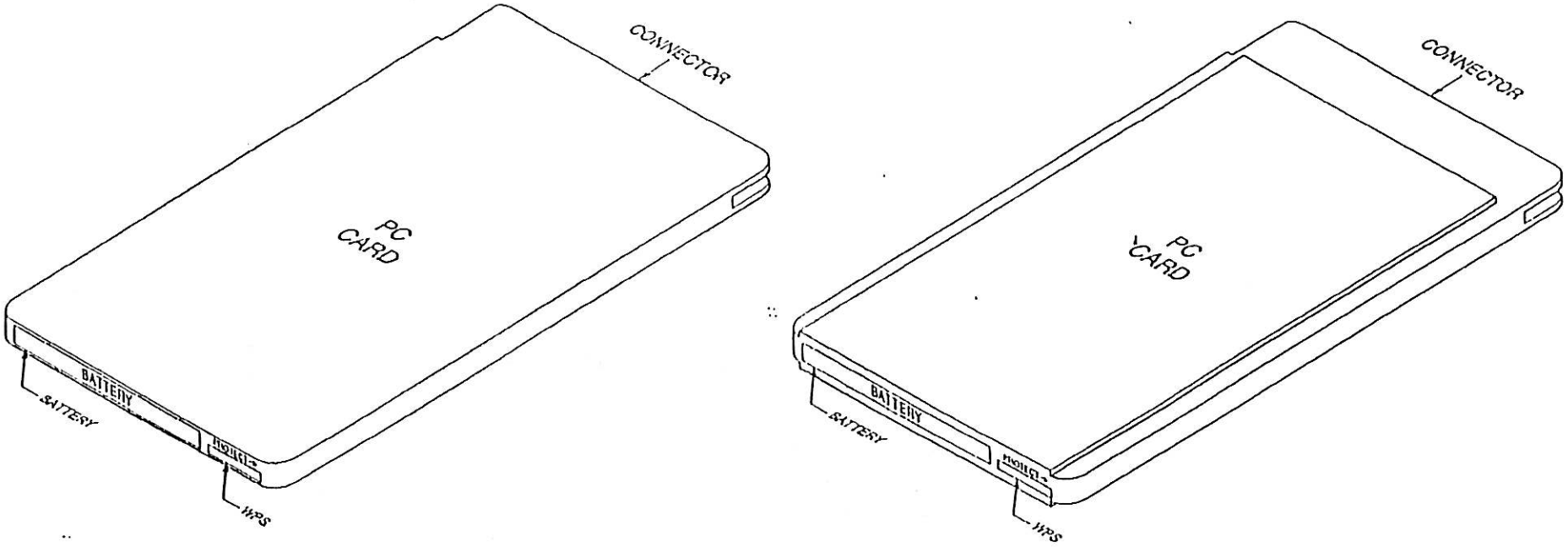
STAN SHARP
FOXCONN INTERNATIONAL
X3T9 10/14-15

$h \geq 17$

PC Card Definition

A PC card is a removable storage media, containing one or more integrated circuits. Currently most PC cards contain memory ICs. In the future, we expect PC cards to provide other types of functionality.

Comparison Type I & Type II PC Card



	Length ±.008	Width ±.004	Interconnect Area ±.002	Substrate Area ±.002
TYPE I	3.370 (85.6)	2.126 (54.0)	.065 (1.65)	.065 (1.65)
TYPE II	3.370 (85.6)	2.126 (54.0)	.065 (1.65)	.098 (2.5) MAX

PCMCIA Background

- Founded in 1989
- Initial Focus on Standardized Solid-State Storage Card
- Market-Driven Philosophy
- Broad Membership
- PCMCIA 1.0 Released 1990
- PCMCIA 2.0 Goes Beyond Data Storage

LS7

Today's Mobile Computer User Critical Buying Factors

- Physical Size
- Weight
- Battery Run-Time
- Display Quality
- Application Compatibility
- Keyboard
- CPU Performance
- Communications Capability
- Cost

Source: Venture Development Corporation

PC Card

857

Next Generation PC Card Products

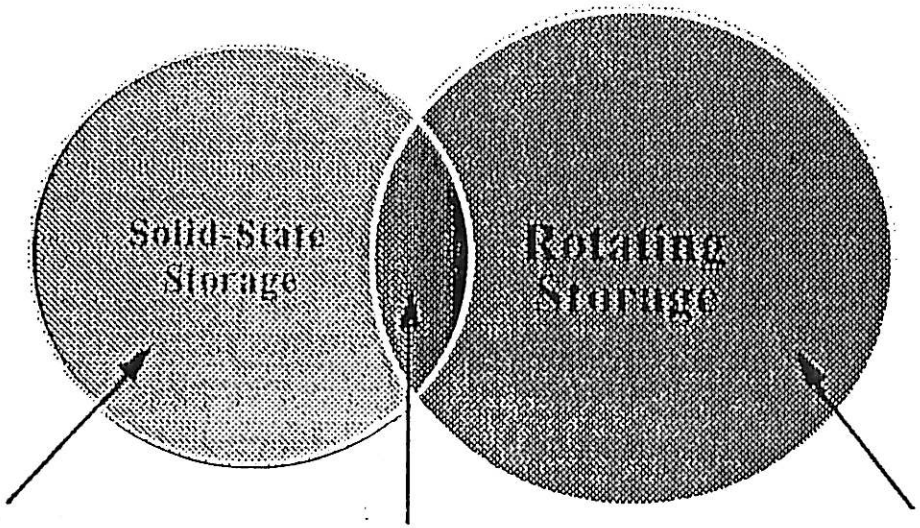
- **Sub-Notebook**
  - Size
  - Low Power
  - OS Compatibility
  - Ruggedness
  - Weight
  - High Capacity Removable Media
- **Application Specific Computers**
  - Size
  - Weight
  - Low Power

Next Generation PC Card Products

- **Pen-Based Products**
  - Ruggedness
  - High Capacity Removable Media
  - Low Power Consumption
  - Size
  - Weight
- **Palmtop Computers**
  - Size
  - Low Power
  - High Capacity Removable Media
  - Weight
  - Ruggedness

PC Card

Solid-State Storage will coexist with Rotating Storage



- Future Pen Products
- Palmtops
- Sub-Notebooks

- First Generation Pen Products
- Today's Notebooks

- High Performance Notebooks
- Laptops

PC Card

Opportunities Created By PC Cards - Hardware Companies

- Unprecedented Mobility
- New classes of Mobile Computer Enabled
  - Palmtop, Pen-Based, Sub-Notebook
  - Imaging Systems
  - Application Specific

Opportunities Created By PC Cards - Hardware Companies (Continued)

- Supporting Hardware
  - Reader/Writers
  - Programmers
  - Test Equipment
  - Data loggers

Opportunities Created By PC Cards - Software Companies

- New Class of Applications for Mobile Users
- Early Market Entry Critical to Secure Market Position

PC Card

Opportunities Created By PC Cards - End Users

- The Functionality of Next Generation Mobile Computers Combined with New Applications, Will give their Users a Competitive Advantage

S94

Mobile Market - Fastest Growing

- 1 Out of 3 Computers Shipped in 1995 Will Be Mobile

Source: Forrester Research

PC Card

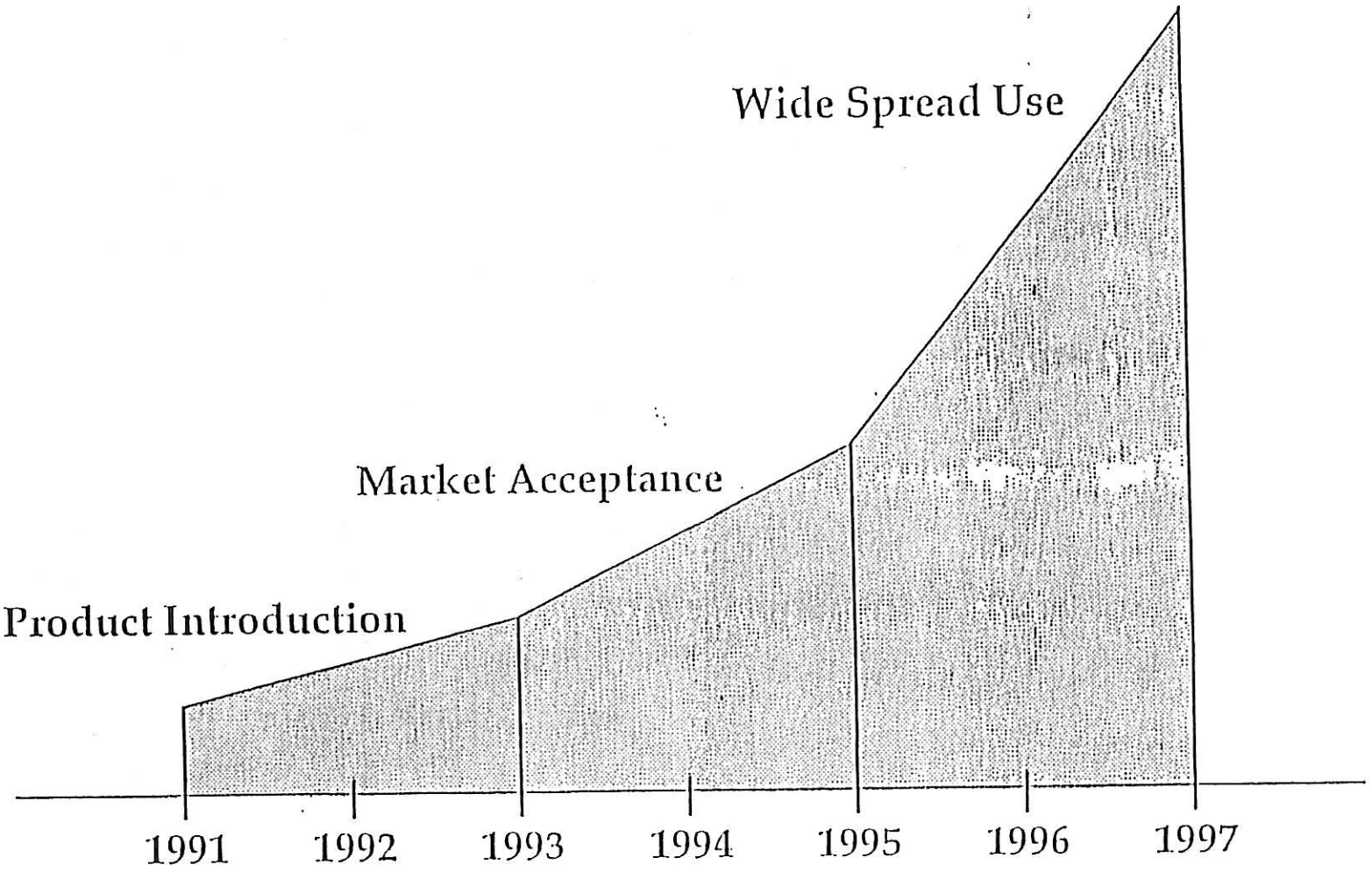
Higher Capacity Hard Drives / Lower Cost Memory

- Industry is moving to higher capacity and smaller size hard drives
  - Requires advanced media, head, motor, and positioning technology
  - Approach increases the base cost of a drive, regardless of capacity
  - Small drives are more costly on a per-byte basis than large drives
  - Minimum capacity of small drives continues to move up
- Industry is moving to higher capacity and lower cost memory chips
  - Rely on batteries for power
  - Battery life is a major issue
  - Smaller is better
- By 1995 silicon drives will be price competitive with the smaller hard drives

Flash Memory Technology

- Offers three advantages over SRAM
  - Does not lose its contents when power is removed (no batter required)
  - Requires less power
  - Costs significantly less
- Projected to be less expensive (on a per-byte bases) than a small hard disk.
- PC memory cards currently outperform floppy and small hard drives in all but one area — price
- Flash memory will be instrumental in making PC memory cards price competitive

Market Trend



Standards Committ

Future Tasks

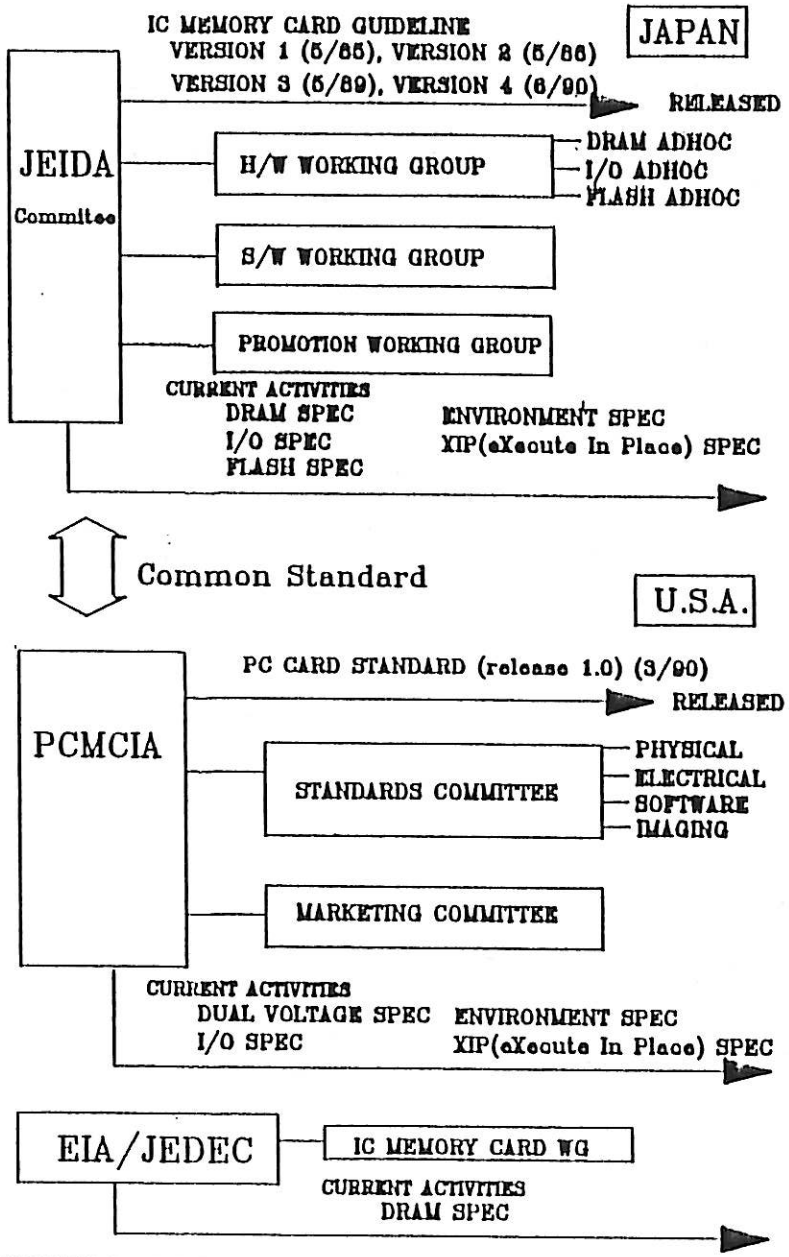
Release 2.0 Released 9/16/91

- Environmental guidelines
- I/O card specifications
- Dual operating voltage specifications 5.0v + 3.3v
- eXecute In Place (XIP) specifications

Potential for Future Releases

- Establish programmable device programming algorithms
- PSEUDO Static card definitions
- Establish file system for block erase devices (Flash EPROM)
- Establish application program interface for XIP
- Establish Image Card guidelines

A WORLD WIDE STANDARD



The PCMCIA Standard

- The standard has been developed by a group of highly motivated people, with a vested interest in the industry.
  - Computer manufacturers
  - Memory card manufacturers
  - Software vendors
  - Suppliers of memory card-specific hardware

- The current standard is optimized for the DOS PC environment.
  - DOS based PC's represent a large market
  - Media interchangeability is a key factor in the acceptance of DOS PCs
  - Cards used with "non-DOS" platforms eventually wind up in DOS PCs

- The standard is especially important to the fastest growing market segment — portable computers.

Promotion of the Standard

- To be successful, a standard must be actively promoted
- PCMCIA's marketing committee serves this function
- Promotion activities include:
  - Technical briefings / Educational seminars
  - Articles / Press releases
  - PCMCIA newsletter
  - Membership recruiting
  - Globalizing standard

MEMORY CARD TYPES

60 PIN DRAM	SIMM REPLACEMENT
68 PIN PC CARD	HARD DRIVE & FLOPPY
88 PIN DRAM	SIMM REPLACEMENT

PC Card Densities

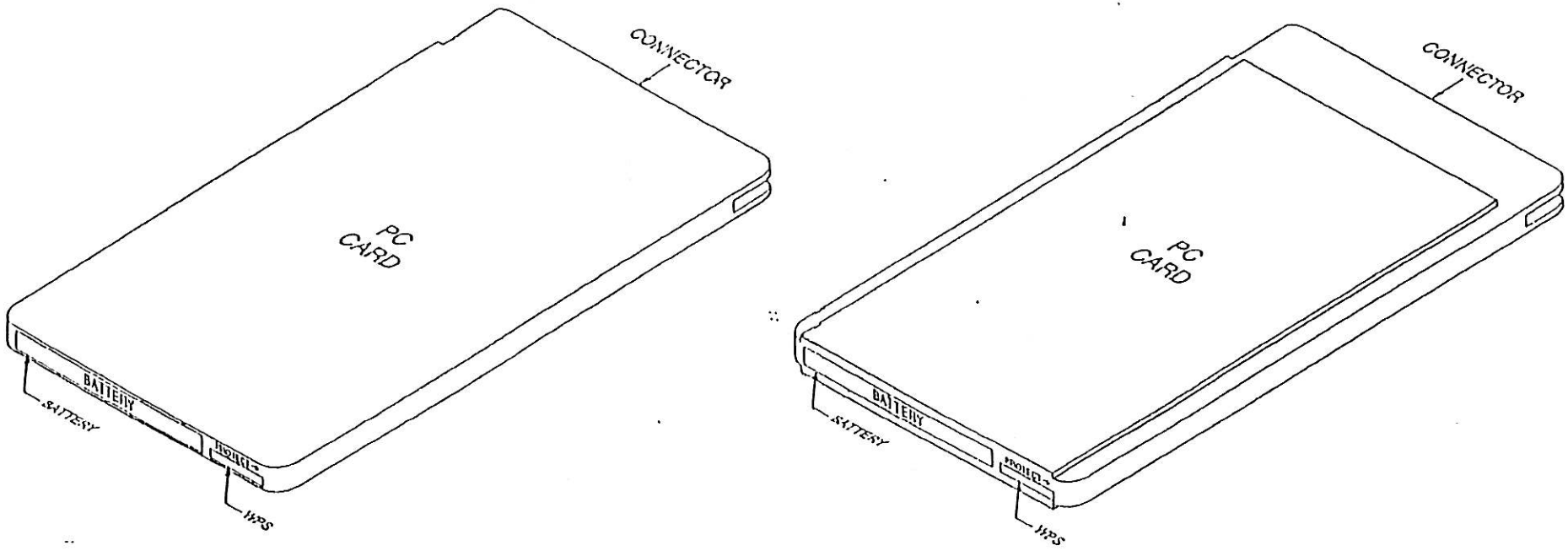
TYPE	Density Range (Approximate)
SRAM	32K - 2MB
ROM	32K - 16MB
FLASH	128K - 10MB
EPROM	32K - 2MB
OTP	32K - 2MB
(DRAM	2MB - 10MB)

PC Card Interface

- Sixty-eight position two-piece pin and socket connector
- Sixty-eight position allows up to 64 MB PC Card
- Socket connector on the PC Card
- Three pin lengths

Pin Type	Pin Length (L) ± .004 (0.1)	Pin Number
Detect	.138 (3.50)	36, 67
General	.167 (4.25)	All Other Pins
Power	.197 (5.00)	1,17,34,35,51,68

Comparison Type I & Type II PC Card



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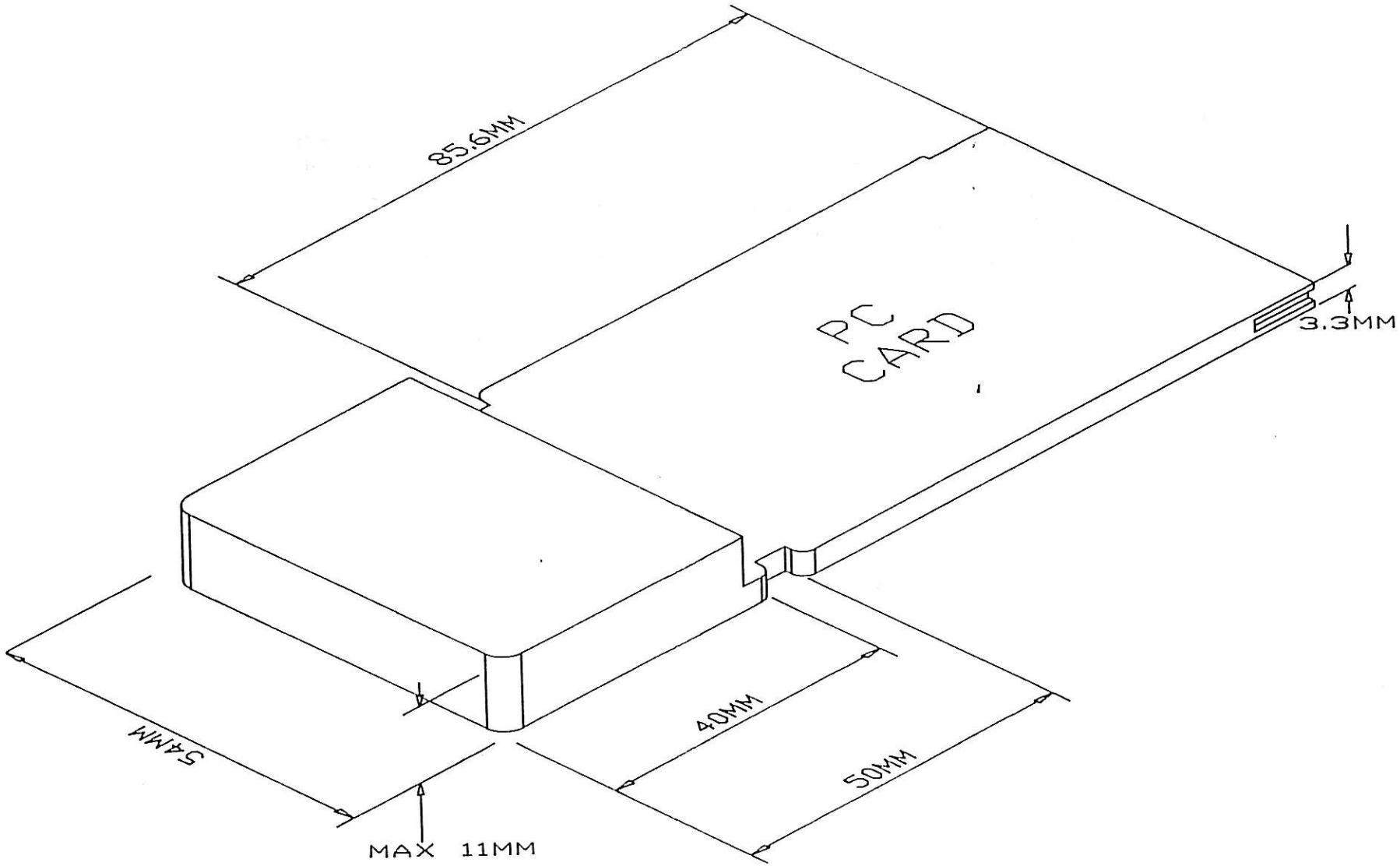
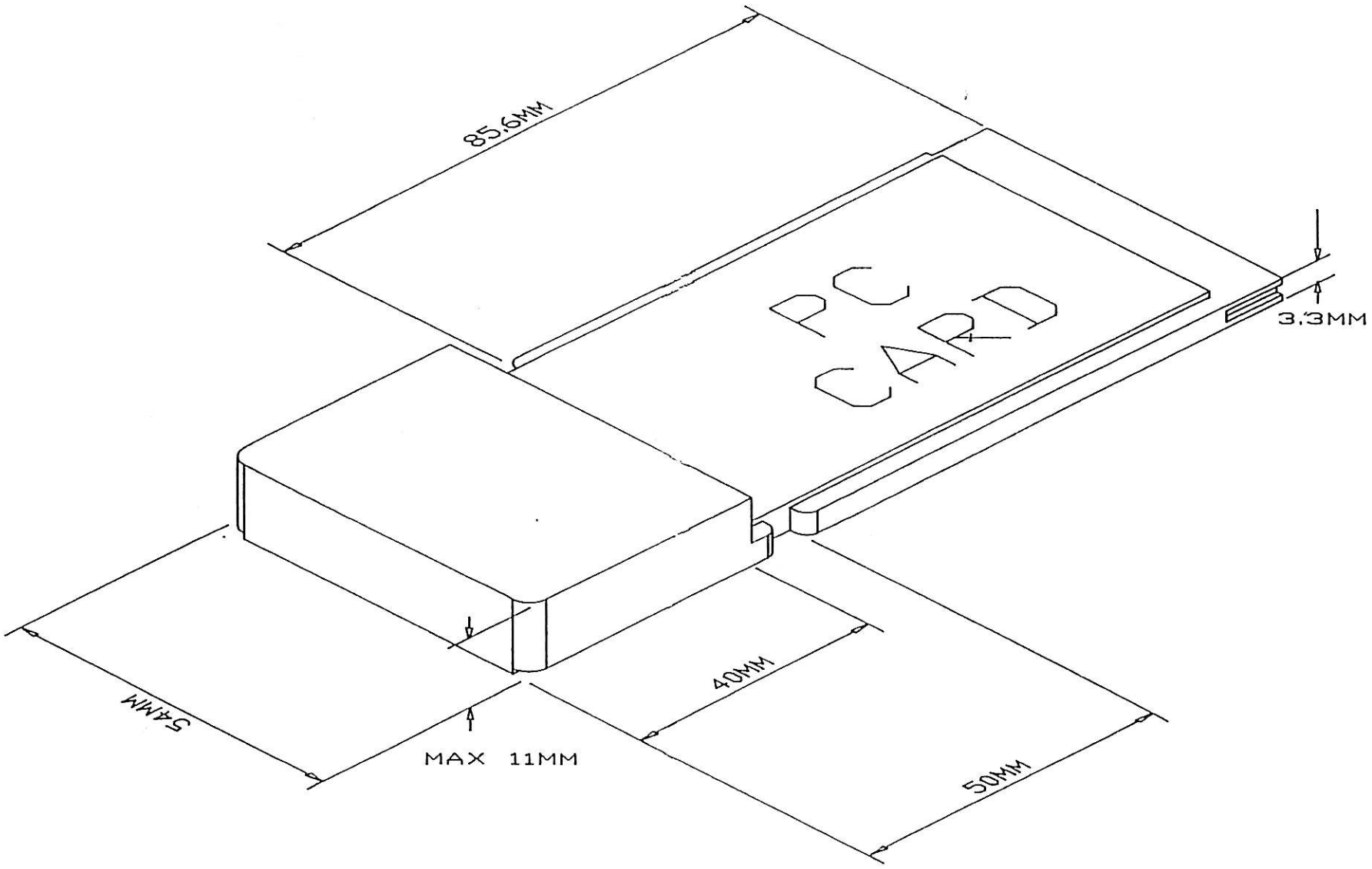
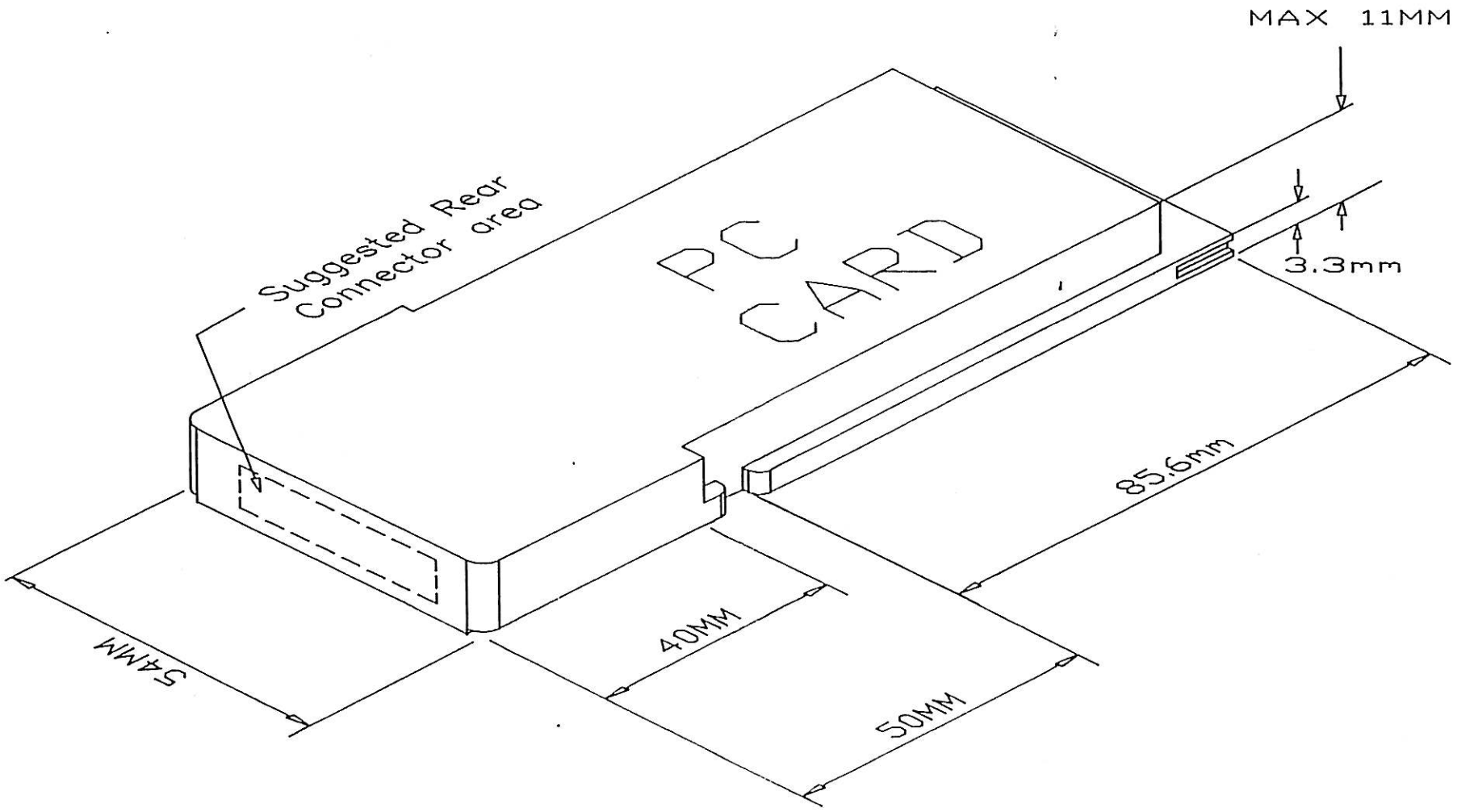


Proposed Type I Extended
PC CARD



Proposed Type II Extended
PC CARD



Proposed Type III Extended
PC CARD

4.1 Pin Assignments[1]

Table 4-1: PCMCIA PC Card Pin 1 To Pin 34 Assignments

Memory Only Card Interface: (Always available at card insertion[1])						I/O and Memory Card Interface: (Available only after card and socket are configured)				
Pin	Signal	I/O	Function	+/-	Notes	Pin	Signal	I/O	Function	+/-
1	GND		Ground			1	GND		Ground	
2	D3	I/O	Data bit 3			2	D3	I/O	Data bit 3	
3	D4	I/O	Data bit 4			3	D4	I/O	Data bit 4	
4	D5	I/O	Data bit 5			4	D5	I/O	Data bit 5	
5	D6	I/O	Data bit 6			5	D6	I/O	Data bit 6	
6	D7	I/O	Data bit 7			6	D7	I/O	Data bit 7	
7	CE1	I	Card enable	-	3	7	CE1	I	Card enable	-
8	A10	I	Address bit 10			8	A10	I	Address bit 10	
9	OE	I	Output enable	-		9	OE	I	Output enable	-
10	A11	I	Address bit 11			10	A11	I	Address bit 11	
11	A9	I	Address bit 9			11	A9	I	Address bit 9	
12	A8	I	Address bit 8			12	A8	I	Address bit 8	
13	A13	I	Address bit 13			13	A13	I	Address bit 13	
14	A14	I	Address bit 14			14	A14	I	Address bit 14	
15	WE/PGM	I	Write enable	-		15	WE/PGM	I	Write enable	-
16	RDY/BSY	O	Ready/busy	+/-	2, 4	16	IREQ	O	Interrupt Request	-
17	Vcc					17	Vcc			
18	Vpp1		Programming Supply Voltage 1		2, 3	18	Vpp1		Programming and Peripheral Supply	
19	A16	I	Address bit 16			19	A16	I	Address bit 16	
20	A15	I	Address bit 15			20	A15	I	Address bit 15	
21	A12	I	Address bit 12			21	A12	I	Address bit 12	
22	A7	I	Address bit 7			22	A7	I	Address bit 7	
23	A6	I	Address bit 6			23	A6	I	Address bit 6	
24	A5	I	Address bit 5			24	A5	I	Address bit 5	
25	A4	I	Address bit 4			25	A4	I	Address bit 4	
26	A3	I	Address bit 3			26	A3	I	Address bit 3	
27	A2	I	Address bit 2			27	A2	I	Address bit 2	
28	A1	I	Address bit 1			28	A1	I	Address bit 1	
29	A0	I	Address bit 0			29	A0	I	Address bit 0	
30	D0	I/O	Data bit 0			30	D0	I/O	Data bit 0	
31	D1	I/O	Data bit 1			31	D1	I/O	Data bit 1	
32	D2	I/O	Data bit 2			32	D2	I/O	Data bit 2	
33	WP	O	Write protect	-	2, 3	33	IOIS16	O	IO Port Is 16 bit	-
34	GND		Ground			34	GND		Ground	

NOTES: Active "low" signals are indicated by -(minus). Active "high" signals are indicated by +(plus).

1. Wait and Reset are RFU (no connect) in Release 1.0. Both must be implemented in the system for Release 2.0 compliance
2. Use of signal changes between memory only and I/O interface.
3. Signal must not be connected between cards.
4. Signal must not be connected between cards when I/O interface is supported.
5. Reset must not be connected between cards unless all cards are reset when any card has Vcc power removed.
6. In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.

1. The glossary in Appendix A defines many of the technical terms in this chapter.

Table 4-2: PCMCIA PC Card Pin 35 To Pin 68 Assignments

Memory Only Card Interface (Always available at card insertion)					Notes	I/O and Memory Card Interface (Available only after card and socket are configured)				
Pin	Signal	I/O	Function	+/-		Pin	Signal	I/O	Function	+/-
35	GND		Ground			35	GND		Ground	
36	CD1	O	Card detect	-	3	36	CD1	O	Card detect	-
37	D11	I/O	Data bit 11			37	D11	I/O	Data bit 11	
38	D12	I/O	Data bit 12			38	D12	I/O	Data bit 12	
39	D13	I/O	Data bit 13			39	D13	I/O	Data bit 13	
40	D14	I/O	Data bit 14			40	D14	I/O	Data bit 14	
41	D15	I/O	Data bit 15			41	D15	I/O	Data bit 15	
42	CE2	I	Card enable	-	3	42	CE2	I	Card enable	-
43	RFSH	I	Refresh			43	RFSH	I	Refresh	
44	RFU		Reserved		2	44	IORD	I	IO Read	-
45	RFU		Reserved		2	45	IOWR	I	IO Write	-
46	A17	I	Address bit 17			46	A17	I	Address bit 17	
47	A18	I	Address bit 18			47	A18	I	Address bit 18	
48	A19	I	Address bit 19			48	A19	I	Address bit 19	
49	A20	I	Address bit 20			49	A20	I	Address bit 20	
50	A21	I	Address bit 21			50	A21	I	Address bit 21	
51	Vcc					51	Vcc			
52	Vpp2		Programming Supply Voltage 2		2, 3	52	Vpp2		Programming and Peripheral Supply 2	
53	A22	I	Address bit 22			53	A22	I	Address bit 22	
54	A23	I	Address bit 23			54	A23	I	Address bit 23	
55	A24	I	Address bit 24			55	A24	I	Address bit 24	
56	A25	I	Address bit 25			56	A25	I	Address bit 25	
57	RFU		Reserved			57	RFU		Reserved	
58	RESET	I	Card Reset	-	1, 5	58	RESET	I	Card Reset	-
59	WAIT	O	Extend bus cycle	-	1, 3	59	WAIT	O	Extend bus cycle	-
60	RFU		Reserved		2, 3	60	INPACK	O	Input Port Acknowledge	-
61	REG	I	Register select	-	2,	61	REG	I	Register select & IO Enable	-
62	BVD2	O	Battery voltage detect 2		2, 3	62	SPKR	O	Audio Digital Waveform	-
63	BVD1	O	Battery voltage detect 1		2, 3	63	STSCHG	O	Card Statuses Changed	-
64	D8	I/O	Data bit 8			64	D8	I/O	Data bit 8	
65	D9	I/O	Data bit 9			65	D9	I/O	Data bit 9	
66	D10	I/O	Data bit 10			66	D10	I/O	Data bit 10	
67	CD2	O	Card detect	-	3	67	CD2	O	Card detect	-
68	GND		Ground			68	GND		Ground	

NOTES: I - Input to card, O - Output from card, I/O - Bidirectional

4.2 Memory Card Features

Table 4-3: Features of PCMCIA Memory Card

Item	Feature
Access	Random access
Data Bus	Bus 16 bits/8 bits
Memory Types	MaskROM, OTPROM, EPROM, EEPROM, Flash-Memory, SRAM
Memory Capacity	64MB (A0-A25) maximum
REG function	Attribute Memory for storing card identification
I/O Address Space	64 Mbyte (A0-A25) maximum (64 Kbyte for PC compatible architectures)
I/O Space Decoding	Overlapping I/O Address Window: card performs partial selection decoding Independent I/O Address Window: system performs entire selection decoding
I/O Interrupts	1 Interrupt Request signal per card. Routed to specific interrupt level by the host system

4.2.1 Memory Types and Speed Version

Table 4-4: Memory Types and Speed Version

Memory Type	Speed Version				
	600ns[1]	250ns	200ns	150ns	100ns
SRAM	Defined	defined	defined	defined	defined
MaskROM, OTPROM, EPROM, EEPROM, Flash-Memory	Defined	defined	defined	defined	defined

1. Specified for Dual Operating Voltage Cards while operating at Reduced Operating Voltage (Vcc = 3.3 volts).

4.3 Signal Description

Table 4-5: PC Card Logic Levels

DC Levels		Host		Card
Parameter	Conditions	Min	Max	
V_{IH}	Vcc = 5 V +/- 5%	2.4 V	Vcc+.25 V	TTL or CMOS
V_{IL}	Vcc = 5 V +/- 5%	0.0 V	0.8 V	TTL or CMOS
V_{OH}	Vcc = 5 V +/- 5%	2.8V (.9Vcc)[1]	Vcc	TTL or CMOS
V_{OL}	Vcc = 5 V +/- 5%	0.0 V	0.5 V (.1 Vcc)[1]	TTL or CMOS
V_{IH}	Vcc = 3.3V +/- 5%	Pending JEDEC Review		
V_{IL}	Vcc = 3.3V +/- 5%	Pending JEDEC Review		
V_{OH}	Vcc = 3.3V +/- 5%	Pending JEDEC Review		
V_{OL}	Vcc = 3.3V +/- 5%	Pending JEDEC Review		

1. (for CMOS Loads)

Implementation Note:

For "PC" compatible computers it is recommended that –IREQ from the card be able to be routed to at least the following interrupt signals in the system.

Function	AT IRQ	XR IRQ
Communications 2 (COM2)	IRQ3	IRQ3
Communications 1 (COM1)	IRQ4	IRQ4
Fixed Disk	IRQ14	IRQ5
Floppy Disk	IRQ6	IRQ6
Parallel Port (LPT1)	IRQ7	IRQ7
Network/Other	IRQ10	Not Available

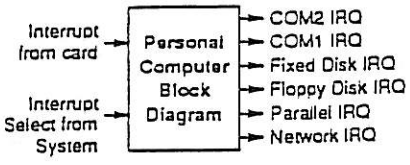


Table 4-14: Electrical Interface

Item	Signal	Card	Host	Card Output Format
Control Signal	CE1 CE2 REG IORD IOWR	pull-up to VCC R > 10K ohms and must be sufficient to keep inputs inactive when the pins are not connected at the host.[3]		
	OE WE/PGM	pull-up to VCC R > 10K ohms*[3]		
	RDY/BSY INPACK WAIT		pull-up*	
	RESET	pull-up to VCC*R > 100K ohms*		
	RFSH	NC	NC	Not Defined
Address	A0-A25	pull-down R > 100K ohms*[2]	[2]	
Data Bus	D0-D15	pull-down R > 100K ohms*[2]		
Card Detect	CD1 CD2	connected to GND in the card	pull-up	
Reserved Pin	RFU	NC	NC	
Battery/Detect	BVD1		pull-up,	asserted or
	BVD2		NOTE 1	ceasserted

*Resistor is optional

1. For implementation of BVD1 only type system.
2. Data & Address – 100pf, 450 mA sink, 150 ma source.
3. Control – 50pf, 700 ma sink, 150 mA source.
4. 50pf, 400 mA sink, 100 mA source.

Table 4-17: I/O Input Function for I/O Cards

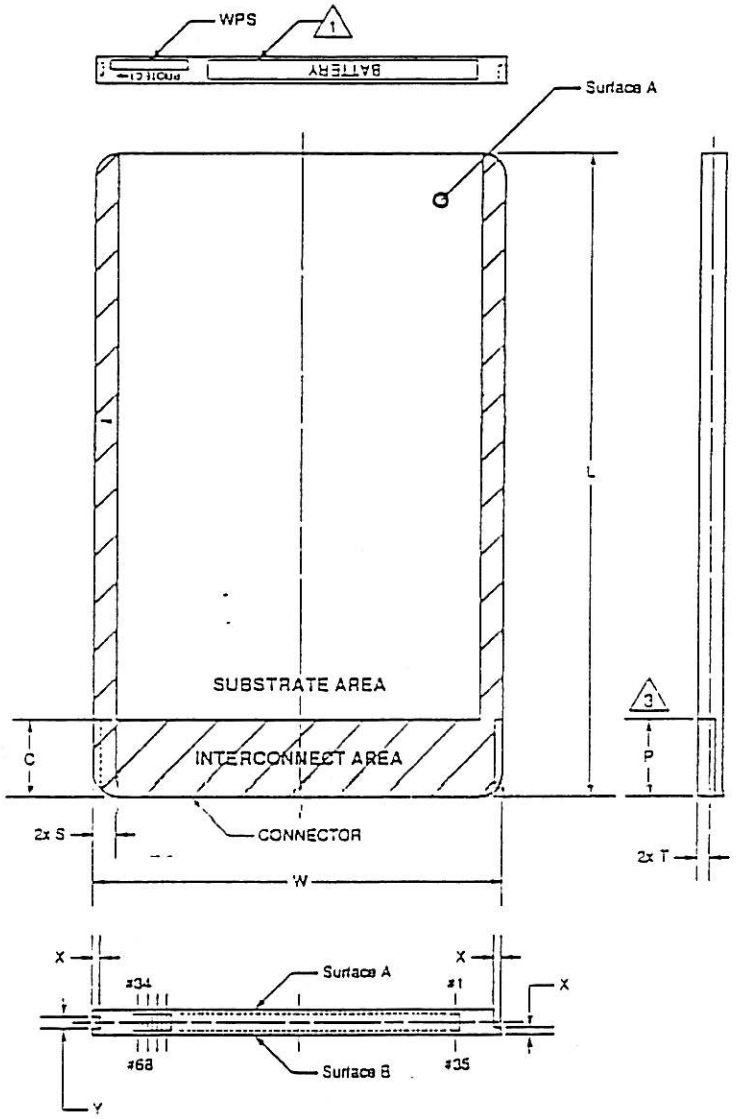
Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X
Byte Input (8 bits)	L	H	L	L	L	H	X	Even-Byte
	L	H	L	H	L	H	X	Odd-Byte
Word Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
I/O Inhibit (e.g. during DMA)	H	X	X	X	L	H	X	X
High Byte Only (Non PC Compatible)	L	L	H	X	L	H	Odd-Byte	X

Note: The VPP1 and VPP2 signals to the I/O Card are not required to be other than VCC specifically for input transfers, however, they may be required to be at other voltage levels for proper card operation as indicated in the Card Information Structure. If the required VPP levels cannot be provided by the system, the card may be rejected by the system.

Table 4-18: I/O Output Function for I/O Cards

Function Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X
Byte Input (8 bits)	L	H	L	L	H	L	X	Even-Byte
	L	H	L	H	H	L	X	Odd-Byte
Word Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Inhibit (e.g. during DMA)	H	X	X	X	H	L	X	X
High Byte Only (Non PC Compatible)	L	L	H	X	H	L	Odd-Byte	X

Note: The VPP1 and VPP2 signals to the I/O Card are not required to be other than VCC specifically for output transfers, however, they may be required to be at other voltage levels for proper card operation as indicated in the Card Information Structure. If the required VPP levels cannot be provided by the system, the card may be rejected by the system.

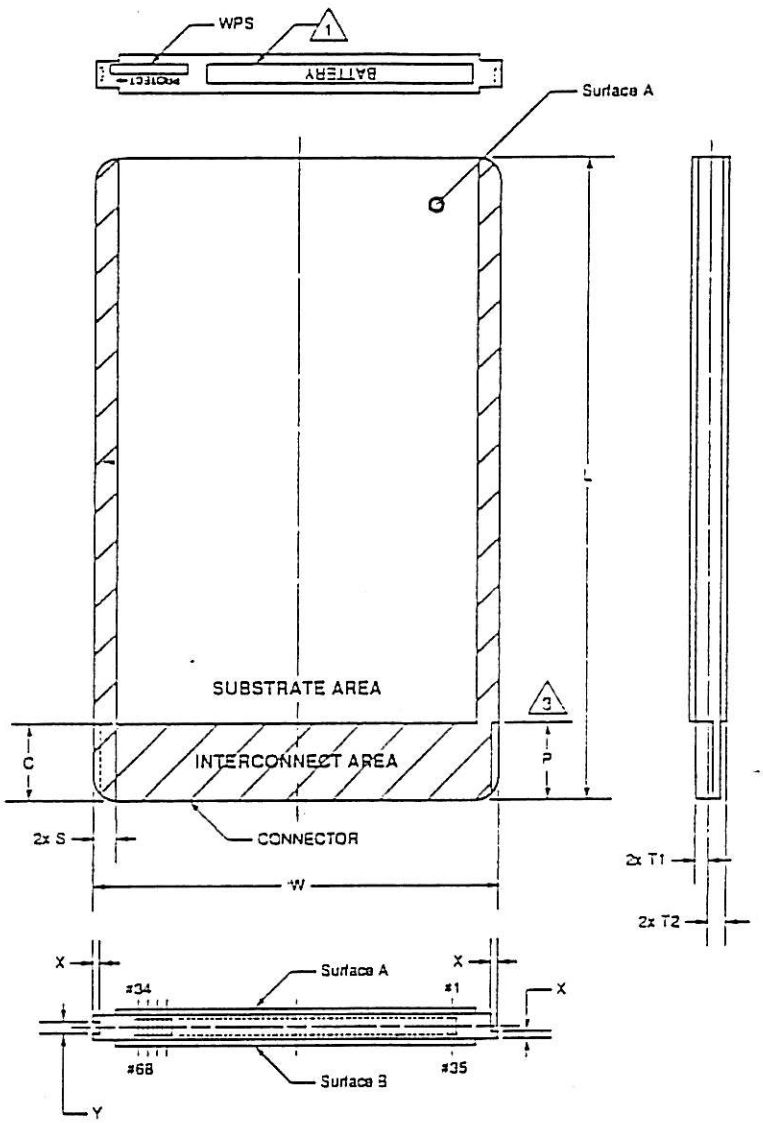


C MIN	L ± 0.008	P MIN ⚠3	S MIN	T ⚠3	W ± 0.004	X ± 0.002	Y ± 0.002
394 (10.0)	3.370 (85.60)	.394 (10.0)	.118 (3.0)	.065 (1.65)	2.126 (54.0)	.039 (1.00)	.063 (1.60)

.394

1. ⚠1 RECOMMENDED BATTERY LOCATION. THE BATTERY HOLDER SHOULD BE DESIGNED SO THAT THE POSITIVE SIDE OF THE BATTERY IS UP.
2. THE PC CARD SHALL BE OPAQUE (NON SEE THRU)
3. ⚠3 POLARIZATION KEY LENGTH.
4. ⚠4 INTERCONNECT AREA TOLERANCE = ±.002
   SUBSTRATE AREA TOLERANCE = ±.004
5. MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-1. TYPE I PC Card Package Dimensions



C MIN	L ± 0.008	P MIN 3	S MIN	T1 ±0.002	T2 MAX	W ± 0.004	X ± 0.002	Y ± 0.002
.394 (10.0)	3.370 (85.60)	.394 (10.0)	.118 (3.0)	.065 (1.65)	.098 (2.50)	2.126 (54.0)	.039 (1.00)	.063 (1.60)

1. RECOMMENDED BATTERY LOCATION. THE BATTERY HOLDER SHOULD BE DESIGNED SO THAT THE POSITIVE SIDE OF THE BATTERY IS UP.
2. THE PC CARD SHALL BE OPAQUE (NON SEE THRU)
3. POLARIZATION KEY LENGTH.
4. MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-2. TYPE II PC Card Package Dimensions

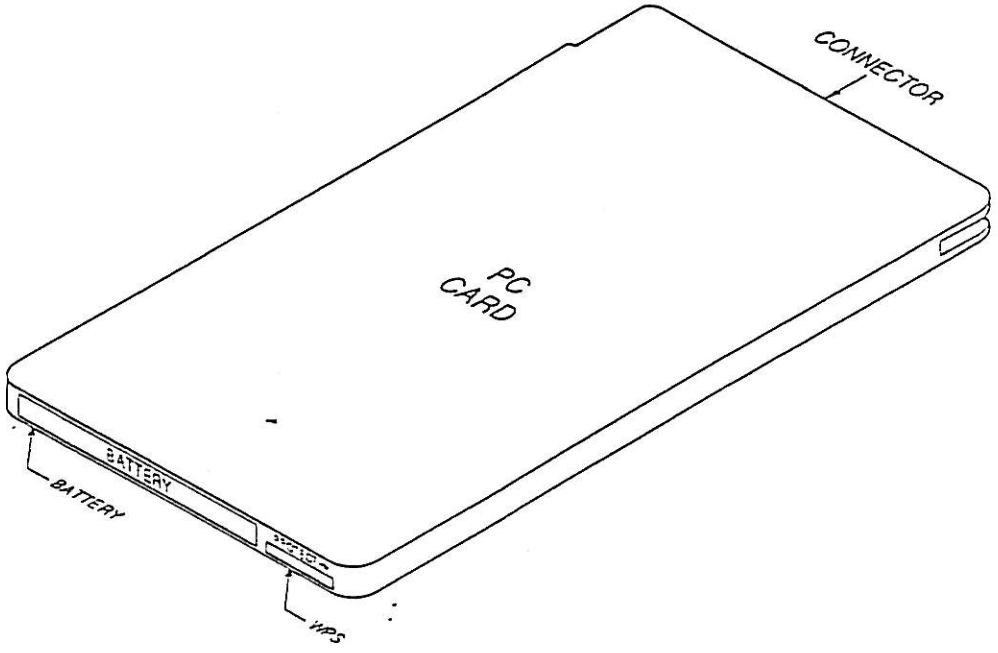


Figure 3-3. TYPE I PC Card

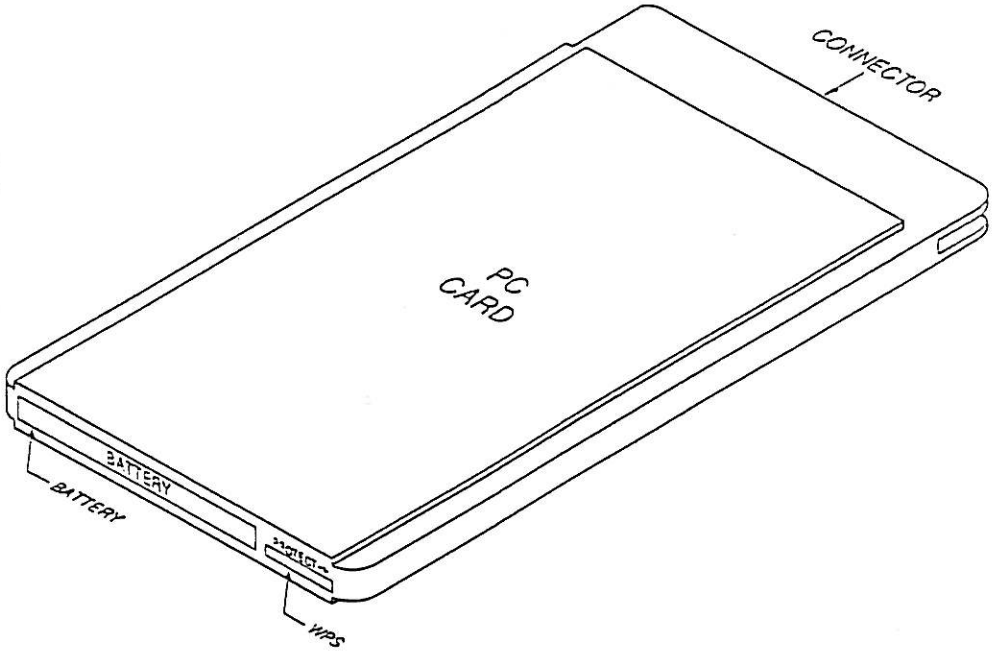
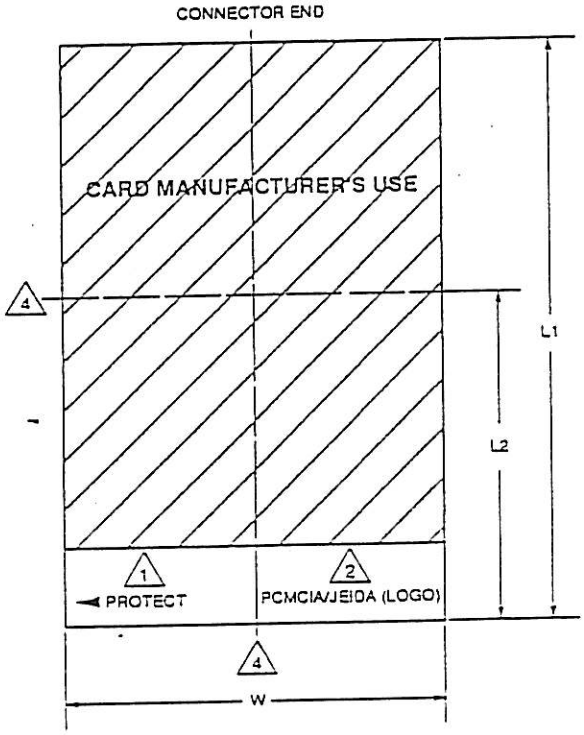


Figure 3-4. TYPE II PC Card



L1 Max	L2 Max	W Max
2.968 (75.39)	1.681 (42.70)	1.886 (47.90)

1 IF WRITE PROTECT SWITCH INSTALLED

2 OTHER REGULATORY LOGOS

3. LABELS MUST WITHSTAND ALL PC CARD ENVIRONMENTAL SPECIFICATIONS IN SUBSECTION 3.6

4 PC CARD CENTERLINES

5 LABEL, IF USED, SHALL BE ATTACHED TO THE BOTTOM COVER (SURFACE B - FIGURES 3-1 AND 3-2).

6 MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-5. PC Card Bottom Cover Label

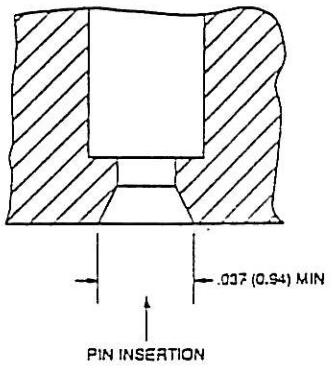
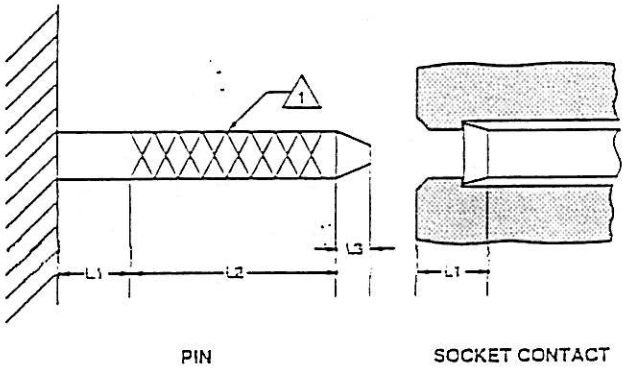


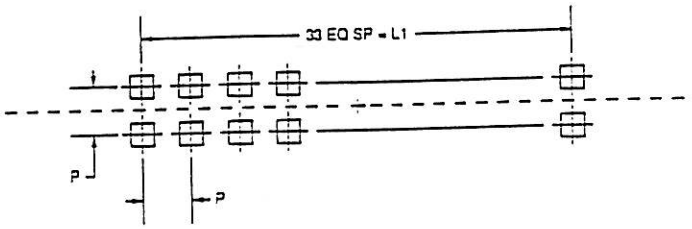
Figure 3-6. Card Connector Socket



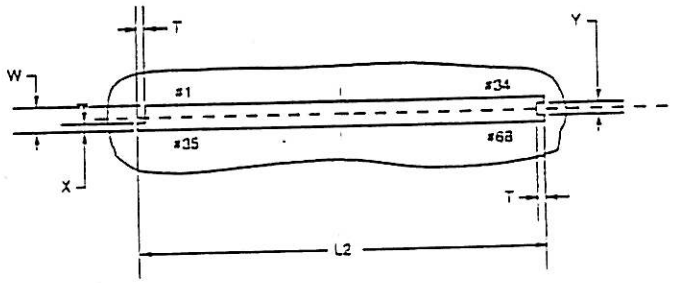
1. PIN/SOCKET CONTACT AREA
2. MILLIMETERS ARE IN PARENTHESIS ( )

L1 MAX	L2	L3 REF
.020 (0.5)	PIN TYPE - SEE TABLE 3-2 DETECT .059 (1.5) ±.039 GENERAL .084 (2.1) ±.064 POWER .098 (2.5) ±.078	.024 (0.6)

Figure 3-7. Pin/Socket Contact length with Wipe



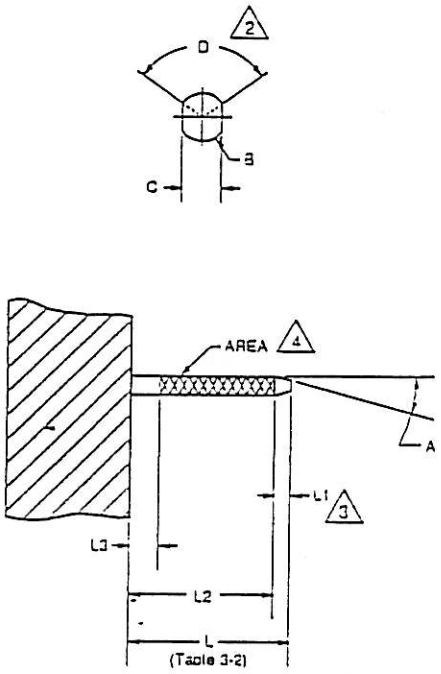
PIN LAYOUT
2 ROW - 68 PINS



FRONT VIEW

L1 ± .006	L2 ± .003	P .004	T ± .002	W ± .003	X ± .002	Y ± .002
1.65 (41.9)	2.135 (54.23)	.050 (1.27)	.035 (0.90)	.139 (3.53)	.047 (1.20)	.055 (1.40)

Figure 3-8. Pin Connector



A +5°/-0°	B ± .001 a	C MAX	D MIN	L1 ± .004	L2 MIN	L3 MAX
10°	.017 (0.44)	.018 (0.46)	110°	.020 (0.50)	.114 (2.91)	.020 (0.50)

1 LENGTH "L" GIVEN IN TABLE 3-2

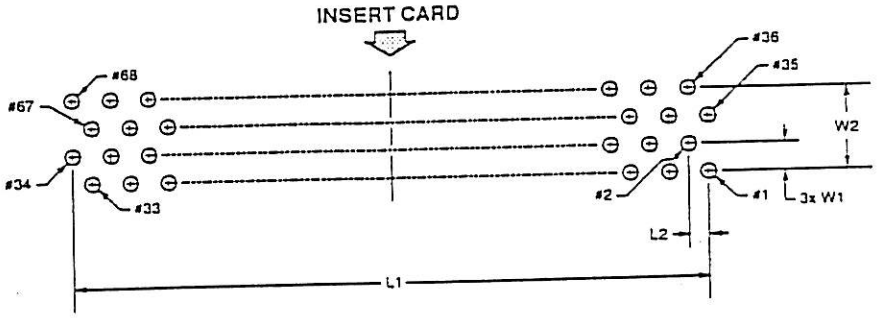
2 MINIMUM CONTACT AREA (2 PLACES)

3 PIN TAPER LENGTH

4 SOCKET CONTACT ENGAGEMENT AREA

5 MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-9. PC Card Contact Pins



L1 ± .003	L2 ± .002	W1 ± .002	W2 REF
1.650 (41.91)	.050 (1.27)	.075 (1.905)	.225 (5.715)

1. MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-10. Recommended Right Angle Connector PCB Footprint

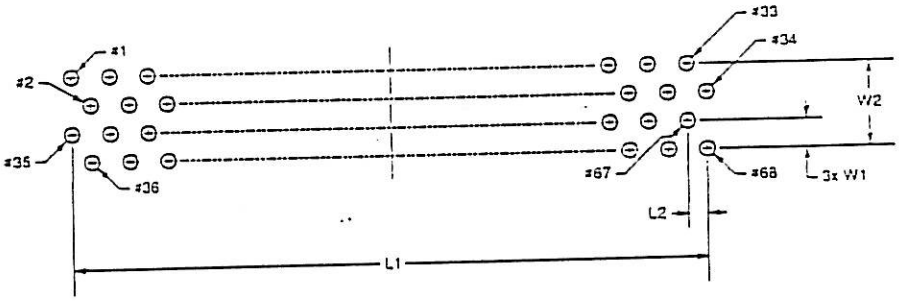
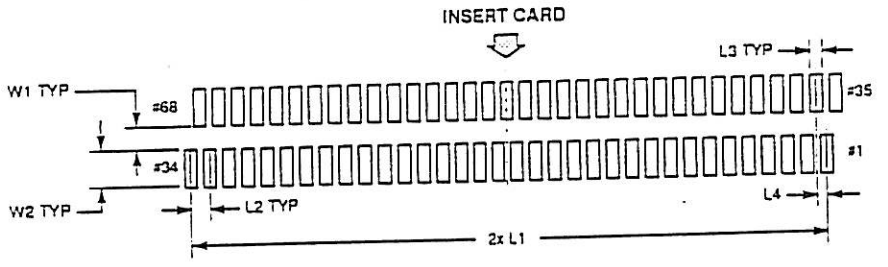


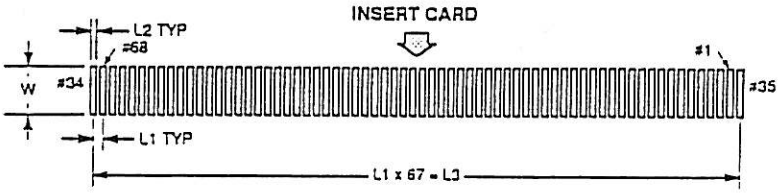
Figure 3-11. Recommended Straight Connector PCB Footprint



L1 ±.004	L2 ±.002	L3 ±.002	L4 Ref	W1 ±.004	W2 ±.04
1.650 (41.91)	.050 (1.27)	.031 (.079)	.025 (0.635)	.059 (1.50)	.098 (2.50)

1. Millimeters are in parenthesis ( ).

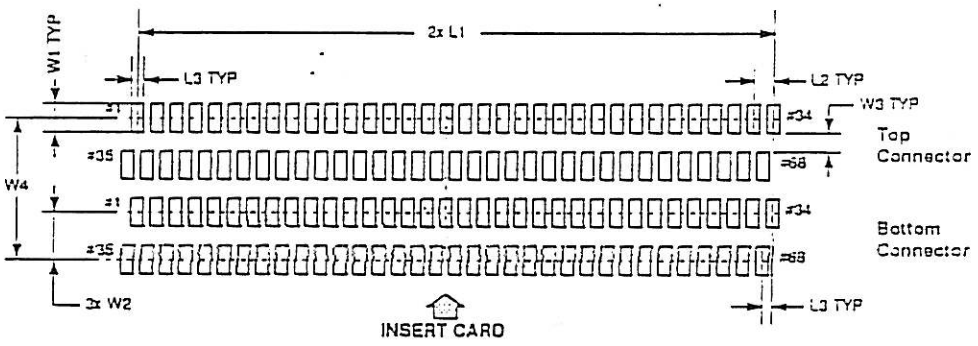
Figure 3-12. Recommended Surface Mount Connector PCB Footprint



L1 ±.002	L2 ±.002	L3 ±.002	W ±.002
.025 (0.635)	.016 (0.40)	1.675 (42.54)	.123 (3.10)

1. Millimeters are in parenthesis ( ).

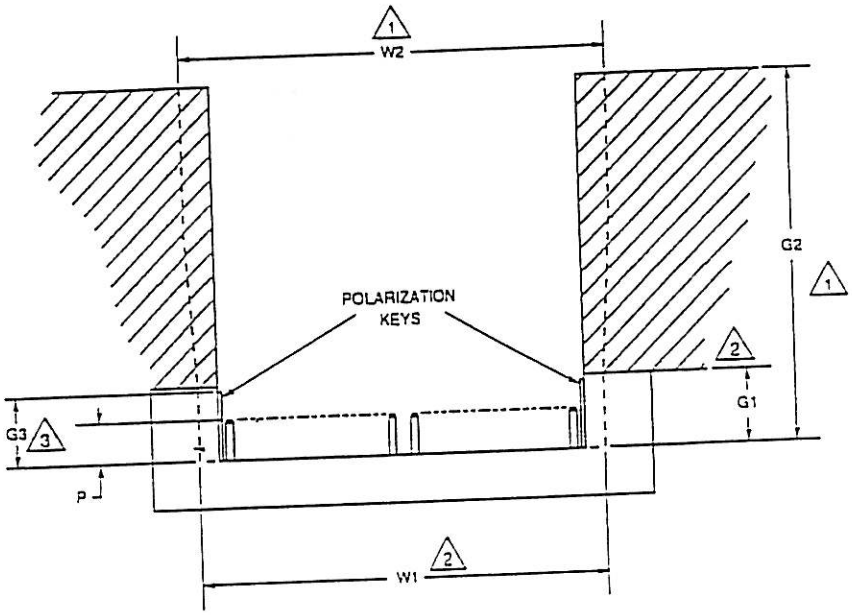
Figure 3-13. Recommended Surface Mount Connector PCB Footprint



L1 ±.004	L2 ±.002	L3 ±.002	W1 ±.004	W2 ±.002	W3 ±.002	W4 Ref
1.650 (41.91)	.050 (1.27)	.025 (0.635)	.075 (1.90)	.126 (3.20)	.051 (1.30)	.378 (9.60)

1. Millimeters are in parenthesis ( ).

Figure 3-14. Recommended Double (136 Position) Surface Mount P.C.B. Footprint



G1 MIN	G2 MIN	G3 ± .012	P MAX	W1 ±.003	W2 ± .005
.394 (10.0)	1.570 (40.0)	.382 (9.7)	.201 (5.1)	2.135 (54.23)	2.239 (56.60)

1 THE PC CARD SHOULD BE GUIDED FOR A MINIMUM DISTANCE OF 1.570 (40.0)

2 THE CONNECTOR MUST GUIDE THE PC CARD FOR A MINIMUM DISTANCE OF .197 (5.0) BEFORE ENGAGEMENT

3 THE CONNECTOR POLARIZATION KEYS ARE DEFINED IN FIGURE 3-8.

4 MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-15. PC Card Guide Guidance

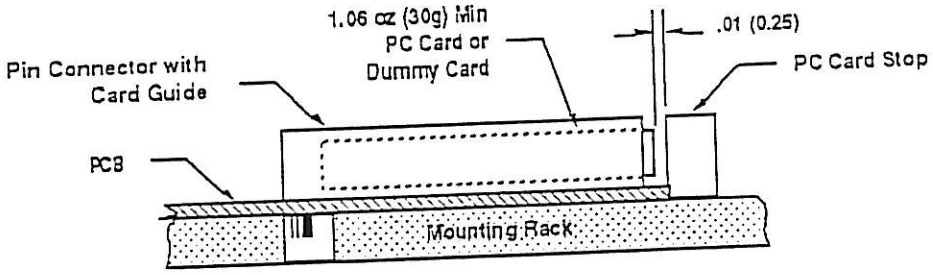
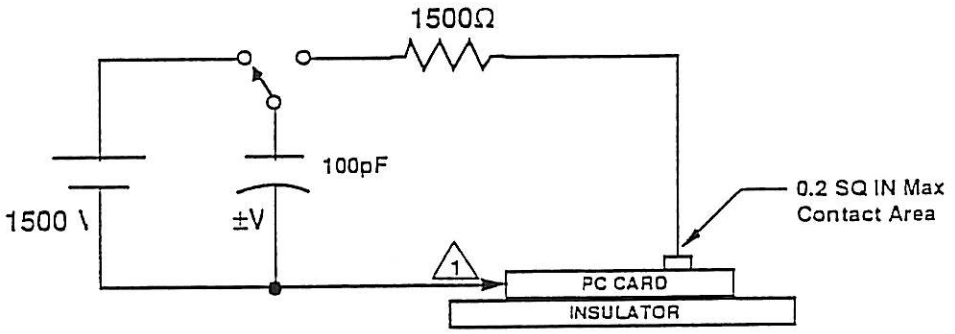
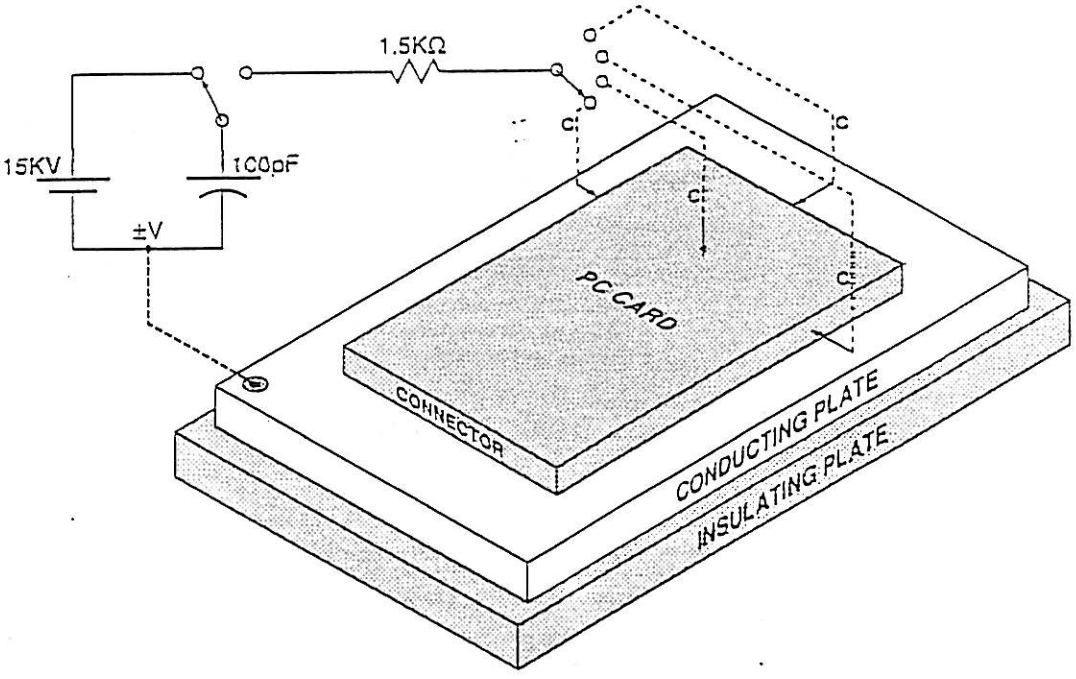


Figure 3-16. Connector Shock & Vibration Test Fixture



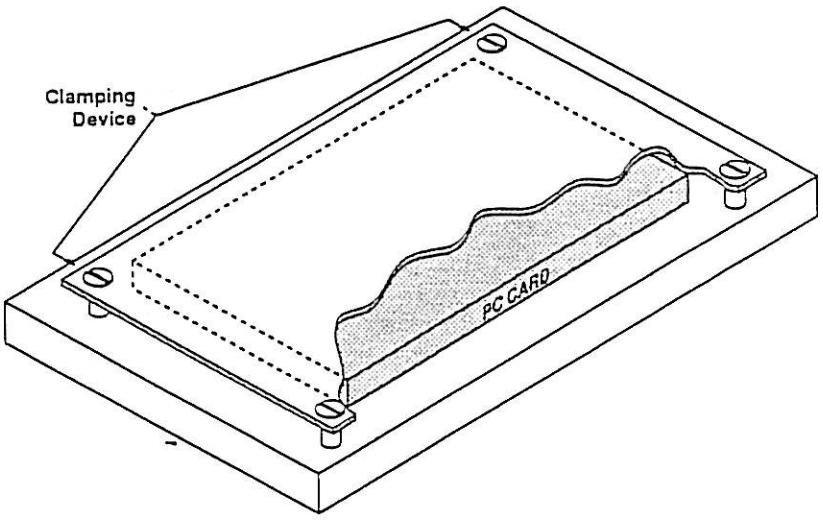
1 Connect to the four (4) ground contacts (Pin No's 1, 34, 35 and 68)

Figure 3-17. Electrostatic Discharge Test-1 Fixture



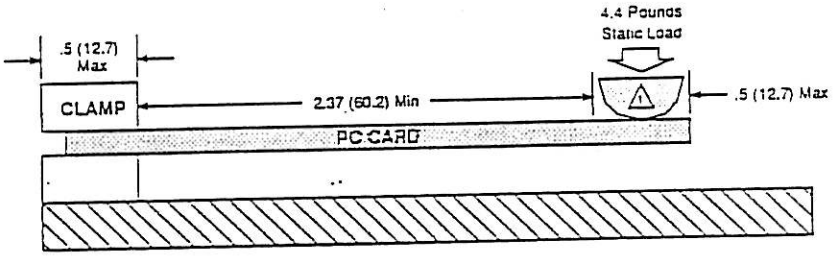
1. PC Card to make contact with the conducting plate. Discharge to top cover, left side, non-connector end and right side three times each. Total discharge cycles = 12 on each side.
2. The pc card cover facing the conducting plate, should make contact with the conducting plate during test.

Figure 3-18. Electrostatic Discharge Test-2 Fixture



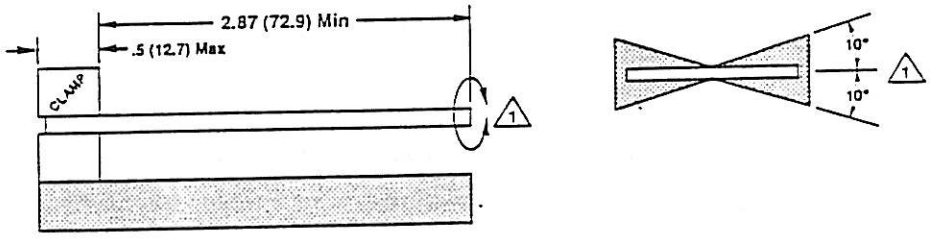
1. The pc card shock and vibration test fixture shall entrap the pc card such that all shock and vibration shall be transmitted into the card.

Figure 3-19. PC Card Shock and Vibration Test Fixture



1 The contact radius force bar is 0.197" ±0.039" (5.0).
2. The force bar shall apply a uniform force across the end of the PC Card.
3. Millimeters are in parenthesis ( ).

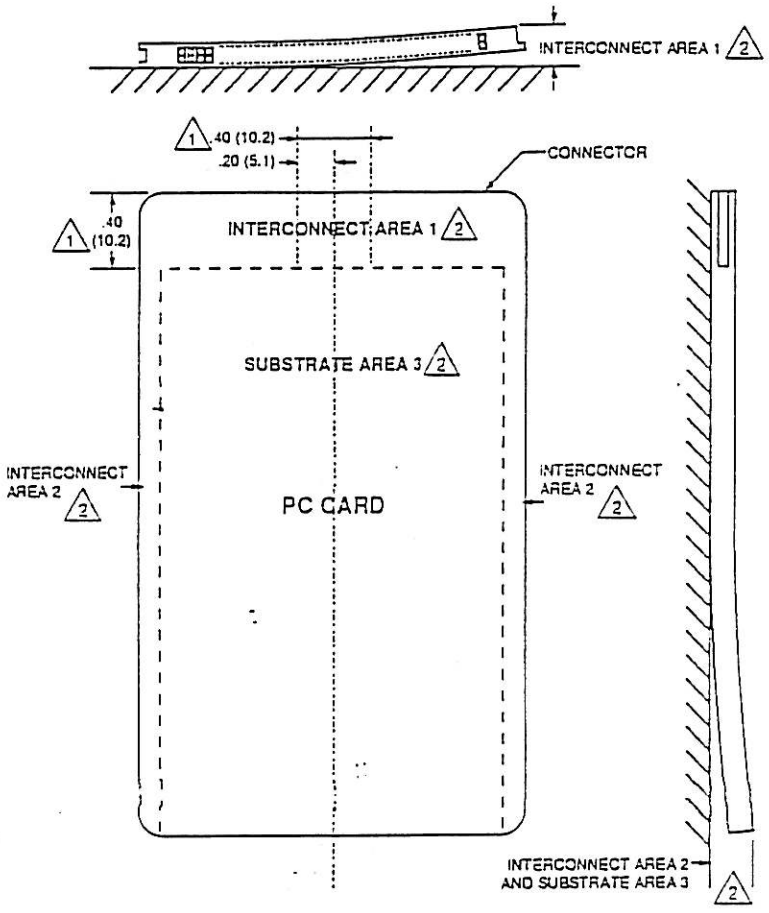
Figure 3-20. Bend Test Fixture



1 Apply torque to unclamped end of PC card. The torque and angle Max are :
Torque 11in-lbs (12.6 kg-cm) or 10° whichever occurs first.

1. Millimeters are in parenthesis ( ).

Figure 3-21. Torque Test Fixture



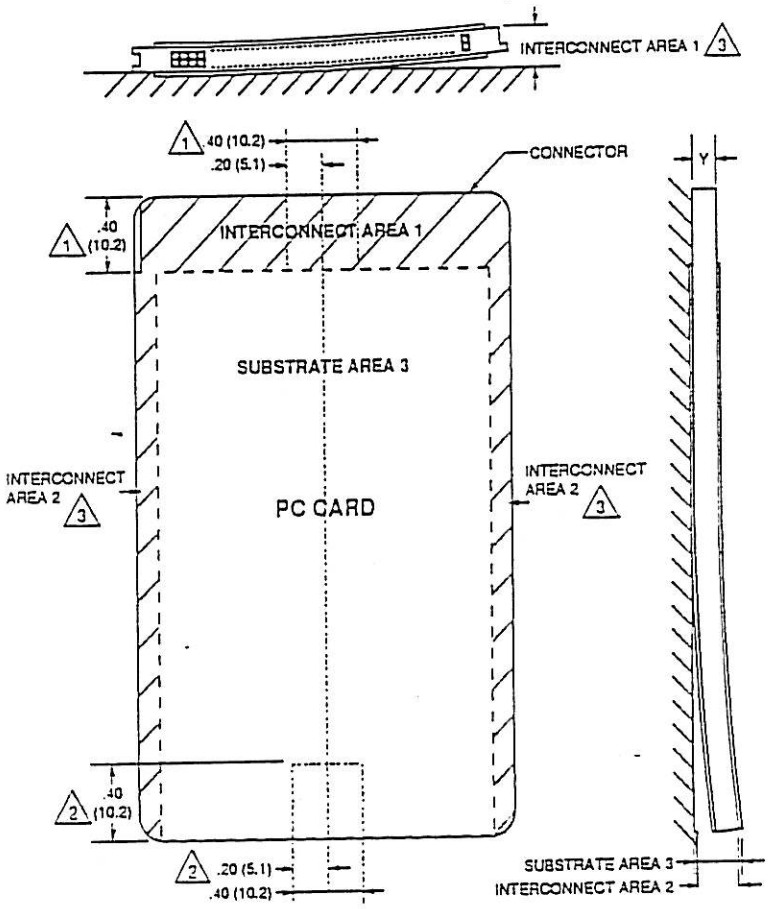
1 PC CARD THICKNESS (T MIN) MEASUREMENT AREA

2 WARPAGE IN INTERCONNECT AREA 1 AND 2 AND SUBSTRATE AREA 3 ARE DEFINED AS:

AREA	WARPAGE SPECIFICATION
INTERCONNECT AREA 1	Tmax ≤ Tmin+0.005 (0.15)
INTERCONNECT AREA 2	Tmax ≤ Tmin+0.014 (0.35)
SUBSTRATE AREA 3	Tmax ≤ Tmin+0.020 (0.5) ≤ 0.150 (3.8)

3. MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-22. Type I PC Card Warpage Test Fixture



1. PC CARD INTERCONNECT THICKNESS (T MIN) MEASUREMENT AREA
2. PC CARD SUBSTRATE THICKNESS (T SUB) MEASUREMENT AREA
3. WARPAGE IN INTERCONNECT AREA 1 AND 2 AND SUBSTRATE AREA 3 ARE DEFINED AS:

AREA	WARPAGE SPECIFICATION
INTERCONNECT AREA 1	Tmax ≤ Tmin+0.006 (0.15)
INTERCONNECT AREA 2	Tmax ≤ Tmin+0.014 (0.35)
SUBSTRATE AREA 3	Tmax ≤ Tsub+0.020 (0.5) ≤ 0.211 (5.35)

4. THE PC CARD SUBSTRATE AREA 3 THICKNESS SHALL NOT EXCEED: T SUB±0.008 (0.2)
5. MILLIMETERS ARE IN PARENTHESIS ( ).

Figure 3-23. Type II PC Card Warpage Test Fixture

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