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X3T9.2/91-010R4

Working draft proposed
American National Standard
for information systems -

SCSI-3 Parallel Interface
(SPI)

May 14, 1992

Secretariat

Computer and Business Equipment Manufacturers Association

Abstract: This standard defines mechanical, electrical, and timing requirements for the SCSI-3 Parallel Interface. This standard is principally intended to be used in conjunction with the SCSI-3 Interlocked Protocol Standard. Alternately, the SCSI-3 Generic Packetized Protocol (GPP) Standard may be used in conjunction with this Standard. The resulting interface facilitates the interconnection of computers and intelligent peripherals and thus provides a common interface specification for both systems integrators and suppliers of intelligent peripherals.

This is an internal working document of X3T9.2, a Task Group of Accredited Standards Committee X3. As such, this is not a completed standard. The contents are actively being modified by the X3T9.2 Task Group. This document is made available for review and comment only.

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STATUS OF EDITING:

The SCSI-3 Parallel Interface contains several changes to the SCSI-2 physical standard:

1. Elimination of the A and B cables
2. Inclusion of P and Q cables, including a new retention mechanism
3. A packetized data transfer mode characterized by SELECTION with ATN false.
4. More concise timing definitions
5. Tighter restrictions on cabling and transceivers to improve signal quality

REVISION 3:

- Added Houlder suggestion from 91-180 (Fast refers to negotiated values only, not to actual transfer rate).
- Table 1 - Diff nonshielded low density should be table 5 not 6, diff A/P/Q shielded high density should be 5/6/7, not 6/7/8, diff low density should be 5 not 6 (Spence 12/2).
- SELECTION Phase updated to include intermix (rules regarding who drives parity and who checks)
- 1000 mA for P-cable TERMPWR, not 1500 mA (3/13/92).
- A-cable removed, except for backwards references to SCSI-2 where applicable (3/13/92)
- Annex C added, Table 12 simplified to have just one set of setup/hold timings (3/20/92)
- Fast cable skew removed - just one cable skew, which is achievable by all cable vendors and simplifies skew calculations (3/20/92).

REVISION 4:

- Tables converted to IBM characters to allow ASCII export. Tables renumbered to get correct sequence.
- Figures 1, 2, and 3 updated. Figure 6 added. Figures renumbered.
- Added List of Tables, and List of Figures to Table of Contents
- Incorporated changes from the April SPI Working Group:
  - Steele's glitch swallowing
  - Chan's adjusted skew budget
  - Corrected propagation delay
  - Corrected bus timing values
  - corrected pin capacitance
- Corrected Table 6 column DB(15-0,P) for command, status, and message phases.
- Annex C, Figure 11 still needs correction for change in skew values
- Annex B still needs work adding measurement recommedations

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LIST OF FIGURES

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1 Forward

The SCSI protocol is designed to provide an efficient peer-to-peer I/O bus with up to 32 devices, including one or more hosts. Data may be transferred asynchronously at rates that depend primarily on device implementation and cable length. Synchronous data transfers are supported at rates up to 10 mega-transfers per second. With the 32-bit wide data transfer option, data rates of up to 40 megabytes per second are possible.

With any technical document there may arise questions of interpretation as new products are implemented. The X3 Committee has established procedures to issue technical opinions concerning the standards developed by the X3 organization. These procedures may result in SCSI Technical Information Bulletins being published by X3.

These Bulletins, while reflecting the opinion of the Technical Committee which developed the standard, are intended solely as supplementary information to other users of the standard. This standard, ANS X3.xxx-199x, as approved through the publication and voting procedures of the American National Standards Institute, is not altered by these bulletins. Any subsequent revision to this standard may or may not reflect the contents of these Technical Information Bulletins.

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2 Scope

This American National Standard defines the physical attributes of an input/output bus for interconnecting computers and peripheral devices. Figure 1 shows the relationship of this document to other SCSI-3 standards.

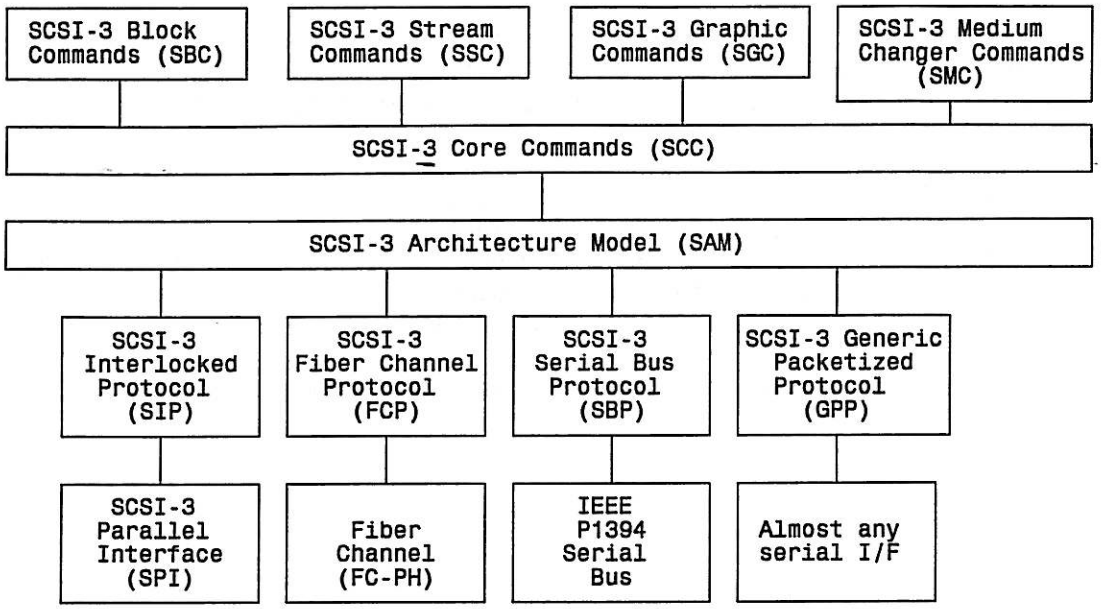


Figure 1: SCSI-3 Document Roadmap

This roadmap is intended to show the general applicability of documents to one another, not a hierarchy, protocol stack, or system architecture. For example:

- ASIP, SBP, and FCP are link-specific protocols designed to be applied to the physical interfaces directly below them.
- SBC, SSC, SGC, SMC, SCC and SAM are applicable to all link protocols.
- GPP is intended to be used with any physical interface.

Of the above standards, only the following fall under the jurisdiction of X3T9.2:

SCSI-3 Generic Packetized Protocol (GPP) [X3T9.2/92-101]
SCSI-3 Serial Bus Protocol (SBP) [X3T9.2/92-102]
SCSI-3 Fiber Channel Protocol (FCP) [X3T9.2/92-103]
SCSI-3 Architecture Model (SAM) [X3T9.2/92-104]
SCSI-3 Core Commands (SCC) [X3T9.2/92-105]
SCSI-3 Block Commands (SBC) [X3T9.2/92-106]
SCSI-3 Stream Commands (SSC) [X3T9.2/92-107]
SCSI-3 Graphic Commands (SGC) [X3T9.2/92-108]
SCSI-3 Medium Changer Commands (SMC) [X3T9.2/92-109]

The original Small Computer System Interface Standard, X3.131-1986, is referred to herein as SCSI-1. SCSI-1 was revised resulting in the Small Computer System Interface - 2 (X3.131-199x), referred to herein

as SCSI-2. This standard, the SCSI-3 Interlocked Protocol, the SCSI Packetized Protocol, and the SCSI-3 Command Set are referred to herein as SCSI-3. The term SCSI is used wherever it is not necessary to distinguish between the versions of SCSI.

This document defines the mechanical, electrical, and timing requirements of the parallel interface to allow inter-operatability of conforming devices at the data transport level.

The SCSI-3 Parallel Interface is a local I/O bus that can be operated over a wide range of data rates. The objectives of the Parallel Interface and Interlocked Protocol on SCSI-3 are:

1. To provide host computers with device independence within a class of devices. Thus, different disk drives, tape drives, printers, optical media drives, and other devices can be added to the host computers without requiring modifications to generic system hardware. Provision is made for the addition of special features and functions through the use of vendor unique indications. Reserved areas are provided for future standardization.

2. To provide compatibility with SCSI-2 devices. Devices meeting SCSI-2 and the SCSI-3 Parallel Interface standards can co-exist on the same bus. Properly conforming SCSI-2 devices, both initiators and targets, should respond in an acceptable manner to reject SCSI-3 protocol extensions. All SCSI-3 protocol extensions are designed to be permissive of such rejections and to allow the SCSI-2 device to continue operation without requiring the use of the extension.

3. To move device-dependent intelligence out to the SCSI-3 devices. Refer to the SCSI-3 Interlocked Protocol and SCSI-3 Command Set standards.

The interface protocol includes provision for the connection of multiple initiators (SCSI devices capable of initiating an I/O process) and multiple targets (SCSI devices capable of responding to a request to perform an I/O process). Distributed arbitration (i.e., bus-contention logic) is built into the architecture of SCSI. A priority system awards interface control to the highest priority SCSI device that is contending for use of the bus.

The SCSI-3 Parallel Interface standard is divided into four major sections:

Section 5: Physical characteristics (primarily cable, connector, and pinout descriptions).
Section 6: Electrical characteristics (both single-ended and differential).
Section 7: Bus Timing (both standard and fast parallel bus timing).
Section 8: Logical characteristics (primarily Parallel Bus events and phases)

Annexes A and B provide information to assist with implementation of the Parallel Interface standard.

3 Referenced Standards and Organizations

This standard is intendend for use in conjunction with the Standard for Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems, EIA RS-485-1983 (available from the Electronic Industries Association, 2001 Eye Street NW, Washington, D.C. 20006).

American National Standard Small Computer System Interface - 2, X3.131-1991, may also be useful to achieve compatibility with devices that conform to version 2 of SCSI.

The SCSI-3 Interlocked Protocol (X3T9.2/91-xxx) defines the bus conditions, phase sequences, messaging, and interlocked-specific commands and status needed to support the Parallel Interface.

The SCSI-3 Command Set (X3T9.2/91-yyy) defines the device-specific command sets used by both the SCSI-3 Packetized Protocol and the SCSI-3 Interlocked Protocol.

EIA 364-23A

IEEE 1156.2

ASTM D-4566

4 Glossary and Conventions

4.1 Glossary

This section contains a glossary of special terms used in this standard.

4.1.1 ACKx: A bus signal which is either the ACK or ACKQ signal.

4.1.2 AWG: American Wire Gauge

4.1.3 byte: In this standard, this term indicates an 8-bit construct.

4.1.4 contact: The electrically-conductive portion of a connector associated with a single conductor in a cable.

4.1.5 fast synchronous data transfer: When devices negotiate a synchronous data transfer period of 196 nanoseconds or less they are said to be using fast synchronous data transfers.

4.1.6 initiator: An SCSI device (usually a host system) that requests an I/O process to be performed by another SCSI device (a target).

4.1.7 initiator mode: The mode of operation of a port in which the port performs initiator functions.

4.1.8 interlocked mode: When a port operates under the protocol defined in the SCSI-3 Interlocked Protocol document it is said to be in interlocked mode.

4.1.9 mandatory: The referenced item is required to claim compliance with this standard.

4.1.10 mm: Millimeter.

4.1.11 ms: Millisecond.

4.1.12 ns: Nanosecond.

4.1.13 odd parity: Odd logical parity, where the parity bit is driven and verified to be that value which makes the number of assertions on the associated data byte plus the parity bit equal to an odd number (1,3,5, or 7). See parity bit.

4.1.14 optional: The referenced item is not required to claim compliance with this standard.

4.1.15 packetized mode: When a port operates under the protocol defined in the SCSI-3 Packetized Protocol document it is said to be in packetized mode.

4.1.16 parity bit: A bit associated with a byte which is used to detect the presence of single-bit errors within the byte. The parity bit is driven such that the number of logical ones in the byte plus the parity bit is either even or odd.

4.1.17 port: A single attachment to an SCSI bus from an SCSI device.

4.1.18 REQx: A bus signal which is either the REQ or REQQ signal.

4.1.19 reserved: The term used for bits, fields, signals, and code values that are set aside for future standardization.

4.1.20 SCSI: Either SCSI-2 or SCSI-3.

4.1.21 SCSI-2: The Small Computer System Interface - 2 (X3.131-199X).

4.1.22 SCSI Address: The decimal representation of the unique address (0-31) assigned to an SCSI device. This address would normally be assigned and set in the SCSI device during system installation.

4.1.23 SCSI ID: The bit-significant representation of the SCSI address referring to one of the signal lines DB(31-0).

4.1.24 SCSI device: An initiator or a target that can be attached to the SCSI bus.

4.1.25 signal assertion: The act of driving a signal to the true state.

4.1.26 signal negation: The act of performing a signal release or of driving a signal to the false state.

4.1.27 signal release: The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

4.1.28 source (a signal): The act of either signal assertion, signal negation, or signal release.

4.1.29 target: An SCSI device that performs an I/O process requested by an initiator.

4.1.30 target mode: The mode of operation of a port in which the port performs target functions.

4.1.31 us: Microsecond.

4.1.32 word: In this standard, this term indiates a 1-byte, 2-byte, or 4-byte construct.

4.1.33 xx: Digits 0-9, except those used as section numbers, in the text of this standard that are not immediately followed by lower-case "b" or "h" are decimal values. Large Numbers are not separated by commas or spaces (e.g., 12345; not 12,345 or 12 345).

4.1.34 xxb: Digits 0 and 1 immediately followed by lower-case "b" are binary values.

4.1.35 xxh: Digits 0-9 and the upper-case letters "A"-"F" immediately followed by lower-case "h" are hexadecimal values.

4.2 Editorial Conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in the glossary or in the text where they first appear. Names of signals and phases are in all uppercase. Lower case is used for words having the normal English meaning.

5 Physical Characteristics

This section contains the physical definition of alternative cabling methods for 16 bit and 32 bit data paths on SCSI devices. The connectors, cables, signals, terminators, and bus timing values needed to implement the interface are covered.

5.1 Physical Description

SCSI-3 devices are daisy-chained together using either a common 68-conductor P cable and, optionally, a 68-conductor Q cable. Both ends of each cable are terminated. All signals are common among all SCSI devices on the cable. SCSI-3 devices may be mixed with SCSI-2 devices; see Annex A for information on interconnecting buses of different widths.

Two driver/receiver alternatives are specified:

(1) Single-ended drivers and receivers, which allow a cable length of six meters. See Annex B for information on constructing systems with cable lengths longer than six meters.
(2) Differential drivers and receivers, which allow a maximum cable length of 25 meters.

The single-ended and differential alternatives are mutually exclusive.

5.2 Cable Requirements

Except where noted, the cable requirements in 5.2 may also be applied to SCSI-2 A cables. The characteristic impedance of SCSI cables should be:

	Single-ended	Differential
Minimum, any signal	75 ohms	120 ohms
Maximum, any signal	96 ohms	145 ohms
Maximum difference between any two signals on the same cable (excluding the TERMPWR pair)	12 ohms	20 ohms

It is recommended that a minimum conductor size of 0.05092 square millimeters (30 AWG) be used for all conductors. This does not apply to the 8-bit SCSI-2 A cable.

The propagation delay of SCSI cables should be:

Minimum, any signal	3.429 ns/m
Maximum, any signal	4.191 ns/m
Maximum difference between any two signals on the same cable (excluding the TERMPWR pair)	0.381 ns/m

In cable assemblies incorporating shielded round, twisted-pair cable comprising a core surrounded by two or more layers of twisted pairs:

a) The REQ and ACK pairs shall be in the core. If there are more than two pairs in the core, the remainder shall contain ground pairs.
b) The data and parity pairs shall be in the outermost layers.

5.2.1 Single-Ended Cable

A 68-conductor flat cable or 34-signal twisted-pair cable shall be used for the P cable and the Q cable. The recommended maximum cumulative cable length is 6.0 meters. If twisted-pair cables are used, then twisted pairs in the cable shall be wired to physically opposing contacts in the connector.

A stub length of no more than 0.1 meters is allowed off the mainline interconnection within any connected equipment or from any connected point. Stub clustering should be avoided. Stubs should be spaced at least 0.3 meters apart.

SCSI bus termination shall be at each end of the cable and may be internal to the SCSI devices that are at the ends of the cable.

5.2.2 Differential Cable

A 34-signal twisted-pair cable shall be used for the P cable and the Q cable if the wide SCSI option is implemented. The use of twisted pair cable (either twisted-flat or discrete wire twisted pairs) is strongly recommended. Without twisted pairs, even at slow data rates and very short distances, crosstalk between adjacent signals causes spurious pulses with differential signals. The maximum cumulative cable length shall be 25 meters. If twisted-pair cables are used, then twisted pairs in the cable shall be wired to physically opposing contacts in the connector.

A stub length of no more than 0.2 meters is allowed off the mainline interconnection within any connected equipment or from any connected point.

SCSI bus termination shall be at each end of the cable and may be internal to the SCSI devices that are at the ends of the cable.

5.2.3 Cable Requirements for Fast Synchronous Data Transfer

In systems which use the fast synchronous data transfer option, cables should meet the conductor size and impedance recommendations in 5.2. In addition, it is recommended that single-ended cable lengths be restricted to 3 meters.

In such systems, the cables shall have the following electrical characteristics:
Signal Attenuation: 0.095 dB maximum per meter at 5 MHz, measured differentially
DC Resistance: 0.230 ohms maximum per meter at 20 degrees C

5.3 Connector Requirements

Two types of connectors are defined:- nonshielded and shielded. The nonshielded connectors are typically used for in-cabinet applications. Shielded connectors are typically used for external applications where electromagnetic compatibility (EMC) and electrostatic discharge (ESD) protection may be required. Either type of connector may be used with the single-ended or differential drivers.

The P-connector system shall be a multi-wipe design with contact geometry and normal force sufficeint to pass the following test:

1) Initial contact measurement is made using the test procedure for low level contact resistence as definced in EIA 364-23A.
2) 50 mating/unmating cycles.
3) Contact resistance is measured (this is an optional step).
4) Perform flowing mixed gas test per IEEE 1156.2 on mated connectors.
5) Measure contact resistance and if there is a delta less that 15 milliohm then the connector passes.

The resistance shall be measured using a four-point dry-circuit method directly across the mated contact.

5.3.1 Nonshielded Connector Requirements

The nonshielded high-density SCSI device connector (Figure 2) shall be a 68-conductor connector consisting of two rows of 34 female contacts with adjacent contacts 1.27 mm (0.05 in) apart. The nonmating portion of the connector is shown for reference reference only.

The nonshielded high-density cable connector (Figure 3) shall be a 68-conductor connector consisting of two rows of 34 male contacts with adjacent contacts 1.27 mm (0.05 in) apart. The nonmating portion of the connector is shown for reference only.

5.3.2 Shielded Connector Requirements

One shielded connector is specified for both the P and Q cables The connector shielding system should provide a DC resistance of less than 10 milliohms from the cable shield at its termination point to the SCSI device enclosure.

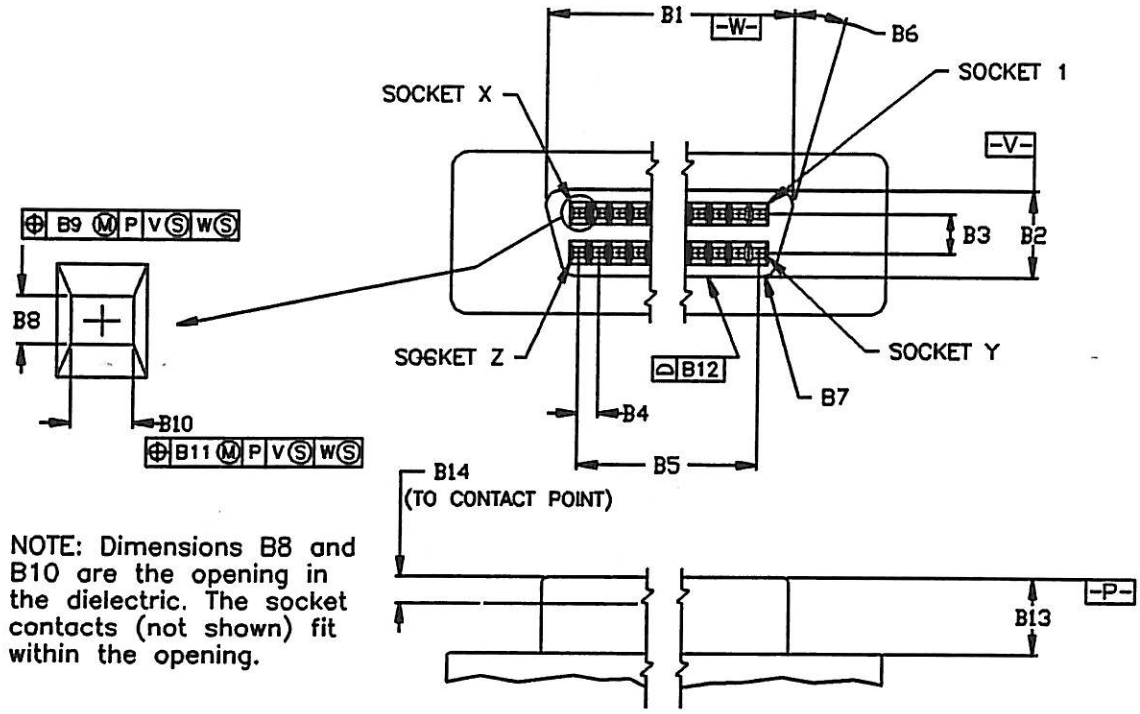
In order to support daisy-chain connections, SCSI devices that use shielded connectors should provide two shielded device connectors on the device enclosure. These two connectors may be wired

"one-to-one" with a stub to the SCSI device's drivers and receivers provided the maximum stub length is not exceeded. Alternatively, two cables may be run from the two shielded connectors to the drivers and receivers so that the maximum stub length is not exceeded. The length of the cable within the device enclosure is included when calculating the total cable length of the SCSI bus.

The shielded device connector (Figure 4) is a 68-conductor connector consisting of two rows of 34 female contacts with adjacent contacts 1.27 mm (0.05 in) apart. adjacent contacts 1.27 mm (0.05 in) apart. The nonmating portion of the connector is shown for reference only.

The shielded cable connector (Figure 5) is a 68-conductor connector consisting of two rows of 34 male contacts with adjacent contacts 1.27 mm (0.05 in) apart. The nonmating portion of the connector is shown for reference only.

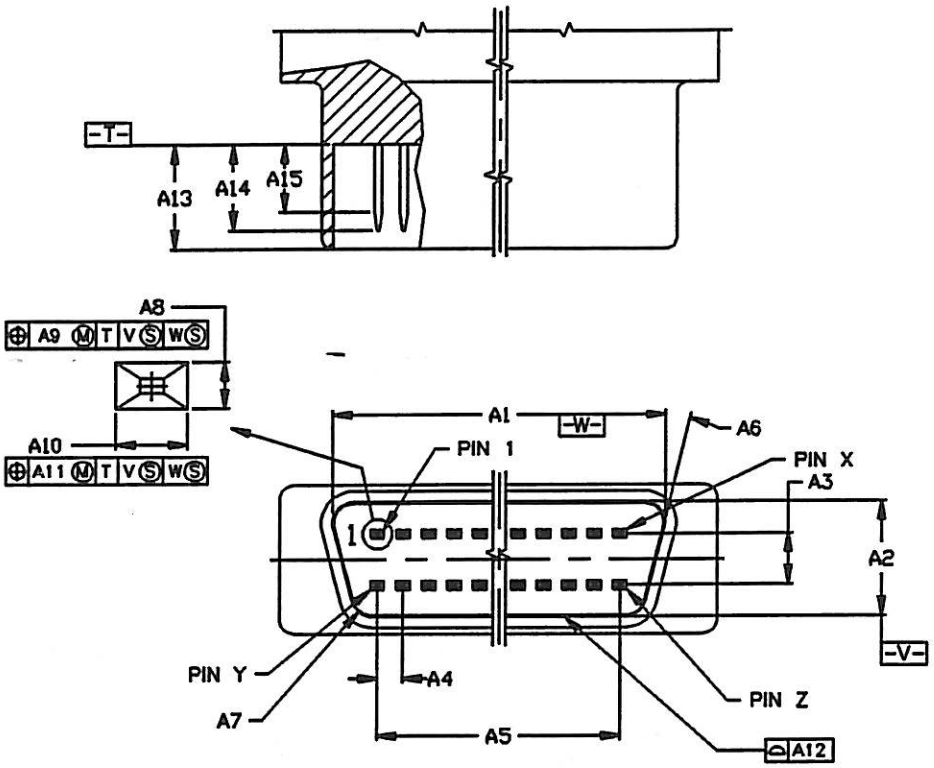
Cable retention shall consist of 2-56 jack screws capable of withstanding a minimum torque of 11 inch-pounds.



NOTE: Dimensions B8 and B10 are the opening in the dielectric. The socket contacts (not shown) fit within the opening.

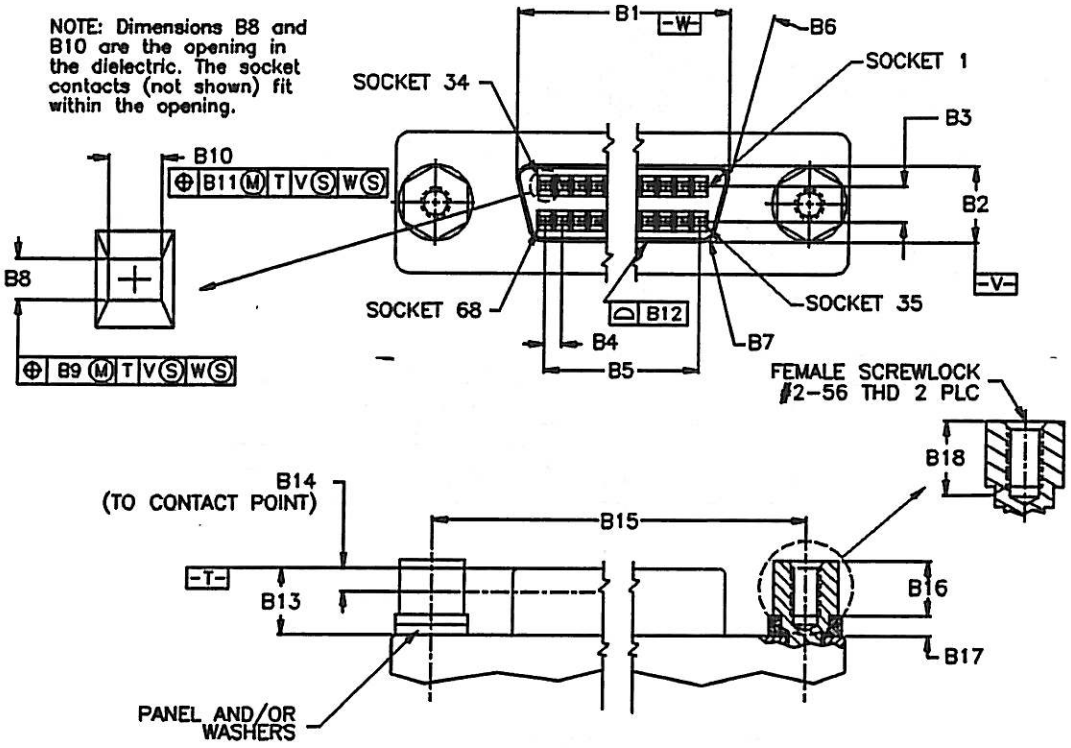
DIMENSIONS	68 POSITION MILLIMETERS	INCHES
B1	46,13	1,816
B2	5,54	0,218
B3	2,54	0,100
B4	1,27	0,050
B5	41,91	1,650
B6	15°	15°
B7	1,00 R	0,039 R
B8	0,61±0,05	0,024±0,002
B9	0,15	0,006
B10	0,86±0,10	0,034±0,004
B11	0,15	0,006
B12	0,05	0,002
B13	5,00±0,13	0,197±0,005
B14	1,75 MAX	0,069 MAX
SOCKET X	34	
SOCKET Y	35	
SOCKET Z	68	

Figure 2: Non-Shielded Device Connector



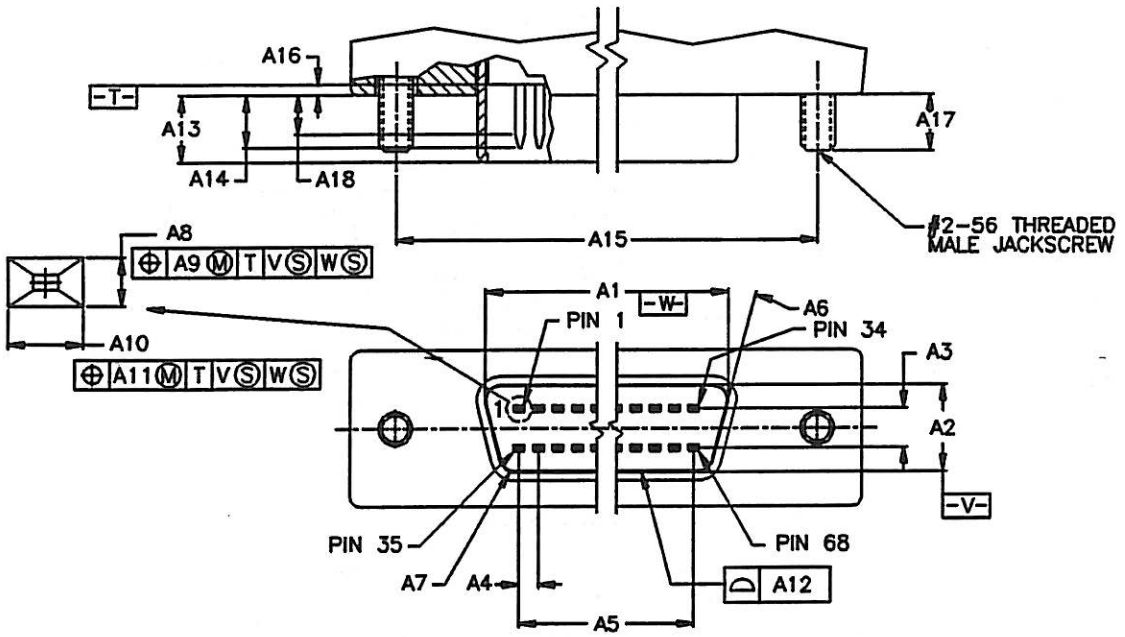
DIMENSIONS	68 POSITION	
	MILLIMETERS	INCHES
A1	46,28	1,822
A2	5,69	0,224
A3	2,54	0,100
A4	1,27	0,050
A5	41,91	1,650
A6	15°	15°
A7	1,04 R	0,041 R
A8	0,40±0,010	0,0156±0,0004
A9	0,23	0,009
A10	0,60±0,03	0,024±0,001
A11	0,23	0,009
A12	0,05	0,002
A13	5,15±0,15	0,203±0,006
A14	4,39 MAX	0,173 MAX
A15	3,02 MIN	0,119 MIN
PIN X	34	
PIN Y	35	
PIN Z	68	

Figure 3: Non-Shielded Cable Connector



DIMENSIONS	MILLIMETERS	INCHES
B1	46,13	1,816
B2	5,54	0,218
B3	2,54	0,100
B4	1,27	0,050
B5	41,91	1,650
B6	15°	15°
B7	1,00 R	0,039 R
B8	0,61±0,05	0,024±0,002
B9	0,15	0,006
B10	0,86±0,10	0,034±0,004
B11	0,15	0,006
B12	0,05	0,002
B13	5,00±0,13	0,197±0,005
B14	1,65 MAX	0,065 MAX
B15	57,91±0,13	2,280±0,005
B16	3.99±0,05	0,157±0,002
B17	1,52±0.13	0,060±0,005
B18	3,86 MIN	0,152 MIN

Figure 4: Shielded Device Connector



DIMENSIONS	MILLIMETERS	INCHES
A1	46,28	1,822
A2	5,69	0,224
A3	2,54	0,100
A4	1,27	0,050
A5	41,91	1,650
A6	15°	15°
A7	1,04 R	0,041 R
A8	0,40±0,010	0,0156±0,0004
A9	0,23	0,009
A10	0,60±0,03	0,024±0,001
A11	0,23	0,009
A12	0,05	0,002
A13	4,90±0,10	0,193±0,004
A14	4,27 MAX	0,168 MAX
A15	57,91±0,13	2,280±0,005
A16	0,25±0,13	0,010±0,005
A17	3,73±0,15	0,147±0,006
A18	2,64 MIN	0,104 MIN

Figure 5: Shielded Cable Connector

5.3.3 Connector Contact Assignments

The connector contact assignments are defined in Tables 1 through 5. Table 1 defines which of the other four tables to use and which set of contact assignments to use.

Table 1: Cross-Reference to Connector Contact Assignments

Connector Type	Driver/ Receiver Type	Cable Name	Connector Figure		Contact Assignment Table
			Device	Cable	
Nonshielded	Single-ended	P	2	3	2
	—	Q	2	3	3
	Differential	P	2	3	4
		Q	2	3	3
	Differential	P	2	3	4
		Q	2	3	5
Shielded	Single-ended	P	4	5	2
		Q	4	5	3
	Differential	P	4	5	4
		Q	4	5	5

Table 2: Single-Ended Contact Assignments - P Cable

Signal Name	Connector Contact Number	Cable Conductor Number		Connector Contact Number	Signal Name
GROUND	1	1	2	35	-DB(12)
GROUND	2	3	4	36	-DB(13)
GROUND	3	5	6	37	-DB(14)
GROUND	4	7	8	38	-DB(15)
GROUND	5	9	10	39	-DB(P1)
GROUND	6	11	12	40	-DB(0)
GROUND	7	13	14	41	-DB(1)
GROUND	8	15	16	42	-DB(2)
GROUND	9	17	18	43	-DB(3)
GROUND	10	19	20	44	-DB(4)
GROUND	11	21	22	45	-DB(5)
GROUND	12	23	24	46	-DB(6)
GROUND	13	25	26	47	-DB(7)
GROUND	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	-BSY
GROUND	24	47	48	58	-ACK
GROUND	25	49	50	59	-RST
GROUND	26	51	52	60	-MSG
GROUND	27	53	54	61	-SEL
GROUND	28	55	56	62	-C/D
GROUND	29	57	58	63	-REQ
GROUND	30	59	60	64	-I/O
GROUND	31	61	62	65	DB(8)
GROUND	32	63	64	66	-DB(9)
GROUND	33	65	66	67	-DB(10)
GROUND	34	67	68	68	-DB(11)

NOTES:

1) The hyphen preceding a signal name indicates that signal is active low.
2) The conductor number refers to the conductor position when using 0.025-inch centerline flat ribbon cable.

Table 3: Single-Ended Contact Assignments - Q Cable

Signal Name	Connector Contact Number	Cable Conductor Number		Connector Contact Number	Signal Name
GROUND	1	1	2	35	-DB(28)
GROUND	2	3	4	36	-DB(29)
GROUND	3	5	6	37	-DB(30)
GROUND	4	7	8	38	-DB(31)
GROUND	5	9	10	39	-DB(P3)
GROUND	6	11	12	40	-DB(16)
GROUND	7	13	14	41	-DB(17)
GROUND	8	15	16	42	-DB(18)
GROUND	9	17	18	43	-DB(19)
GROUND	10	19	20	44	-DB(20)
GROUND	11	21	22	45	-DB(21)
GROUND	12	23	24	46	-DB(22)
GROUND	13	25	26	47	-DB(23)
GROUND	14	27	28	48	-DB(P2)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
TERMPWRQ	17	33	34	51	TERMPWRQ
TERMPWRQ	18	35	36	52	TERMPWRQ
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
GROUND	21	41	42	55	TERMINATED
GROUND	22	43	44	56	GROUND
GROUND	23	45	46	57	TERMINATED
GROUND	24	47	48	58	-ACKQ
GROUND	25	49	50	59	TERMINATED
GROUND	26	51	52	60	TERMINATED
GROUND	27	53	54	61	TERMINATED
GROUND	28	55	56	62	TERMINATED
GROUND	29	57	58	63	-REQQ
GROUND	30	59	60	64	TERMINATED
GROUND	31	61	62	65	-DB(24)
GROUND	32	63	64	66	-DB(25)
GROUND	33	65	66	67	-DB(26)
GROUND	34	67	68	68	-DB(27)

NOTES:

1) The hyphen preceding a signal indicates that signal is active low.
2) The conductor number refers to the conductor position when using 0.025-inch centerline flat ribbon cable.
3) See 6.3.1 for a definition of the RESERVED lines.

Table 4: Differential Contact Assignments - P Cable

Signal Name	Connector Contact Number	Cable Conductor Number		Connector Contact Number	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
GROUND	6	11	12	40	GROUND
+DB(0)	7	13	14	41	-DB(0)
+DB(1)	8	15	16	42	-DB(1)
+DB(2)	9	17	18	43	-DB(2)
+DB(3)	10	19	20	44	-DB(3)
+DB(4)	11	21	22	45	-DB(4)
+DB(5)	12	23	24	46	-DB(5)
+DB(6)	13	25	26	47	-DB(6)
+DB(7)	14	27	28	48	-DB(7)
+DB(P)	15	29	30	49	-DB(P)
DIFFSENS	16	31	32	50	GROUND
TERMPWR	17	33	34	51	TERMPWR
TERMPWR	18	35	36	52	TERMPWR
RESERVED	19	37	38	53	RESERVED
+ATN	20	39	40	54	-ATN
GROUND	21	41	42	55	GROUND
+BSY	22	43	44	56	-BSY
+ACK	23	45	46	57	-ACK
+RST	24	47	48	58	-RST
+MSG	25	49	50	59	-MSG
+SEL	26	51	52	60	-SEL
+C/D	27	53	54	61	-C/D
+REQ	28	55	56	62	-REQ
+I/O	29	57	58	63	-I/O
GROUND	30	59	60	64	GROUND
+DB(8)	31	61	62	65	DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

NOTES:

1) The hyphen preceding a signal name indicates that signal is active low.
2) The conductor number refers to the conductor position when using 0.025-inch centerline flat ribbon cable.

Table 5: Differential Contact Assignments - Q Cable

Signal Name	Connector Contact Number	Cable Conductor Number		Connector Contact Number	Signal Name
+DB(28)	1	1	2	35	-DB(28)
+DB(29)	2	3	4	36	-DB(29)
+DB(30)	3	5	6	37	-DB(30)
+DB(31)	4	7	8	38	-DB(31)
+DB(P3)	5	9	10	39	-DB(P3)
GROUND	6	11	12	40	GROUND
+DB(16)	7	13	14	41	-DB(16)
+DB(17)	8	15	16	42	-DB(17)
+DB(18)	9	17	18	43	-DB(18)
+DB(19)	10	19	20	44	-DB(19)
+DB(20)	11	21	22	45	-DB(20)
+DB(21)	12	23	24	46	-DB(21)
+DB(22)	13	25	26	47	-DB(22)
+DB(23)	14	27	28	48	-DB(23)
+DB(P2)	15	29	30	49	-DB(P2)
DIFFSENS	16	31	32	50	GROUND
TERMPWRQ	17	33	34	51	TERMPWRQ
TERMPWRQ	18	35	36	52	TERMPWRQ
RESERVED	19	37	38	53	RESERVED
TERMINATED	20	39	40	54	TERMINATED
GROUND	21	41	42	55	GROUND
TERMINATED	22	43	44	56	TERMINATED
+ACKQ	23	45	46	57	-ACKQ
TERMINATED	24	47	48	58	TERMINATED
TERMINATED	25	49	50	59	TERMINATED
TERMINATED	26	51	52	60	TERMINATED
TERMINATED	27	53	54	61	TERMINATED
+REQQ	28	55	56	62	-REQQ
TERMINATED	29	57	58	63	TERMINATED
GROUND	30	59	60	64	GROUND
+DB(24)	31	61	62	65	-DB(24)
+DB(25)	32	63	64	66	-DB(25)
+DB(26)	33	65	66	67	-DB(26)
+DB(27)	34	67	68	68	-DB(27)

NOTES:

1) The hyphen preceding a signal name indicates that signal is active low. ||
2) The conductor number refers to the conductor position when using 0.025-inch centerline flat ribbon cable.
3) See 6.3.1 for a definition of the RESERVED lines.

6 Electrical Characteristics

Except where noted, the electrical specifications in section 6 may be applied to the SCSI-2 A cable. For the measurements in this section, SCSI bus termination is assumed to be external to the SCSI device. See 6.3.1 for the terminating requirements for the RESERVED lines. SCSI devices may have the provision for allowing optional internal termination.

6.1 Single-Ended Alternative

All signals not defined as RESERVED, GROUND, or TERMPWR shall be terminated at both ends of the cable. The termination of each signal shall meet these requirements:

a) The terminators shall be powered by the TERMPWR line and may receive additional power from other sources but shall not require such additional power for proper operation (see 6.3).
b) Each terminator shall source current to the signal line whenever its terminal voltage is below 2.5 volts. This current shall not exceed 24 mA for any line voltage above 0.2 volts.
c) The voltage on all released signal lines shall be at least 2.5 volts dc when the TERMPWR line is within specified values (see 6.3).
d) These conditions shall be met with any legal configuration of targets and initiators as long as at least one device is supplying TERMPWR.

6.1.1 Single-Ended Output Characteristics

All signals shall use open-collector or three-state drivers. Each signal sourced by an SCSI device shall have the following output characteristics when measured at the SCSI device's connector:
V_{OL} (low-level output voltage) = 0.0 to 0.5 volts dc at I_{OL}=48 mA (signal assertion)
V_{OH} (high-level output voltage) = 2.5 to 5.25 volts dc (signal negation)

It is recommended that devices using active negation observe the following limits:
$2.5 \leq V_{OH} \leq 3.24$ volts dc at $I_{OH} = 7$ mA
$2.0 \leq V_{OH} \leq 3.0$ volts dc at $I_{OH} \geq 24$ mA

It is recommended that devices actively negate the ACK, REQ, DATA BUS, and PARITY signals during fast synchronous data transfers.

It is recommended that all devices meet the following specifications for all signals:
t_{rise} (rise time) = 5 ns minimum (10% to 90% of full amplitude)
t_{fall} (fall time) = 5 ns minimum (90% to 10% of full amplitude)

The recommended test circuit for measurement of rise time is shown in Figure 6.

****
Bill Ham has wording to add. Single-ended drivers (both passive and active) shall maintain a high impedance state during power-up and power-down cycle until enabled.
****

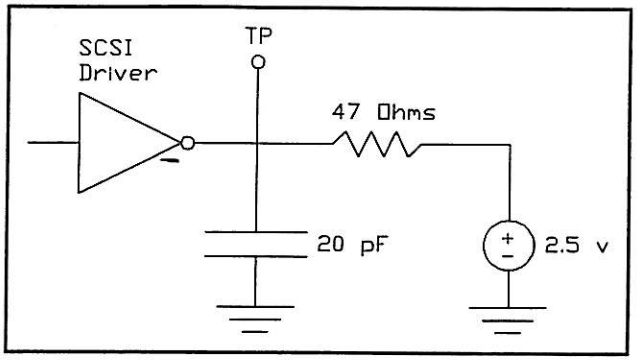


Figure 6: Rise Time Test Circuit

6.1.2 Single-Ended Input Characteristics

SCSI devices with power on shall meet the following electrical characteristics on each signal (including both receivers and passive drivers):

V_{IL} (Low-level input voltage)	= 0.0 to 0.8 volts dc (signal true)
V_{IH} (High-level input voltage)	= 2.0 to 5.25 volts dc (signal false)
I_{IL} (Low-level input current)	= -20 to 0 uA at V_I = 0.5 volts dc
I_{IH} (High-level input current)	= 0 to 20 uA at V_I = 2.7 volts dc
Minimum input hysteresis	= 0.3 volts dc
Maximum input capacitance	= 25 pF (measured at the device connector closest to the stub, if any, within the device)

It is recommended that SCSI devices with power off also meet the above I_{IL} and I_{IH} electrical characteristics on each signal.

To achieve maximum noise immunity and to assure proper operation with complex cable configurations, it is recommended that the nominal switching threshold be approximately 1.4 volts.

After a receiver recognizes a negation transition, it shall not respond for at least ten nanoseconds to a signal reversal of 1 volt or less.

****
Bill Ham has wording to add. Single-ended drivers (both passive and active) shall maintain a high impedance state during power-up and power-down cycle until enabled.
****

6.2 Differential Alternative

All signals consist of two lines denoted +SIGNAL and -SIGNAL. A signal is true when +SIGNAL is more positive than -SIGNAL, and a signal is false when -SIGNAL is more positive than +SIGNAL. All assigned signals described in 6.5 shall be terminated at each end of the cable with a terminator network as shown in Figure 7. Resistor tolerances in the terminator network shall be $\pm$5% or less.

The DIFFSENS signal of the connector is used as an active high enable for the differential drivers. If a single-ended device or terminator is inadvertently connected, this signal is grounded, disabling the differential drivers (see Figure 8).

The characteristic impedance of differential terminators is 122 ohms.

6.2.1 Differential Output Characteristics

Each signal sourced by an SCSI device shall have the following output characteristics when measured at the SCSI device's connector:

V_{OL} (Low-level output voltage) = 1.7 V maximum at I_{OL} (Low-level output current) = 55 mA.
V_{OH} (High-level output voltage) = 2.7 V minimum at I_{OH} (High-level output current) = -55 mA.
V_{OD} (Differential output voltage) = 1.0 V minimum with common-mode voltage ranges from -7 to +12 volts dc.

V_{OL} and V_{OH} shall be measured between the output terminal and logic ground of the SCSI device.

The output characteristics shall additionally conform to EIA RS-485 1983.

6.2.2 Differential Input Characteristics

SCSI devices shall meet the following electrical characteristics on each signal (including both receivers and passive drivers):

Maximum I_I (Input current on either input) = $\pm$ 2.0 mA at $-7V <= V_I <= 12$ V, device power on or off.
Maximum input capacitance = 25 pF.
Minimum input hysteresis = 35 millivolts

The output characteristics shall additionally conform to EIA RS-485 1983.

6.3 Terminator Power

SCSI initiators shall supply terminator power to the TERMPWR contact(s). This power shall be supplied through a diode or similar semiconductor that prevents backflow of power to the SCSI device. Targets and SCSI devices that become temporary initiators (e.g., targets which implement the COPY command or asynchronous event notification) are not required to supply terminator power. Any SCSI device may supply terminator power. Interface error rates are lower if the termination voltage is maintained at the extreme ends of the cable.

All terminators independent of location shall be powered from the TERMPWR contact(s). The use of keyed connectors is recommended in SCSI devices that provide terminator power to prevent accidental grounding or the incorrect connection of terminator power.

Regulatory agencies may require limiting maximum (short circuit) current to the terminator power lines.

SCSI devices providing TERMPWR shall have the characteristics shown in the following table. This table does not apply to SCSI-2 A cables.

	TERMPWR Voltage (volts DC) Minimum	Maximum	Minimum TERMPWR Source Current (milliamperes)	Recommended TERMPWR Current Limiting (Amperes)
Single-ended	4.25	5.25	1500	2.0
Differential	4.00	5.25	1000	2.0

For systems utilizing multiple initiators, the initiators may be configured with option straps or current limiting devices. Maximum available current should not exceed 5 amperes.

SCSI devices shall sink no more than 1.0 mA from TERMPWR and no more than 1.0 mA from TERMPWRB except to power an optional internal terminator.

It is recommended that the terminator power lines be decoupled at each terminator with at least a 2.2 microfarad high-frequency capacitor to improve signal quality.

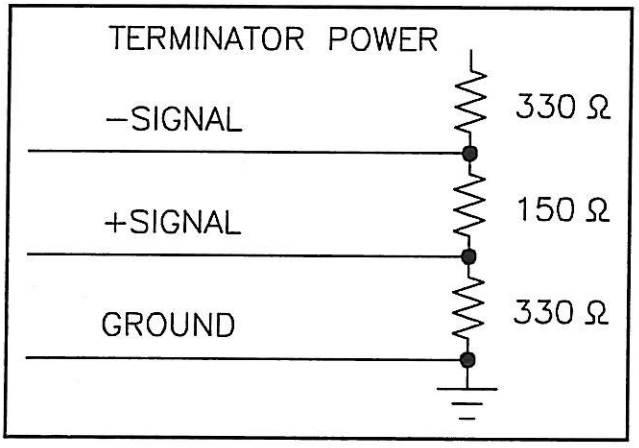


Figure 7: Termination for Differential Devices

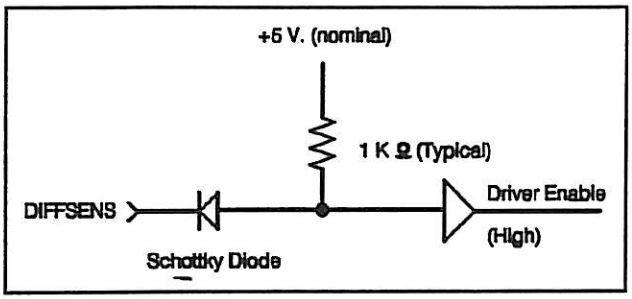


Figure 8: Differential Driver Protection Circuit

6.3.1 RESERVED Lines

The lines labeled RESERVED shall be connected to ground in the bus terminator assemblies or in the end devices on the SCSI cable. The RESERVED lines should be open in the other SCSI devices, but may be connected to ground.

6.4 SCSI Bus

Communication on the SCSI bus is allowed between only two SCSI devices at any given time. There is a maximum of 16 SCSI devices on a P cabled system and 32 SCSI devices on a P/Q cabled system. The devices can be any combination of initiators (or ports in initiator mode) and targets (or ports in target mode) provided there is at least one of each.

Each SCSI device has an SCSI address and a corresponding SCSI ID bit assigned as shown in Table 8. When two SCSI devices communicate on the SCSI bus, one acts as an initiator and the other acts as a target. The initiator originates an I/O process and the target performs the I/O process. An SCSI device usually has a fixed role as an initiator or target, but some devices may be able to assume either role.

Certain SCSI bus functions are assigned to the initiator and certain SCSI bus functions are assigned to the target. The initiator may arbitrate for the SCSI bus and select a particular target, or the target may aribtrate for the SCSI bus and reselect a particular initiator.

Table 8 shows the relationship between SCSI Addresses, SCSI IDs, and arbitration priority. A hyphen ("-") represents a logical zero bit.

Table 8: SCSI Addresses, IDs, and Arbitration Priorities

6.5 SCSI Bus Signals

The P cable has 9 control signal pairs and 18 data and parity pairs. The Q cable has 2 control signal pairs and 18 data and parity pairs.

SCSI ADDRESS	DB(31) DB(24)	DB(23) DB(16)	DB(15) DB(8)	DB(7) DB(0)	PRIORITY	
7	---- ----	---- ----	---- ----	1--- ----	1	HIGHEST
6	---- ----	---- ----	---- ----	-1-- ----	2	
5	---- ----	---- ----	---- ----	--1- ----	3	
4	---- ----	---- ----	---- ----	---1 ----	4	
3	---- ----	---- ----	---- ----	---- 1---	5	
2	---- ----	---- ----	---- ----	---- -1--	6	
1	---- ----	---- ----	---- ----	---- --1-	7	
0	---- ----	---- ----	---- ----	---- ---1	8	
15	---- ----	---- ----	1--- ----	---- ----	9	
14	---- ----	---- ----	-1-- ----	---- ----	10	
13	---- ----	---- ----	--1- ----	---- ----	11	
12	---- ----	---- ----	---1 ----	---- ----	12	
11	---- ----	---- ----	---- 1---	---- ----	13	
10	---- ----	---- ----	---- -1--	---- ----	14	
9	---- ----	---- ----	---- --1-	---- ----	15	
8	---- ----	---- ----	---- ---1	---- ----	16	
23	---- ----	1--- ----	---- ----	---- ----	17	
22	---- ----	-1-- ----	---- ----	---- ----	18	
21	---- ----	--1- ----	---- ----	---- ----	19	
20	---- ----	---1 ----	---- ----	---- ----	20	
19	---- ----	---- 1---	---- ----	---- ----	21	
18	---- ----	---- -1--	---- ----	---- ----	22	
17	---- ----	---- --1-	---- ----	---- ----	23	
16	---- ----	---- ---1	---- ----	---- ----	24	
31	1--- ----	---- ----	---- ----	---- ----	25	
30	-1-- ----	---- ----	---- ----	---- ----	26	
29	--1- ----	---- ----	---- ----	---- ----	27	
28	---1 ----	---- ----	---- ----	---- ----	28	
27	---- 1---	---- ----	---- ----	---- ----	29	
26	---- -1--	---- ----	---- ----	---- ----	30	
25	---- --1-	---- ----	---- ----	---- ----	31	
24	---- ---1	---- ----	---- ----	---- ----	32	LOWEST

BSY (BUSY). An "OR-tied" signal that indicates that the bus is being used.

SEL (SELECT). An "OR-tied" signal used by an initiator to select a target or by a target to reselect an initiator.

C/D (CONTROL/DATA). A signal sourced by a target that indicates whether control or data information is on the DATA BUS. True indicates CONTROL.

I/O (INPUT/OUTPUT). A signal sourced by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates INPUT to the initiator. In interlocked mode, this signal is also used to distinguish between SELECTION and RESELECTION phases.

MSG (MESSAGE). A signal sourced by a target to indicate the MESSAGE phase.

REQ (REQUEST). A signal sourced by a target on the P cable to indicate a request for a REQ/ACK data transfer handshake.

REQQ (REQUEST). A signal sourced by a target on the Q cable to indicate a request for a REQQ/ACKQ data transfer handshake.

ACK (ACKNOWLEDGE). A signal sourced by an initiator on the P cable to indicate an acknowledgment for a REQ/ACK data transfer handshake.

ACKQ (ACKNOWLEDGE). A signal sourced by an initiator on the Q cable to indicate an acknowledgment for a REQQ/ACKQ data transfer handshake.

ATN (ATTENTION). A signal sourced by an initiator which generates the attention event when asserted.

RST (RESET). An "OR-tied" signal that generates the RESET event when asserted.

DB(n,P) (DATA BUS). A data bit is defined as one when the signal is true, and defined as zero when the signal is false. Data parity shall be odd. Parity is undefined during the ARBITRATION phase. Bit significance and priority during arbitration are shown in Table 8.

DB(15-0,P,P1) (16-bit DATA BUS). Sixteen data-bit signals, plus two parity-bit signals that form the 16-bit DATA BUS. DB(P,P1) are parity bits for DB(7-0) and DB(15-8) respectively. The P cable carries these signals.

DB(31-0,P,P1,P2,P3) (32-bit DATA BUS). Thirty-two data-bit signals, plus four parity-bit signals that form the 32-bit DATA BUS. DB(P,P1,P2,P3) are parity bits for DB(7-0), DB(15-8), DB(23-16), and DB(31-24) respectively. The Q cable carries DB(31-16),DB(P2),DB(P3).

6.5.1 Signal Values

Signals may assume true or false values. There are two methods of driving these signals. In both cases, the signal shall be actively driven true, or asserted. In the case of OR-tied signals, the driver does not actively negate the signal. Rather the bias circuitry of the bus terminators pulls the signal false whenever it is released by the drivers at every SCSI device. If any driver is asserted, then the signal is true. In the case of non-OR-tied drivers, the signal may be actively driven false. In this standard, wherever the term negated is used, it means that the signal may be actively driven false, or may be simply released (in which case the bias circuitry pulls it false), at the option of the implementor. The advantage to actively negating signals false during information transfer is that the transition from true to false occurs more quickly and the noise margin is much higher than if the signal is simply released. This facilitates reliable data transfer at high rates, especially at the longer cable lengths used with differential drivers.

6.5.2 OR-Tied Signals

The BSY, SEL, and RST signals shall be OR-tied only. In the ordinary operation of the bus, the BSY and RST signals may be simultaneously driven true by several drivers. No signals other than BSY, RST, and DB(P) are simultaneously driven by two or more drivers, and any signal other than BSY, SEL, and RST may employ OR-tied or non-OR-tied drivers. Parity bits shall not be driven false during the ARBITRATION phase but may be driven false in other phases. There is no operational problem in mixing OR-tied and non-OR-tied drivers on signals other than BSY and RST.

6.5.3 Signal Sources

Table 6 indicates which type of SCSI device is allowed to source each signal. No attempt is made to show if the source is driving asserted, driving negated, or is passive. All SCSI device drivers that are not active sources shall be in the passive state. The RST signal may be asserted by any SCSI device at any time.

Table 6: Signal Sources

Bus Phase	P Cable Signals					Q Cable Signals		
	BSY	SEL	C/D, I/O, MSG, REQ	ACK, ATN	DB(15-0) DB(P)	REQQ	ACKQ	DB(31-16) DB(P2) DB(P3)
BUS FREE	None	None	None	None	None	None	None	None
ARBITRATION	All	Win	None	None	S ID	None	None	S ID
SELECTION	I&T	Init	None	Init	Init	None	None	Init
RESELECTION	I&T	Targ	Targ	Init	Targ	None	None	Targ
COMMAND	Targ	None	Targ	Init	Init?	None	None	None
DATA IN	Targ	None	Targ	Init	Targ	Targ	Init	Targ
DATA OUT	Targ	None	Targ	Init	Init	Targ	Init	Init
STATUS	Targ	None	Targ	Init	Targ?	None	None	None
MESSAGE IN	Targ	None	Targ	Init	Targ?	None	None	None
MESSAGE OUT	Targ	None	Targ	Init	Init?	None	None	None

All: The signal shall be driven by all SCSI devices that are actively arbitrating.

S ID: A unique data bit (the SCSI ID) shall be driven by each SCSI device that is actively arbitrating; the other seven data bits shall be released (i.e., not driven) by this SCSI device. The parity bit (DB(P)) may be released or driven to the true state, but shall never be driven to the false state during this phase.

I&T: The signal shall be driven by the initiator, target, or both, as specified in the SELECTION phase and RESELECTION phase.

Init: If driven, this signal shall be driven only by the active initiator.

None: The signal shall be released; that is, not be driven by any SCSI device. The bias circuitry of the bus terminators pulls the signal to the false state.

Win: The signal shall be driven by the one SCSI device that wins arbitration.

Targ: If the signal is driven, it shall be driven only by the active target.

7 SCSI Parallel Bus Timing

Unless otherwise indicated, the delay-time measurements for each SCSI device, shown in Table 7, shall be calculated from signal conditions existing at that SCSI device's own SCSI bus connection. Thus, these measurements (except cable skew delay) can be made without considering delays in the cable. The timing characteristics of each signal are described in the following paragraphs. The timing specifications in this section may be applied to SCSI-2 A cables.

Table 7: SCSI Bus Timing Values

Timing Description	Megatransfer Rate Five	Ten
Arbitration Delay	2.4 us	
Assertion Period	80 ns	30 ns
Bus Clear Delay	800 ns	
Bus Free Delay	800 ns	
Bus Set Delay	1.8 us	
Bus Settle Delay	400 ns	
Cable Skew Delay (note 2)	4 ns	
Data Release Delay	400 ns	
Negation Period	80 ns	30 ns
Receive Hold Time (note 3)	22 ns	
Receive Setup Time (note 3)	12 ns	
Receiver Delay Skew (notes 1,2)	6 ns	
Reset Hold Time	25 us	
Selection Abort Time	200 us	
Selection Time-out Delay (note 1)	250 ms	
System Deskew Delay	45 ns	20 ns
Transfer Period	200-1020 ns	100-196 ns
Transmit Hold Time (note 3)	35 ns	
Transmit Setup Time (note 3)	25 ns	
Transmitter Delay Skew (notes 1,2)	6 ns	

Notes:
1) This is a recommended time. It is not mandatory.
2) This time does not apply at the SCSI device connectors.
3) See Annex C for examples of how to calculate setup and hold timing for SCSI protocol chips.

7.1 Arbitration Delay

The minimum time an SCSI device shall wait from asserting BSY for arbitration until the DATA BUS can be examined to see if arbitration has been won. There is no maximum time.

7.2 Assertion Period

The minimum time that a target shall assert REQ (or REQQ) while using synchronous data transfers. Also, the minimum time that an initiator shall assert ACK (or ACKQ) while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.3 Bus Clear Delay

The maximum time for an SCSI device to stop driving all bus signals after:

1) The BUS FREE phase is detected (BSY and SEL both false for a bus settle delay)
2) SEL is received from another SCSI device during the ARBITRATION phase
3) The transition of RST to true.

For the first condition above, the maximum time for an SCSI device to clear the bus is 1200 nanoseconds from BSY and SEL first becoming both false. If an SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall clear the bus within a bus clear delay minus the excess time.

7.4 Bus Free Delay

The minimum time that an SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of BSY when going to the ARBITRATION phase.

7.5 Bus Set Delay

The maximum time for an SCSI device to assert BSY and its SCSI ID bit on the DATA BUS after it detects BUS FREE phase (BSY and SEL both false for a bus settle delay) for the purpose of entering the ARBITRATION phase.

7.6 Bus Settle Delay

The minimum time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

7.7 Cable Skew Delay

The maximum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices.

7.8 Data Release Delay

The maximum time for an initiator to release the DATA BUS signals following the transition of the I/O signal from false to true.

7.9 Negation Period

The minimum time that a target shall negate REQ (or REQQ) while using synchronous data transfers. Also, the minimum time that an initiator shall negate ACK (or ACKQ) while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.10 Receive Hold Time

The minimum time required by the receiving device between the assertion of REQ (or REQQ) or ACK (or ACKQ) and the changing of the data lines while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.11 Receive Setup Time

The minimum time required by the receiving device between the changing of data lines and the assertion of REQ (or REQQ) or ACK (or ACKQ) while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.12 Receiver Delay Skew

When receivers outside the SCSI protocol chip are used, this is the maximum propagation delay time difference between any two receivers on the REQ, ACK, DATA or PARITY signals of the same cable when the receivers have the same power supply voltage and are operating within 5 degrees Centigrade of one another (ambient temperature). This is a component specification, not a SCSI device specification, and is used to estimate the remaining skew budget for protocol chips.

7.13 Reset Hold Time

The minimum time for which RST is asserted. There is no maximum time.

7.14 Selection Abort Time

The maximum time that a target (or initiator) shall take from its most recent detection of being selected (or reselected) until asserting a BSY response. This time-out is required to ensure that a target (or initiator) does not assert BSY after a SELECTION (or RESELECTION) phase has been aborted. This is not the selection time-out period; see 8.1.3.1 and 8.1.4.2 for a complete description.

7.15 Selection Time-out Delay

The minimum time that an initiator (or target) should wait for a BSY response during the SELECTION (or RESELECTION) phase before starting the time-out procedure. Note that this is only a recommended time period.

7.16 System Deskew Delay

The minimum time that a device should wait after receiving a SCSI signal to ensure any signals transmitted at the same time are valid.

7.17 Transmit Hold Time

The minimum time provided by the transmitting device between the assertion of REQ (or REQQ) or ACK (or ACKQ) and the changing of the data lines while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.18 Transmit Setup Time

The minimum time provided by the transmitting device between the changing of data lines and the assertion of REQ (or REQQ) or ACK (or ACKQ) while using synchronous data transfers. REQQ and ACKQ timings only apply to optional wide data transfers.

7.19 Transmitter Delay Skew

When drivers outside the SCSI protocol chip are used, this is the maximum propagation delay time difference between any two drivers on the REQ, ACK, DATA or PARITY signals of the same cable when the drivers have the same power supply voltage and are operating within 5 degrees Centigrade of one another (ambient temperature). This is a component specification, not a SCSI device specification, and is used to estimate the remaining skew budget for protocol chips.

7.20 Transfer Period

The Transfer Period specifies the minimum time allowed between the leading edges of successive REQ pulses and of successive ACK pulses while using synchronous data transfers (see 8.1.6.2). When devices negotiate a synchronous data transfer period of less than 200 nanoseconds they are said to be using "fast synchronous data transfer". These devices use timing parameters specified in the right hand column of Table 7. Devices which negotiate a synchronous data transfer period greater than or equal to 200 nanoseconds use timing parameters specified in the left hand column of Table 7. When fast synchronous data transfers are agreed upon, fast timing must be observed even though the actual data transfer period is greater than or equal to 200ns. The minimum synchronous data transfer period is 100 nanoseconds.

8 SCSI Parallel Bus Logical Characteristics

8.1 SCSI Parallel Bus Events and Phases

The SCSI architecture includes three events and nine phases:

ATTENTION Event
RESET Event
DISCONNECT Event

BUS FREE phase
ARBITRATION phase
SELECTION phase
RESELECTION phase
SETUP phase
COMMAND phase
DATA phase
STATUS phase
MESSAGE phase.

The COMMAND, DATA, STATUS, and MESSAGE phases are referred to collectively as information transfer phases.

The SCSI bus can never be in more than one phase at any given time. In the following descriptions, signals that are not mentioned shall not be asserted.

8.1.1 BUS FREE Phase

The BUS FREE phase is used to indicate that no SCSI device is actively using the SCSI bus and that it is available.

SCSI devices shall detect the BUS FREE phase after the SEL and BSY signals are both continuously false for at least a bus settle delay. When an SCSI device in initiator mode detects the BUS FREE phase it shall generate a Disconnect Event. The SCSI-3 Interlocked Protocol interprets this event as either expected or unexpected.

SCSI devices shall release all SCSI bus signals within a bus clear delay after the BSY and SEL signals become continuously false for a bus settle delay. If an SCSI device requires more than a bus settle delay to detect the BUS FREE phase then it shall release all SCSI bus signals within a bus clear delay minus the excess time to detect the BUS FREE phase. The total time to clear the SCSI bus shall not exceed a bus settle delay plus a bus clear delay.

8.1.2 ARBITRATION Phase

The ARBITRATION phase allows one SCSI device to gain control of the SCSI bus so that it can initiate or resume an I/O process.

The procedure for an SCSI device to obtain control of the SCSI bus is as follows:

1) The SCSI device shall first wait for the BUS FREE phase to occur. The BUS FREE phase is detected whenever both the BSY and SEL signals are simultaneously and continuously false for a minimum of a bus settle delay.

   This bus settle delay is necessary because a transmission line phenomenon known as a "wired-OR glitch" may cause the BSY signal to briefly appear false, even though it is being asserted.

2) The SCSI device shall wait a minimum of a bus free delay after detection of the BUS FREE phase (i.e. after the BSY and SEL signals are both false for a bus settle delay) before driving any signal.

3) Following the bus free delay in Step (2), the SCSI device may arbitrate for the SCSI bus by asserting both the BSY signal and its own SCSI ID, however the SCSI device shall not arbitrate (i.e. assert the BSY signal and its SCSI ID) if more than a bus set delay has passed since the BUS FREE phase was last observed.

   There is no maximum delay before asserting the BSY signal and the SCSI ID following the bus free delay in Step (2) as long as the bus remains in the BUS FREE phase. However, SCSI devices that delay longer than a bus settle delay plus a bus set delay from the time when the BSY and SEL signals first become false may fail to participate in arbitration when competing with faster SCSI devices.

4) After waiting at least an arbitration delay (measured from its assertion of the BSY signal) the SCSI device shall examine the DATA BUS. If a higher priority SCSI ID bit is true on the DATA BUS (DB(7) is the highest), then the SCSI device has lost the arbitration and the SCSI device may release its signals and return to Step (1). If no higher priority SCSI ID bit is true on the DATA BUS, then the SCSI device has won the arbitration and it shall assert the SEL signal. Any SCSI device other than the winner has lost the arbitration and shall release the BSY signal and its SCSI ID bit within a bus clear delay after the SEL signal becomes true. An SCSI device that loses arbitration may return to Step (1).

   Any device shall complete the arbitration to the point of SEL being asserted if it begins the arbitration phase as stated in step (3). This precludes the possibility of the bus being hung. It is recommended that new implementations wait for the SEL signal to become true before releasing the BSY signal and SCSI ID bit when arbitration is lost.

5) The SCSI device that wins arbitration shall wait at least a bus clear delay plus a bus settle delay after asserting the SEL signal before changing any signals.

   The SCSI ID bit is a single bit on the DATA BUS that corresponds to the SCSI device's unique SCSI address. All other DATA BUS bits shall be released by the SCSI device. Parity is not valid during the ARBITRATION phase. During the ARBITRATION phase, DB(Px) may be released or asserted, but shall not be actively negated.

8.1.3 SELECTION Phase

SCSI targets or target-mode ports shall respond to SELECTION in interlocked mode, packetized mode, or both modes.

8.1.3.1 SELECTION Phase, Interlocked Mode

In interlocked mode, the SELECTION phase allows an initiator to select a target for the purpose of initiating some target function (e.g., READ or WRITE command). During the SELECTION phase the I/O signal is negated so that this phase can be distinguished from the RESELECTION phase.

The SCSI device that won the arbitration has both the BSY and SEL signals asserted and has delayed at least a bus clear delay plus a bus settle delay before ending the ARBITRATION phase. In interlocked mode, the SCSI device that won the arbitration becomes an initiator by not asserting the I/O signal.

The initiator shall set the DATA BUS to a value which is the OR of its SCSI ID bit and the target's SCSI ID bit and it shall assert the ATN signal (indicating that a MESSAGE OUT phase is to follow the SELECTION phase). The initiator shall then wait at least two system deskew delays and release the BSY signal. Minimally, the initiator shall drive all DATA BUS bytes containing the two SCSI ID bits plus any lower DATA BUS bytes. All parity bits associated with these bytes shall also be driven. Optionally, the initiator may drive its entire implemented DATA BUS width. In this case, all associated parity bits shall be driven. The initiator shall then wait at least a bus settle delay before looking for a response from the target.

The target shall determine that it is selected when the SEL signal and its SCSI ID bit are true and the BSY and I/O signals are false for at least a bus settle delay. The selected target may examine the DATA BUS in order to determine the SCSI ID of the selecting initiator. The selected target shall then assert the BSY signal within a selection abort time of its most recent detection of being selected; this is required for correct operation of the selection time-out procedure.

The SCSI device shall check parity as indicated in the table that follows.

Check for odd parity on:	If at least one bit is active on:
DB(7-0),P	DB(31-0,P1,P2,P3,P4)
DB(15-8),P1	DB(31-8,P1,P2,P3)
DB(23-16),P2	DB(31-16,P2,P3)
DB(31-24),P3	DB(31-16,P2,P3)

These rules are necessary to permit interoperation of devices with different bus widths. For example, if a 16-bit device selects a 32-bit device, the 32-bit device will observe invalid parity on the upper 16 bits of the data bus.

The SCSI device shall not respond to SELECTION or RESELECTION phases if one or more of the following occur:

a) No SCSI ID bits are true on any of the DATA BUS bytes
b) Bad parity is detected on one or more DATA BUS bytes

c) More than two SCSI ID bits are true on the DATA BUS
d) In the case of SELECTION phase, no SCSI ID bits are true on bits DB(7-0) and there are less than two SCSI ID bits true on the remaining bits of the DATA BUS. In the case of RESELECTION phase, there are other than two SCSI ID bits true on the DATA BUS.

The target shall not respond to a selection if bad parity is detected. Also, if more than two SCSI ID bits are on the DATA BUS, the target shall not respond to selection.

No less than two system deskew delays after the initiator detects the BSY signal is true, it shall release the SEL signal and the initiator may change the DATA BUS (see SETUP phase). The target shall wait until the SEL signal is false before asserting the REQ signal to enter an information transfer phase.

8.1.3.2 SELECTION Phase, Packetized-Mode

In packetized mode, the SELECTION phase allows an initiator-mode port to select a target-mode port for the purpose of transferring information packet(s) via a DATA OUT phase.

The initiator-mode port has both the BSY and SEL signals asserted and has delayed at least a bus clear delay plus a bus settle delay before ending the ARBITRATION phase. The initiator-mode port shall negate the I/O signal and shall set the DATA BUS to a value which is the OR of its SCSI ID bit and the SCSI ID bit of the target-mode port. The initiator-mode port shall negate the ATN signal, indicating the DATA OUT phase is to be the first information transfer phase. The initiator-mode port shall then wait at least two system deskew delays and release the BSY signal. Minimally, the initiator-mode port shall drive all DATA BUS bytes containing the two SCSI ID bits plus any lower DATA BUS bytes. All parity bits associated with these bytes shall also be driven. Optionally, the initiator-mode port may drive its entire implemented DATA BUS width. In this case, all associated parity bits shall be driven. The initiator-mode port shall then wait at least a bus settle delay before looking for a response from the target-mode port.

The target-mode port shall determine that it is selected when the SEL signal and its SCSI ID bit are true and the BSY and I/O signals are false for at least a bus settle delay. The target-mode port may examine the DATA BUS in order to determine the SCSI ID of the initiator-mode port. The target-mode port shall then assert the BSY signal within a selection abort time of its most recent detection of being selected; this is required for correct operation of the selection time-out procedure.

The target-mode port shall not respond to a selection if bad parity is detected. Also, if more than two SCSI ID bits are on the DATA BUS, the target-mode port shall not respond to selection.

No less than two system deskew delays after the initiator-mode port detects the BSY signal is true, it shall release the SEL signal and the initiator-mode port may change the DATA BUS (see SETUP phase). The target-mode port shall wait until the SEL signal is false before asserting the REQ signal to enter an information transfer phase.

8.1.3.3 SELECTION Time-out Procedure

The SELECTION time-out procedure applies to both packetized and interlocked modes, except where noted. In this section, the terms "initiator" and "target" are synoymous with the packetized terms "initiator-mode port" and "target-mode port", respectively.

Two optional selection time-out procedures are specified for clearing the SCSI bus if the initiator waits a minimum of a selection time-out delay and there has been no BSY signal response from the target:

1) Optionally, the initiator shall assert the RST signal;
2) Optionally, the initiator shall continue asserting the SEL signal and shall release the data bus. In interlocked mode the initiator shall also continue asserting the ATN signal. If the initiator has not detected the BSY signal to be true after at least a selection abort time plus two system deskew delays, the initiator shall release the SEL and ATN signals allowing the SCSI bus to go to the BUS FREE phase. Targets shall ensure that when responding to selection that the selection was still valid within a selection abort time of their assertion of the BSY signal. Failure to comply with this requirement could result in an improper selection (two targets connected to the same initiator, wrong target connected to an initiator, or a target connected to no initiator).

8.1.4 RESELECTION Phase

RESELECTION is an optional phase for devices in interlocked mode that allows a target to reconnect to an initiator for the purpose of continuing some I/O process that was previously started by the initiator but was suspended by the target, (i.e., the target disconnected by allowing a BUS FREE phase to occur before the I/O process was complete). Devices in packetized mode do not implement RESELECTION phase.

8.1.4.1 RESELECTION

Upon completing the ARBITRATION phase, the winning SCSI device has both the BSY and SEL signals asserted and has delayed at least a bus clear delay plus a bus settle delay. The winning SCSI device becomes a target by asserting the I/O signal. The winning SCSI device shall also set the DATA BUS to a value that is the logical OR of its SCSI ID bit and the initiator's SCSI ID bit. Minimally, the target shall drive all DATA BUS bytes containing the two SCSI ID bits plus any lower DATA BUS bytes. All parity bits associated with these bytes shall also be driven. Optionally, the target may drive its entire implemented DATA BUS width. In this case, all associated parity bits shall be driven. The target shall wait at least two system deskew delays and release the BSY signal. The target shall then wait at least a bus settle delay before looking for a response from the initiator.

The initiator shall determine that it is reselected when the SEL and I/O signals and its SCSI ID bit are true and the BSY signal is false for at least a bus settle delay. The reselected initiator may examine the DATA BUS in order to determine the SCSI ID of the reselecting target. The reselected initiator shall then assert the BSY signal within a selection abort time of its most recent detection of being reselected; this is required for correct operation of the time-out procedure. The initiator shall not respond to a RESELECTION phase if bad parity is detected. Also, the initiator shall not respond to a RESELECTION phase if other than two SCSI ID bits are on the DATA BUS.

After the target detects the BSY signal is true, it shall also assert the BSY signal and wait at least two system deskew delays and then release the SEL signal. The target may then change the I/O signal and the DATA BUS. After the reselected initiator detects the SEL signal is false, it shall release the BSY signal. The target shall continue asserting the BSY signal until it relinquishes the SCSI bus.

When the target is asserting the BSY signal, a transmission line phenomenon known as a "wired-OR glitch" may cause the BSY signal to appear false for up to a round-trip propagation delay following the release of the BSY signal by the initiator. This is the reason why the BUS FREE phase is recognized only after both the BSY and SEL signals are continuously false for a minimum of a bus settle delay. Cables longer than 25 meters should not be used even if the chosen driver, receiver, and cable provide adequate noise margins, because they increase the duration of the glitch and could cause SCSI devices to inadvertently detect the BUS FREE phase.

8.1.4.2 RESELECTION Time-out Procedure

Two optional RESELECTION time-out procedures are specified for clearing the SCSI bus during a RESELECTION phase if the target waits a minimum of a selection time-out delay and there has been no BSY signal response from the initiator:

1) Optionally, the target shall assert the RST signal;
2) Optionally, the target shall continue asserting the SEL and I/O signals and shall release all DATA BUS signals. If the target has not detected the BSY signal to be true after at least a selection abort time plus two system deskew delays, the target shall release the SEL and I/O signals allowing the SCSI bus to go to the BUS FREE phase. SCSI devices that respond to the RESELECTION phase shall ensure that the reselection was still valid within a selection abort time of their assertion of the BSY signal. Failure to comply with this requirement could result in an improper reselection (two initiators connected to the same target or the wrong initiator connected to a target).

8.1.5 SETUP Phase

The SETUP phase is the phase between:

a) SELECTION phase and the first information transfer phase,
b) RESELECTION phase and the first information transfer phase,
c) any two information transfer phases,
d) the last information transfer phase and BUS FREE.

At the end of SELECTION or RESELECTION phase, the target shall wait until the SEL signal is false before entering the SETUP phase.

Each information transfer phase transitions to the SETUP phase when the target changes the C/D, I/O, or MSG signals.

8.1.6 Information Transfer Phases

Information transfers on the DATA BUS follow a defined REQ/ACK handshake protocol which is asynchronous for COMMAND, STATUS, and MESSAGE phases. One or two byte(s) of information may be transferred with each handshake on the P cable. DATA phases operate asynchronously by default, but also have a synchronous data transfer option.

The COMMAND, DATA, STATUS, and MESSAGE phases are all grouped together as the information transfer phases because they are all used to transfer data or control information via the DATA BUS. The actual content of the information is beyond the scope of this standard.

The information transfer phases use one or more REQ/ACK handshakes to control the information transfer. Each REQ/ACK handshake allows the transfer of a maximum of one word of information. During the information transfer phases the BSY signal shall remain true and the SEL signal shall remain false. Additionally, during the information transfer phases, the target shall continuously envelope the REQ/ACK handshake(s) with the C/D, I/O, and MSG signals in such a manner that these control signals are valid for a bus settle delay before the assertion of the REQ signal of the first handshake and remain valid until after the negation of the ACK signal at the end of the handshake of the last transfer of the phase.

The C/D, I/O, and MSG signals are used to distinguish between the different information transfer phases (see Table 9). The target drives these three signals and therefore controls all changes from one phase to another. In interlocked mode, the initiator can request a MESSAGE OUT phase by asserting the ATN signal, while the target can cause the BUS FREE phase by releasing the MSG, C/D, I/O, and BSY signals.

After the negation of the ACK signal of the last transfer of the phase, the target may prepare for a new phase by asserting or negating the C/D, I/O, and MSG signals. These signals may be changed together or individually. They may be changed in any order and may be changed more than once. It is desirable that each line change only once.

An initiator is allowed to anticipate a new phase based on:

a) the previous phase,
b) the expected new phase, and
c) early information provided by changes in the C/D, I/O, and MSG signals.

However, the anticipated phase is not valid until the REQ signal is asserted at the beginning of the next phase.

Table 8: Information Transfer Phases

Signal				
MSG	C/D	I/O	Phase Name	Direction of Transfer
0	0	0	DATA OUT	Initiator to Target or Initiator-mode port to Target-mode port
0	0	1	DATA IN	Initiator from Target
0	1	0	COMMAND	Initiator to Target
0	1	1	STATUS	Initiator From Target
1	0	0	*	
1	0	1	*	
1	1	0	MESSAGE	Initiator to Target
1	1	1	MESSAGE IN	Initiator from Target
Key: 0=False, 1=True, *=Reserved for future standardization				

8.1.6.1 Asynchronous Information Transfer

The target shall control the direction of information transfer by means of the I/O signal. When the I/O signal is true, information shall be transferred from the target to the initiator. When the I/O signal is false, information shall be transferred from the initiator to the target.

If the I/O signal is true (transfer to the initiator), the target shall first drive the DB(7-0,P) signals to their desired values, delay at least one transmit setup time, then assert the REQ signal. The DB(7-0,P) signals shall remain valid until the ACK signal is true at the target. The initiator shall read the DB(7-0,P) signals after the REQ signal is true, then indicate its acceptance of the data by asserting the ACK signal. When the ACK signal becomes true at the target, the target may change or release the DB(7-0,P) signals and shall negate the REQ signal. After the REQ signal is false the initiator shall then negate the ACK signal. After the ACK signal is false the target may continue the transfer by driving the DB(7-0,P) signals and asserting the REQ signal, as described above.

If the I/O signal is false (transfer to the target) the target shall request information by asserting the REQ signal. The initiator shall drive the data and parity signals to their desired values, delay at least one transmit hold time and assert the ACK signal. The initiator shall continue to drive the data and parity signals until the REQ signal is false. When the ACK signal becomes true at the target, the target shall read the data and parity signals then negate the REQ signal. When the REQ signal becomes false at the initiator, the initiator may change or release the data and parity signals and shall negate the ACK signal. The target may continue the transfer by asserting the REQ signal, as described above.

8.1.6.2 Synchronous Data Transfer

Synchronous data transfer is optional and is only used in data phases. It shall be used in a data phase if a synchronous data transfer agreement has been established (see SCSI-3 Interlocked Protocol document). The agreement specifies the REQ/ACK offset and the minimum transfer period.

The REQ/ACK offset specifies the maximum number of REQ pulses that can be sent by the target in advance of the number of ACK pulses received from the initiator, establishing a pacing mechanism. If the number of REQ pulses exceeds the number of ACK pulses by the REQ/ACK offset, the target shall not assert the REQ signal until after the leading edge of the next ACK pulse is received. A requirement for successful completion of the data phase is that the number of ACK and REQ pulses be equal.

The target shall assert the REQ signal for a minimum of an assertion period. The target shall then wait at least the greater of a transfer period from the last transition of the REQ signal to true or a minimum of a negation period from the last transition of the REQ signal to false before again asserting the REQ signal.

The initiator shall send one pulse on the ACK signal for each REQ pulse received. The ACK signal may be asserted as soon as the leading edge of the corresponding REQ pulse has been received. The initiator shall assert the ACK signal for a minimum of an assertion period. The initiator shall wait at least the greater of a transfer period from the last transition of the ACK signal to true or for a minimum of a negation period from the last transition of the ACK signal to false before asserting the ACK signal.

If the I/O signal is true (transfer to the initiator), the target shall first drive the data and parity signals to their desired values, wait at least one transmit setup time, then assert the REQ signals. The data and parity signals shall be held valid for a minimum of one transmit hold time after the assertion of the REQ signal. The target shall assert the REQ signal for a minimum of an assertion period. The target may then negate the REQ signal and change or release the data and parity signals. The initiator shall read the value on the data and parity signals within one receive hold time of the transition of the REQ signal to true. The initiator shall then respond with an ACK pulse.

If the I/O signal is false (transfer to the target), the initiator shall transfer one byte for each REQ pulse received. After receiving the leading edge of a REQ pulse, the initiator shall first drive the data and parity signals to their desired values, delay at least one transmit setup time, then assert the ACK signal. The initiator shall hold the data and parity signals valid for at least one transmit hold time after the assertion of the ACK signal. The initiator shall assert the ACK signal for a minimum of an assertion period. The initiator may then negate the ACK signal and may change or release the data and parity signals. The target shall read the value of the data and parity signals within one receive hold time of the transition of the ACK signal to true.

Some implementors have presumed that the leading edge of the first REQ pulse beyond the REQ/ACK offset agreement would not occur until after the trailing edge of the last ACK pulse within the agreement. Devices implemented with this understanding may be subject to data loss when in synchronous data

transfer mode with devices that issue the leading edge of the next REQ pulse, at the boundary of the agreement, as soon as the leading edge of the last ACK pulse within the agreement is received. Implementors of initiators attaching such devices may ensure data integrity by restricting the synchronous offset agreement to values smaller than the maximum nominally offered by their device.

8.1.6.3 Wide Data Transfer

Wide data transfer is optional and may be used in the DATA phase only if a nonzero wide data transfer agreement is in effect. The messages determine the use of wide mode by both SCSI devices and establish a data path width to be used during the DATA phase.

Wide data transfers of 16- or 32-bits may be established. Although not mandatory, it is recommended that targets and initiators that support 32-bit wide transfers also support 16-bit wide transfers. All SCSI devices shall support 8-bit data transfers.

During 16-bit wide data transfers, the first and second logical data bytes for each data phase shall be transferred across the DB(7-0,P) and DB(15-8,P2) signals on the P cable. Subsequent pairs of data bytes are likewise transferred in parallel across the P cable (see Figure 9).

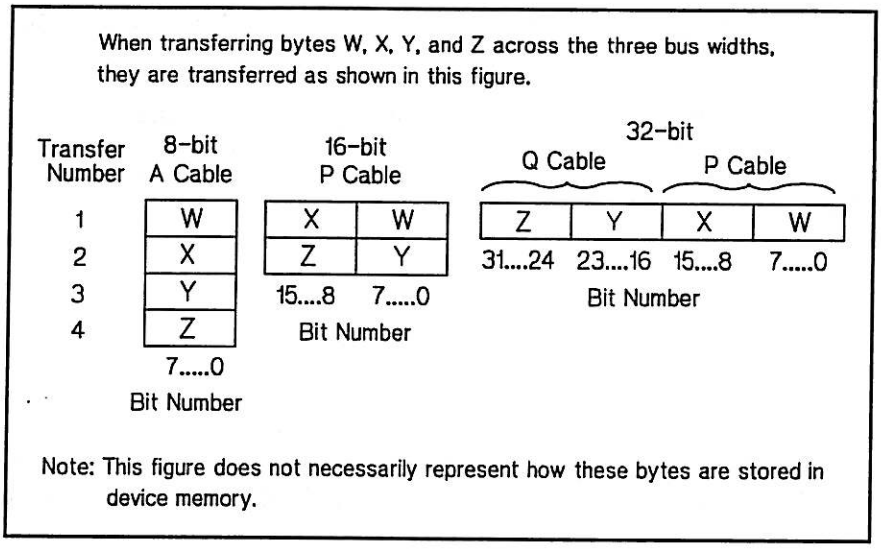


Figure 9: Wide SCSI Byte Ordering

During 32-bit wide data transfers on a P/Q cabled system, the first and second logical data bytes for each data phase shall be transferred across the DB(7-0,P) and DB(15-8,P2) signals, respectively, on the P cable, and the third and fourth logical data bytes shall be transferred across the DB(23-16,P2) and DB(31-24,P3) signals, respectively, on the Q cable. Subsequent pairs of data bytes are likewise transferred in parallel across the P and Q cables (see Figure 9).

If the last data byte transferred for a command does not fall on the DB(15- 8) signals for a 16-bit wide transfer or the DB(31-24) signals for a 32-bit wide transfer, then the values of the remaining higher-numbered bits are undefined. However, parity bits for these undefined bytes shall be valid for whatever data is placed on the bus.

On a P/Q cabled system to ensure proper data integrity, certain sequence requirements shall be met between the REQ/ACK handshakes on the P cable and the REQQ/ACKQ handshakes on the Q cable:

1) The REQQ and ACKQ signals shall only be asserted during data phases while a nonzero wide data transfer agreement is in effect. These signals shall not be asserted during other phases.

2) The same information transfer mode (asynchronous or synchronous) shall be used for both the P cable and the Q cable. If synchronous data transfer mode is in effect, the same REQ/ACK offset and transfer period shall be used for both cables.

3) The information transfer procedures defined in the ANSI SCSI-2 Standard X3.131-1991 sections 5.1.5.1 Asynchronous Information Transfer and 5.1.5.2 Synchronous Data Transfer for the P cable (the REQ, ACK, and DB(15-0,P,P1) signals) shall also apply to the Q cable (the REQQ, ACKQ, and DB(31-16,P2,P3) signals). The only means available for a target to manage the timing relationship between the signals on the two cables is its management of the REQ and REQQ signals. Similarly, the only means for the initiator to manage the timing between the two cables is its management of the ACK and ACKQ signals.

4) The target shall ensure that the number of REQ/ACK handshakes and the number of REQQ/ACKQ handshakes in a data phase are equal before it changes to another phase. The target shall not change the phase until the ACK and ACKQ signals have both become false for the last REQ/ACK handshake and the last REQQ/ACKQ handshake.

If any violations of these rules are detected by the target, the target may attempt to end the data phase and return CHECK CONDITION status. If it is impossible to correctly terminate the data phase, the target may abnormally terminate the I/O process by an unexpected disconnect. If any violations of these rules are detected by the initiator, the initiator may attempt to send an INITIATOR DETECTED ERROR message to the target. If the initiator is unable to terminate the I/O process normally, it may generate the reset condition.

8.1.7 COMMAND Phase

The COMMAND phase allows the target to request command information from the initiator.

The target shall assert the C/D signal and negate the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

8.1.8 Data Phase

The data phase is a term that encompasses both the DATA IN phase and the DATA OUT phase.

8.1.8.1 DATA IN Phase

The DATA IN phase allows the target to request that data be sent to the initiator from the target.

The target shall assert the I/O signal and negate the C/D and MSG signals during the REQ/ACK handshake(s) of this phase.

8.1.8.2 DATA OUT Phase

The DATA OUT phase allows the target to request that data be sent from the initiator to the target. This phase also allows a target-mode port to request that a packet be sent from the initiator-mode port to the target-mode port.

The target(-mode port) shall negate the C/D, I/O, and MSG signals during the REQ/ACK handshake(s) of this phase.

8.1.9 STATUS Phase

The STATUS phase allows the target to request that status information be sent from the target to the initiator.

The target shall assert the C/D and I/O signals and negate the MSG signal during the REQ/ACK handshake of this phase.

8.1.10 Message Phase

The message phase is a term that references either a MESSAGE IN, or a MESSAGE OUT phase. Multiple messages may be sent during either phase. The first byte transferred in either of these phases shall be either a single-byte message or the first byte of a multiple-byte message. Multiple-byte messages shall be wholly contained within a single message phase.

8.1.10.1 MESSAGE IN Phase

The MESSAGE IN phase allows the target to request that message(s) be sent to the initiator from the target.

The target shall assert the C/D, I/O, and MSG signals during the REQ/ACK handshake(s) of this phase.

8.1.10.2 MESSAGE OUT Phase

The MESSAGE OUT phase allows the target to request that message(s) be sent from the initiator to the target. The target invokes this phase in response to the attention condition created by the initiator (see 5.2.1).

The target shall assert the C/D and MSG signals and negate the I/O signal during the REQ/ACK handshake(s) of this phase. The target shall handshake byte(s) in this phase until the ATN signal is negated, except when rejecting a message.

If the target detects one or more parity error(s) on the message byte(s) received, it may indicate its desire to retry the message(s) by asserting the REQ signal after detecting the ATN signal has gone false and prior to changing to any other phase. The initiator, upon detecting this condition, shall re-send all of the previous message byte(s) in the same order as previously sent during this phase. When re-sending more than one message byte, the initiator shall assert the ATN signal at least two system deskew delays prior to asserting the ACK signal on the first byte and shall maintain the ATN signal asserted until the last byte is sent as described in 5.2.1.

The target may act on messages as received as long as no parity error is detected and may ignore all remaining messages sent under one ATN condition after a parity error is detected. When a sequence of messages is re-sent by an initiator because of a target detected parity error, the target shall not act on any message which it acted on the first time received.

If the target receives all of the message byte(s) successfully (i.e., no parity errors), it shall indicate that it does not wish to retry by changing to any information transfer phase other than the MESSAGE OUT phase and transfer at least one byte. The target may also indicate that it has successfully received the message byte(s) by changing to the BUS FREE phase (e.g., ABORT or BUS DEVICE RESET messages).

8.1.11 Signal Restrictions Between Phases

When the SCSI bus is between two information transfer phases, the following restrictions shall apply to the SCSI bus signals:

1) The BSY, SEL, REQ, REQB, ACK and ACKB signals shall not change.
2) The C/D, I/O, MSG, and DATA BUS signals may change. When switching the DATA BUS direction from out (initiator driving) to in (target driving), the target shall delay driving the DATA BUS by at least a data release delay plus a bus settle delay after asserting the I/O signal and the initiator shall release the DATA BUS no later than a data release delay after the transition of the I/O signal to true. When switching the DATA BUS direction from in (target driving) to out (initiator driving), the target shall release the DATA BUS no later than a system deskew delay after negating the I/O signal.
3) The ATN and RST signals may change as defined under the descriptions for the attention condition (see 5.2.1) and reset condition (see 5.2.2).

8.2 SCSI Bus Events

The SCSI bus has two asynchronous events which create SCSI Bus Conditions; the attention event creates the attention condition and the reset event creates the reset condition. These conditions cause the SCSI device to perform certain actions and can alter the phase sequence. The SCSI Interlocked and Protocols describe the reset and attention conditions more fully.

8.2.1 Attention Event

An attention event creates an attention condition which allows an initiator to inform a target that the initiator has a message ready. The target may get this message by performing a MESSAGE OUT phase.

The initiator creates an attention event by asserting ATN at any time except during the ARBITRATION or BUS FREE phases.

The initiator shall negate the ATN signal at least two system deskew delays before asserting the ACK signal while transferring the last byte of some messages specified in the SCSI-3 Interlocked Protocol standard. If the target detects that the initiator failed to meet this requirement, then the target shall go to BUS FREE phase.

The initiator shall assert the ATN signal at least two system deskew delays before negating the ACK signal for the last byte transferred in a bus phase for the attention condition to be honored before transition to

a new bus phase. Asserting the ATN signal later might not be honored until a later bus phase and then may not result in the expected action.

The initiator should only assert the ATN signal during a RESELECTION phase to transmit a BUS DEVICE RESET or DISCONNECT message. Other uses may result in ambiguities concerning the nexus.

The initiator shall keep the ATN signal asserted if more than one byte is to be transferred. The initiator may negate the ATN signal at any time except it shall not negate the ATN signal while the ACK signal is asserted during a MESSAGE OUT phase. Normally, the initiator negates the ATN signal while the REQ signal is true and the ACK signal is false during the last REQ/ACK handshake of the MESSAGE OUT phase.

8.2.2 Reset Event

The reset event creates a reset condition which is used to immediately clear all SCSI devices from the bus. This condition shall take precedence over all other phases and conditions. Any SCSI device may create the reset event by asserting the RST signal for a minimum of a reset hold time.

Any SCSI device may create the reset event by asserting the RST signal for a minimum of a Reset Hold Time. During the reset event, the state of all SCSI bus signals other than the RST signal is not defined.

All SCSI devices shall release all SCSI bus signals (except the RST signal) within a Bus Clear Delay of the transition of the RST signal to true. The BUS FREE phase always follows the reset event.

Environmental conditions (e.g., static discharge) may generate brief glitches on the RST signal. It is recommended that SCSI devices not react to these glitches. The manner of rejecting glitches is vendor specific. The Bus Clear Delay following a RST signal transition to true is measured from the original transition of the RST signal, not from the time that the signal has been confirmed. This limits the time to confirm the RST signal to a maximum of a Bus Clear Delay.

8.2.3 Disconnect Event

A disconnect event is generated when an SCSI device in initiator mode detects the BUS FREE phase. The SCSI-3 Interlocked Protocol interprets this event as either expected or unexpected.

8.3 SCSI Parallel Bus Phase Sequences

The order in which phases are used on the SCSI bus follows a prescribed sequence.

The reset condition can abort any phase and is always followed by the BUS FREE phase. Also any other phase can be followed by the BUS FREE phase but many such instances are error conditions (see unexpected disconnect, 8.1.1).

The allowable sequences shall be as shown in tables 14, 15, and 16. The normal progressions are:

Interlocked mode:
BUS FREE
ARBITRATION
SELECTION (ATN true) or RESELECTION
SETUP
Information Transfer (COMMAND,DATA,STATUS,MESSAGE)
SETUP
BUS FREE

Packetized mode:
BUS FREE
ARBITRATION
SELECTION (ATN false)
SETUP
DATA OUT
SETUP
BUS FREE

In interlocked mode, the final information transfer phase is normally the MESSAGE IN phase where a DISCONNECT, or COMMAND COMPLETE message is transferred, followed by the BUS FREE phase.

Table 9: Phase Transitions, Interlocked Mode

TO Phase / FROM Phase	BUS FREE	ARB	SEL ATN true	RESEL	SETUP	MSG OUT	CMD	DATA IN	DATA OUT	STATUS	MSG IN
BUS FREE		X									
ARBITRATION	X		X	X							
SELECTION (ATN true)	X				X						
RESELECTION	X				X						
SETUP	X				X	X	X	X	X	X	X
MESSAGE OUT	X				X						
COMMAND	X				X						
DATA IN or DATA OUT	X				X						
STATUS	X				X						
MESSAGE IN	X				X						

An 'X' denotes an allowable phase transition.

The allowable set of Information Transfer Phase-SETUP Phase-Information Transfer Phase sequences are shown in Table 10.

Table 10: Information Phase Transitions, Interlocked Mode

TO SETUP followed by FROM Phase	MSG OUT	CMD	DATA IN or OUT	STATUS	MSG IN
MESSAGE OUT OUT		X	X	X	X
COMMAND	X		X	X	X
DATA IN or — DATA OUT	X			X	X
STATUS	X				X
MESSAGE IN	X	X	X	X	

An 'X' denotes an allowable phase transition.

Table 11: Phase Transitions, Packetized Mode

TO Phase FROM Phase	BUS FREE	ARB	SEL (ATN false)	SETUP	DATA OUT
BUS FREE		X			
ARBITRATION	X		X		
SELECTION (ATN false)	X			X	
SETUP	X				X
DATA OUT	X			X	

An 'X' denotes an allowable phase transition

Annex A - Interconnecting Buses of Different Widths

(normative)

When connectors of dissimilar width are adapted to one another as shown in Figure 10, the DATA BUS signals from the wider of the two buses which end at the adapter shall be terminated at the adapter. The connectors are designed such that A and P shielded connectors will not intermate directly.

Two of the RESERVED lines (A cable contact numbers 23 and 24) and the OPEN line (A cable contact number 25) on the A cable are TERMPWR lines on the P cable (P cable contact numbers 33, 34, and 35).

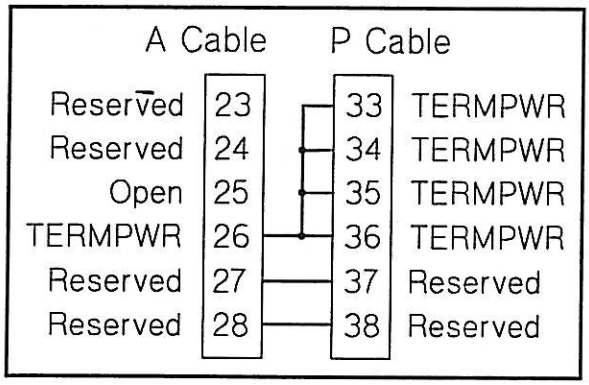


Figure 10: Interconnecting A and P Cables

8 bit devices which connected to the single-ended P-cable shall leave the following 9 signals open: DB(8-15),DB(P1).

8 bit devices which connected to the differential P-cable shall leave the following 18 signals open: +DB(15-8),-DB(15-8),+DB(P1),-DB(P1).

Annex B - Cabling and Cable Measurement Method Recommendations
(informative)

B.1 Cabling

To minimize discontinuities and signal reflections, cables of different impedances should not be used in the same bus. Implementations may require trade-offs in shielding effectiveness, cable length, the number of loads, transfer rates, and cost to achieve satisfactory system operation. To minimize discontinuities due to local impedance variation, a flat cable should be spaced at least 1.27 mm (0.050 in) from other cables, any other conductor, or the cable itself when the cable is folded. Also, use of 26AWG wire in .050" pitch flat cable will more closely match impedances of many round shielded cables, resulting in fewer impedance discontinuities and therefore improved signal quality.

When mixing devices of different widths, particular care should be taken to not to exceed the skew allowances provided by the cable skew delay and the system deskew delay. These timing parameters can be lowered by reducing SCSI device input capacitance, SCSI device stub length, and the number of SCSI devices attached to the bus. The same precautions should be taken on buses with single-ended devices using fast synchronous data transfers in order to maintain system integrity.

B.2 Cable Measurement

The following test procedures are recommended for measuring cable parameters. In addition to the referenced standards, Single-Ended measurements are made between the signal wire of the pair under test and the ground wire of all pairs connected to the shield.

B.2.1 Impedance, TDR, Single-Ended

TBD

B.2.2 Impedance, TDR, Differential

TBD

B.2.3 Impedance, Network Analyzer, Single-Ended

Per ASTM D-4566.

B.2.4 Impedance, TDR, Differential

Per ASTM D-4566.

B.2.5 Attenuation, Single-Ended

Per ASTM D-4566.

B.2.6 Attenuation, Differential

Per ASTM D-4566

B.2.7 Velocity (Propagation Delay) and Skew

TBD

B.2.8 DC Resistance

Per ASTM D-4566

Annex C - Setup and Hold Timing
(informative)

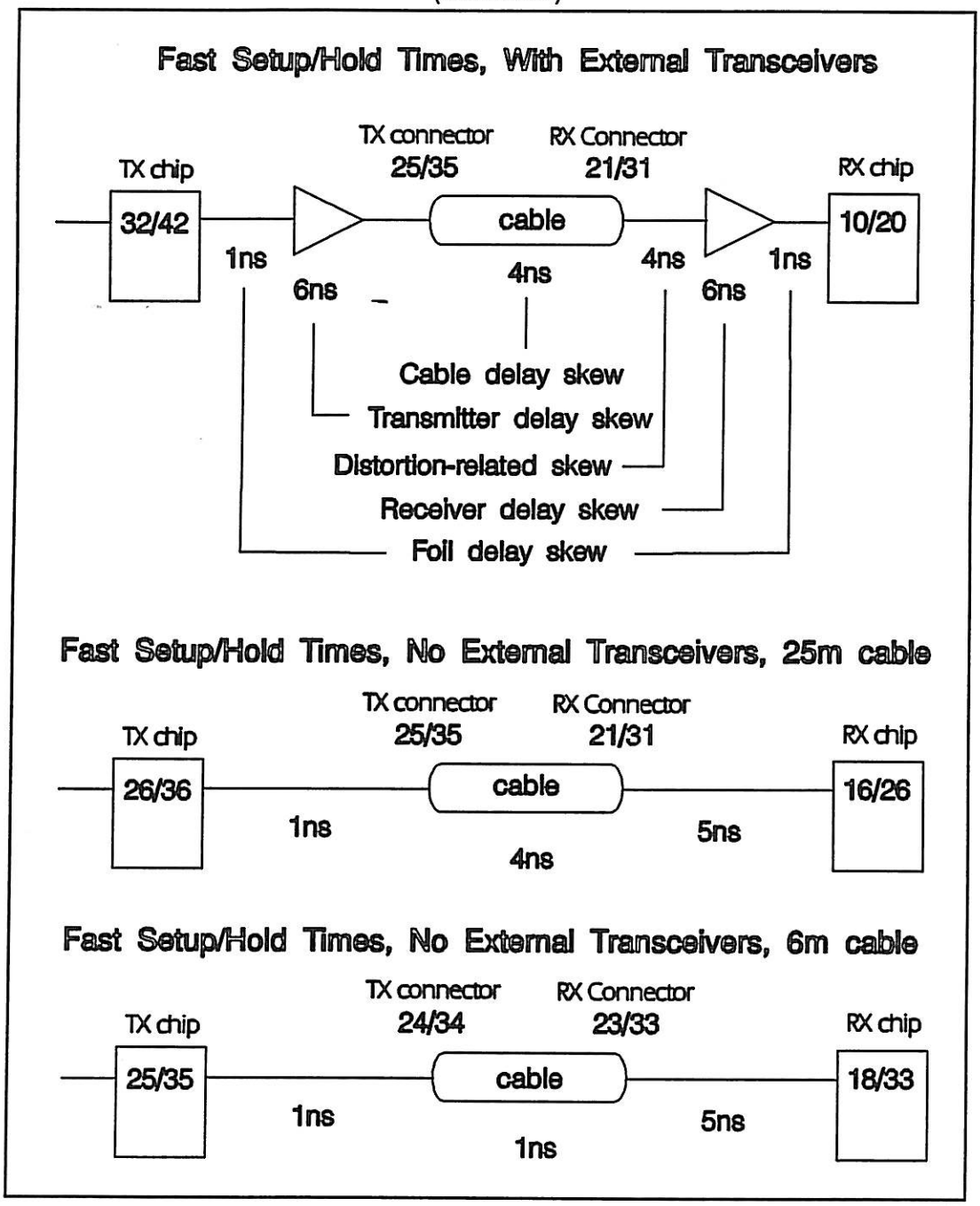


Figure 11: Setup and Hold Timing Examples

Figure 11 shows how the setup and hold times are calculated for various physical configurations. SCSI timing is specified at the SCSI connectors. To calculate the setup and hold timings for SCSI protocol chips, the following examples are provided.

In systems with external transceivers, the total skew budget is 27ns. A 5ns tolerance is allowed for system use (e.g., cable mismatch, jitter, repeaters).

Transmitter chip	32 setup/43 hold	
Foil	1ns	
External driver	6ns (recommended)	
-------- TX connector -------		
25 meter cable	4ns	
Distortion	4ns	27ns
Tolerance	5ns	
-------- RX connector -------		
External Receiver	6ns	
Foil	1ns	
Receiver chip	5 setup/15 hold	

At its connector, the transmitting SCSI device must:

1) drive data no less than 25ns before asserting REQ/ACK, and
2) must keep that data valid for no less than 35ns following the assertion of REQ/ACK.

The receiving device shall be able to latch the data at its connector when:

1) data is valid no more than 12ns prior to the assertion of REQ/ACK, and
2) when data is valid no more than 22ns following the assertion of REQ/ACK.

When 7ns is added to the transmit device timing for transmitter skew and skew due to foil delays, the transmitting SCSI chip setup and hold timings are 32ns and 42ns, respectively. Similarly, when 11ns is subtracted from the skew budget of the recieving device, 5ns and 15ns are left for receive chip setup and hold, respectively.

In the case of fast timing with no external transceivers over a 25m cable, the total skew budget is 15ns, compared to 27ns. The 12ns difference is used to relax the timing at the SCSI devices (6ns for the transmitting device, and 6ns for the receiving device).

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END OF DOCUMENT

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