X3T9.2/90-190

DT: 11/30/90
TO: ATA Plannary
FM: Conner Peripherals
RE: Requested changes to the ATA specification.

As Conner has stated repeatedly in the past in order to maintain backwards compatibility with past ATA drives, which from an industry standpoint we feel is very important, Conner is requesting the following changes to the specification.

1. Dual Drive Detection Scheme

Slave present will only be used for backward compatibility. It will remain on pin 39.

At POR on reset -PDIAG will be activated by the slave within 1 ms. If the master does not see -PDIAG active after 4 ms it will assume no slave is present. -PDIAG will remain active until the slave is ready to go not busy or 14.0 seconds on a POR on reset. The master will wait 14.5 seconds or until the slave deactivates -PDIAG on POR on reset before it goes not busy. The slave will de-activate -PDIAG and go not busy, if it is not ready after the 14.0 seconds. Neither drive will set ready or seek complete until they have reached full spin speed and are ready to read and write.

During a software reset, -PDIAG will be activated by the slave within 1 ms. If the master does not see -PDIAG active after 4 ms it will assume no slave is present. The slave will not de-activate -PDIAG until it is ready to go not busy or 400 ms. The master will only wait 450 ms or until the slave de-activates -PDIAG before it goes not busy. Neither the master or the slave will set ready and seek complete until those states are achieved.

After power on time, -PDIAG will be used for the diagnostic command. Some system BIOS timing requires that after a software reset, the drive must be ready within 500 ms. However, the 1 ms time to determine slave present on the drive subsystem, the 4 ms timeout to determine slave present, and the 15 second time to wait for both drives active may be changed since they were arbitrarily chosen and have no known timing requirements.

2. Updating of task file between blocks.

Conner feels that the updating of the task file between blocks should be required since in the ATA interface

commands can be aborted at anytime. Even in the middle of the execution of the command. If this feature of the ATA interface is used then the updating of the task file aids in the computers ability to remember where it was. The argument that some drives in the future may not be able to update the task file quick enough for the computer does not seem to be a viable argument for doing away with what every drive has been able to do in the past. Another reason is that there are diagnostic tests for drives that require that the task file update as expected.

3. Change to what a reset does to cache and multiple commands.

Since resets are commom place in some bios it has been requested that resets do not change the state of the cache or the read multiple commands. So at power up time the cache and multiple commands should default to on for the cache and off for the multiple commands. But after power up the states of cache and multiple commands do not return to their default condition after a reset. The purpose of this is so that after every reset the host is not required to go through and reissue every set up command that has happened preceding the reset.

4. The number of default ECC bytes.

Conner feels that each drive should have its own default number of ECC bytes that is already returned in the drive ID command. The reasons for this are that most bios' have the number of ECC bytes hard coded in the drive type table. If we are required to change to a default other than this table value the computer bios' would then be required either overhaul their existing bios structure or to support two identical drive types for the same drive. The second reason is that most of the common ATA support chips like the CL260 and the AIC6060 do not support an easy way of switching between different number of ECC bytes being transferred. So these parts would be unable to be used as CAM standard parts until they are revised. Thus causing hardware problems for companies trying to switch their drives to CAM compatible drives.

5. Inconsistant pin out with EISA.

The following pins are not compatible with the EISA standard.
Pin 27 IOCHRDY for CAM DACK for EISA
Pin 29 DACK for CAM DRQ for EISA

Pin 21 DRQ for CAM DMAEN for EISA

6. DMA is inaccurately described in the specification?