HEWLETT PACKARD
Roseville Networks Division
8000 Foothills Blvd., Roseville, CA 95678

Date: 17 Oct 90 X3T9.2/90-159R0
From: Kurt Chan, X3T9.2 Principal, Hewlett-Packard
To: X3T9.2 Membership
Subject: REQ/ACK signal quality and Fast Single-ended

New implementations of two old concepts may make Fast single-ended reliable using conventional cable technology. The two concepts are:

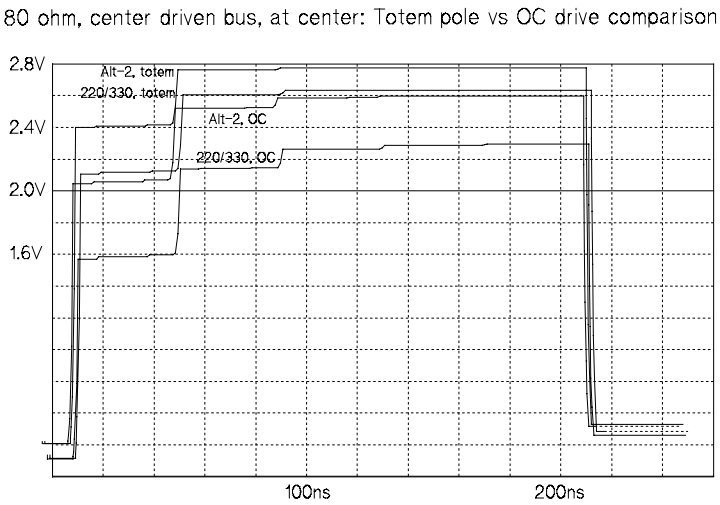
1. Active deassertion (see 4.6.1)
2. Increased hysteresis

ACTIVE DEASSERTION

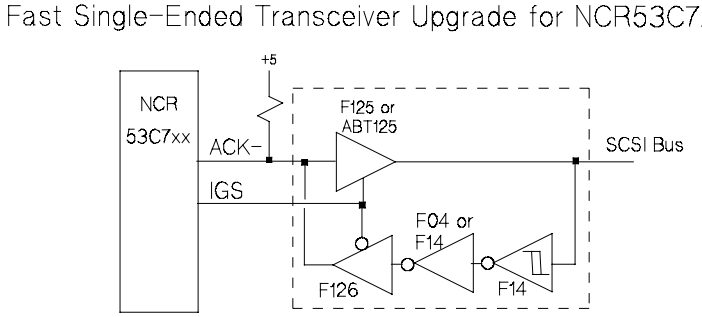
The first improvement involves adding 3-state totem-pole outputs to the speed-critical lines. The SPICE plot below shows the behavior of a very simplistic model of an active pullup circuit. Note the significant improvement in the amplitude of the critical first step of a SCSI bus waveform:

The parameters used were: bus length of 25', driven and viewed from center, cable attenuation = .095dB/m, 4.25V TERMPWR. In order of best to worst performance (based on initial step voltage) the four cases are:

1. Alt-2 termination with 15mA/48mA totem-pole outputs
2. 220/330@4.25V termination with 15mA/48mA totem-pole outputs
3. Alt-2 termination with open-collector outputs
4. 220/330@4.25V termination with open-collector outputs



The control circuitry needed to accomodate active deassertion is identical to that of differential. To breadboard this using VLSI with low-true open-collector outputs (such as the NCR53C700/710 chips):



If our objective is only to "clean up" existing applications, just applying this circuit to:

- REQ (for target-only HW)
- ACK (for initiator-only HW), or
- Both REQ and ACK (for devices which can be either initiators or targets)

is probably sufficient. To experiment with Fast Single-Ended, the Data+Parity lines should also undergo this transformation.

To confirm this idea, I captured some 10MHz waveforms on a 5 meter and 30.4 meter (100') SCSI cable using a variety of drivers. Thevenin termination was used. The Thevenin resistance was 100 ohms, and two Thevenin voltages were used: 2.83V and 2.20V. The drivers used were:

Driver Type	I(oh)	I(ol)	Comments
ALS641	n/a	24mA	Open Collector, weak pulldown
F641	n/a	64mA	Open Collector, strong pulldown
ALS1245	15mA	16mA	Totem-pole, weak pulldown
ALS640	15mA	24mA	Totem-pole, weak pulldown
ABTF245	32mA	64mA	Designed for fast transition times
F1245	15mA	64mA	Standard F-series buffer output
F640	15mA	64mA	Standard F-series buffer output

The following scope traces show characteristic waveforms for each of these drivers. Note that different output stage designs are used within the same logic family depending on the function of the component, which may account for slight differences in the waveforms.

OBSERVATIONS:

1. The average V(high) (3.6V) and peak-peak voltages (3.8V) for the totem-pole devices were at least 50% higher than open-collector devices, measured at both ends and at different terminating voltages.

2. RMS voltages, indicating the amount of energy delivered to the transmission system, were higher for totem-pole devices by more than 50%.

3. Totem-pole devices are much less susceptible than open-collector devices to drops in the terminating voltage. V(high) for open-collector devices dropped .89V per volt drop in the termination voltage compared to only .29V per volt for totem-pole devices.

4. The best totem pole devices have been observed driving 30.4 meters (100') of 28AWG flat ribbon cable at 10MHz very cleanly to 3.20V, measured at the **far** end, with about 5ns of rise time degradation. This was with suboptimal termination (100 ohms pulled up to 2.20V). Using the more conventional voltage of 2.62V to 100 ohms yielded an additional 100mV on the V(rms) and V(high) values.

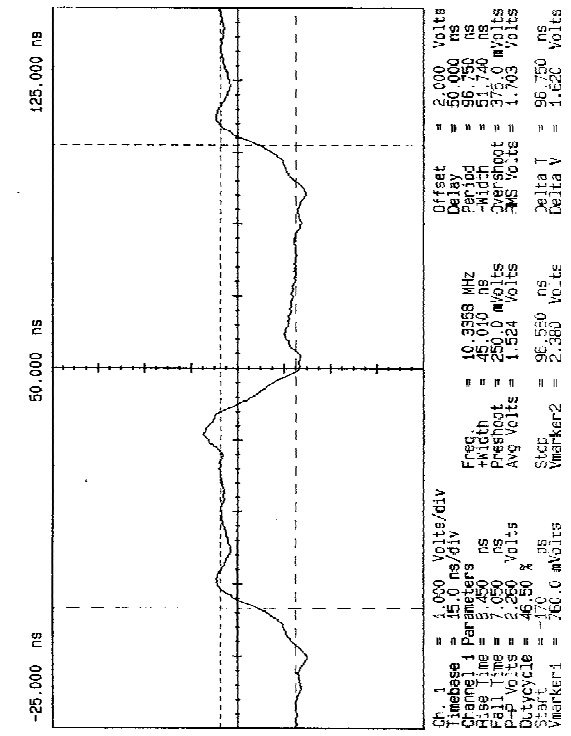


Figure 4 - ALS641 (24mA OC)

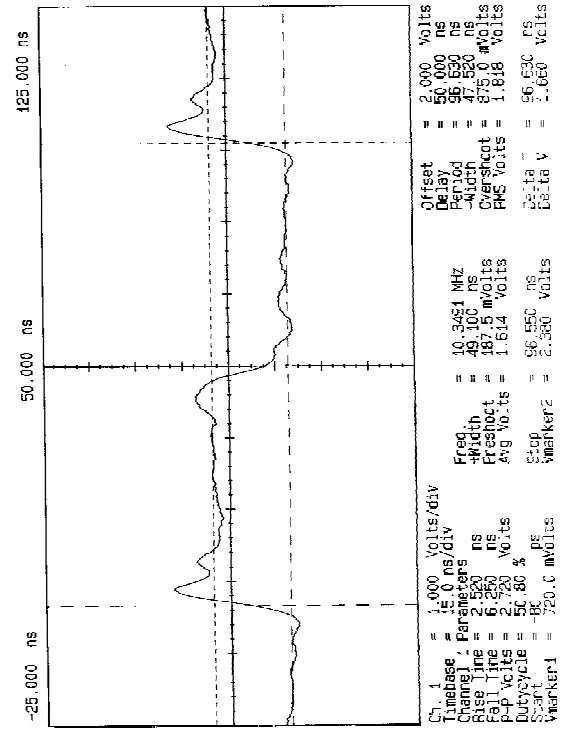


Figure 5 - F641 (64mA OC)

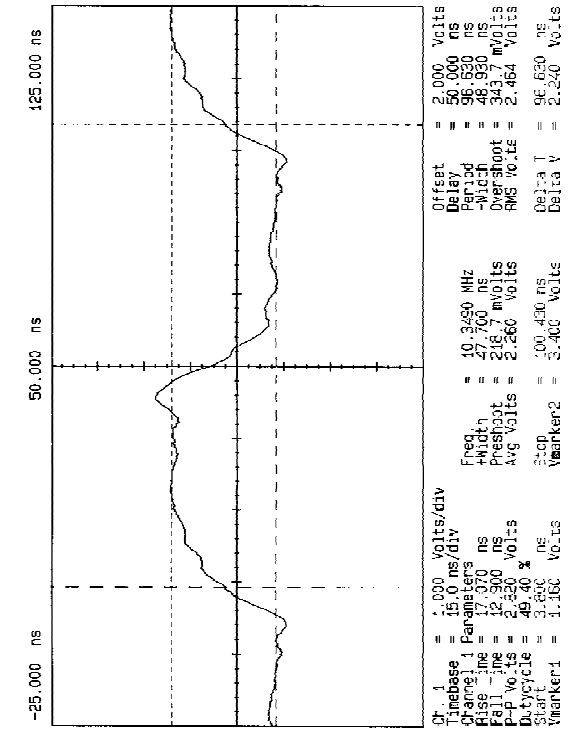


Figure 6 - ALS1245 (-15mA Ioh, 16mA Iol)

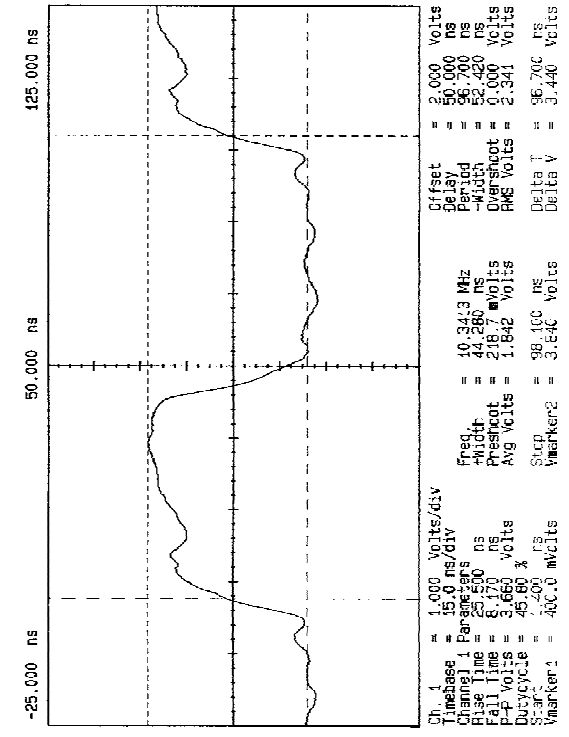


Figure 7 - ALS640 (-15mA Ioh, 24mA Iol)

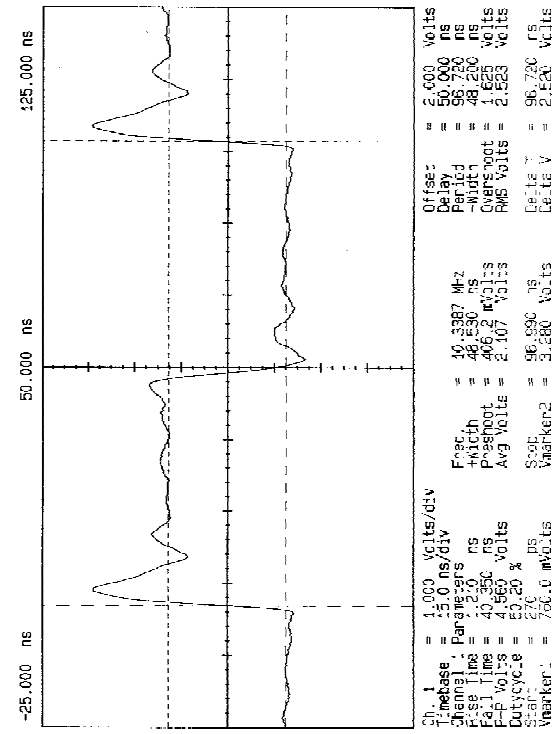


Figure 8 - ABT245 (-32mA Ioh, 64mA Iol)

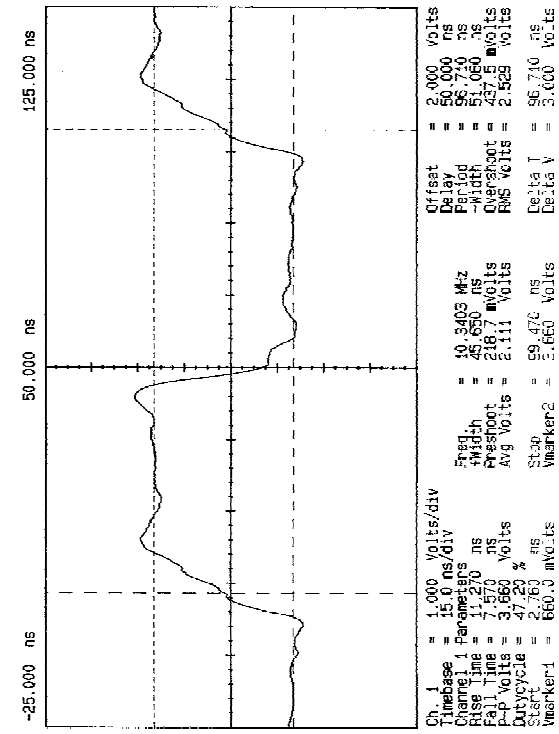


Figure 9 - F1245 (-15mA Ioh, 64mA Iol)

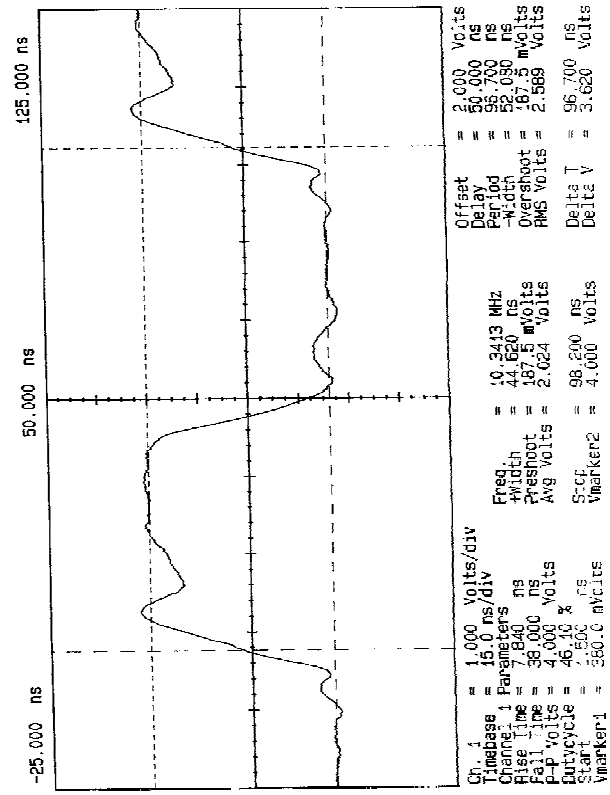


Figure 10 - F640 (-15mA Ioh, 64mA Iol)

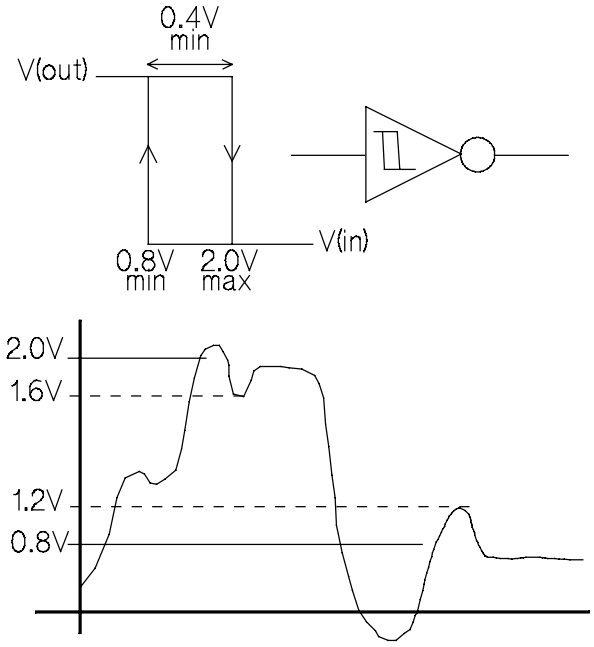
INCREASED HYSTERESIS

While active deassertion is a means of changing the drivers to drive the bus more cleanly, increasing hysteresis is a method of allowing receivers to ignore inadequate drivers and noise due to other system components:

The effect of hysteresis is that any noise discontinuity must be greater than the amplitude of the hysteresis in order to cause a false trigger. By doubling the hysteresis specification, we are doubling the immunity of systems to such disturbances.

The SCSI-2 specification calls for 0.2V of hysteresis. However, it is rare to find any modern TTL or CMOS Schmitt trigger devices with less than 0.4V of hysteresis as a minimum (0.8V typical). I suggest that we adopt the 0.4V minimum specification to increase noise immunity of single-ended devices. This can be a requirement of devices which receive Fast single-ended signals, or a general recommendation for all new devices.

When designing hysteresis circuits, the amount of hysteresis must not exceed the threshold window.
With a 2.0-0.8 = 1.2V window on SCSI, a typical 0.8V value for hysteresis still allows 0.4V before a threshold is violated. These margins are apparently controllable for most modern digital logic family processes.



SUMMARY

1. Active deassertion is an effective and compatible means of improving signal quality, at least equivalent to the improvement seen by adopting active termination. I suggest that VLSI designers consider actively deasserting at least the REQ and ACK lines using their built-in drivers. For those wishing to experiment with Fast single-ended, the data and parity lines should also undergo this treatment.

2. Further testing may reveal that 16-bit Fast single-ended is reliable when Alt-2 termination is used in conjunction with active deassertion and cable working group recommendations (80 ohms, low-loss, etc).

3. Worst-case package power dissipation will not increase significantly. 11 drivers all driving 48mA low at 0.5V dissipate .26W. The same 11 drivers all driving 3V@15mA with VDD=5.25V will dissipate .37W; an increase of less than 1/8 Watt. Note, however, that all of the pullup current comes from local VDD. Devices supporting wider and faster buses should expect to upgrade their power supplies.

4. Increasing input hysteresis to 0.4V aligns SCSI-3 with modern IC technology and doubles immunity to discontinuities between the low and high input thresholds. SCSI-2 requires 0.2V as a **minimum** not a maximum, so interoperability isn't sacrificed.

5. I expect to use the 16-bit P-connector components as a vehicle for future testing of Fast single-ended.