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Date: August 19, 1989
To: X3T9.2 SCSI Committee Members
From: Kurt Chan, Gordon Matheson
Subject: Shielded Cable Evaluation

The objectives of the tests described below were to:

1. Correlate cable parameters with data integrity and signal quality under worst-case conditions,
2. Demonstrate the compatibility of Alt1 (220/330) and Alt2 ("active") terminations.
3. Determine which Alt1/Alt2 terminator combinations are optimal with respect to low TERMPWR immunity, signal rise time, and signal fall time.

Four termination combinations were used in both tests:

1. Alternative 1 terminations at both ends ("Alt1-Alt1")
2. Alt1 terminations at the near (driver) end, Alt2 terminations at the far end ("Alt1-Alt2").
3. Alt 2 terminations at the near (driver) end and Alt 1 terminations at the far end ("Alt2-Alt1").
4. Alt 2 terminations at both ends ("Alt2-Alt2").

We tested 5 cables of varying vintage. Where possible, characteristics are listed for the specific wire pair we used in our test, as provided in test data supplied by some manufacturers to HP. The data supplied by the manufacturers are in the following units of measure:

- Z_0 is in differential ohms
- t_{pd} is in ns/ft, maximum
- Attenuation is in db/ft @ MHz, maximum, measured differentially
- Capacitance is in pF, conductor-to-conductor, maximum
- Resistance is in DC ohms/ft. maximum
- n/a indicates parameter was unavailable at time of publication

Cable	AWM Style	Pair	Z0	t(pd)	Attenuation	C	R
A	2960	yel/red	105+-15	1.65	.06 @ 25	16	.070
B	n/a	gry/wht	108+-5	1.58	.08 @ 50	16	.070
C	2919	wht/red	120+-10	1.56	n/a	12.9	n/a
D	n/a	vio/wht	127.3	1.6	n/a	n/a	n/a
E	20276	yel/blu	130	1.39	.06 @ 50	10.7	n/a

For all combinations of five cables and four termination schemes, we measured:

1. Error rate sensitivity of the cables to low TERMPWR by lowering TERMPWR and measuring the voltage at which the first error occurred.
2. Settling time to 2.0V (rise time).
3. Settling time to 0.8V (fall time).

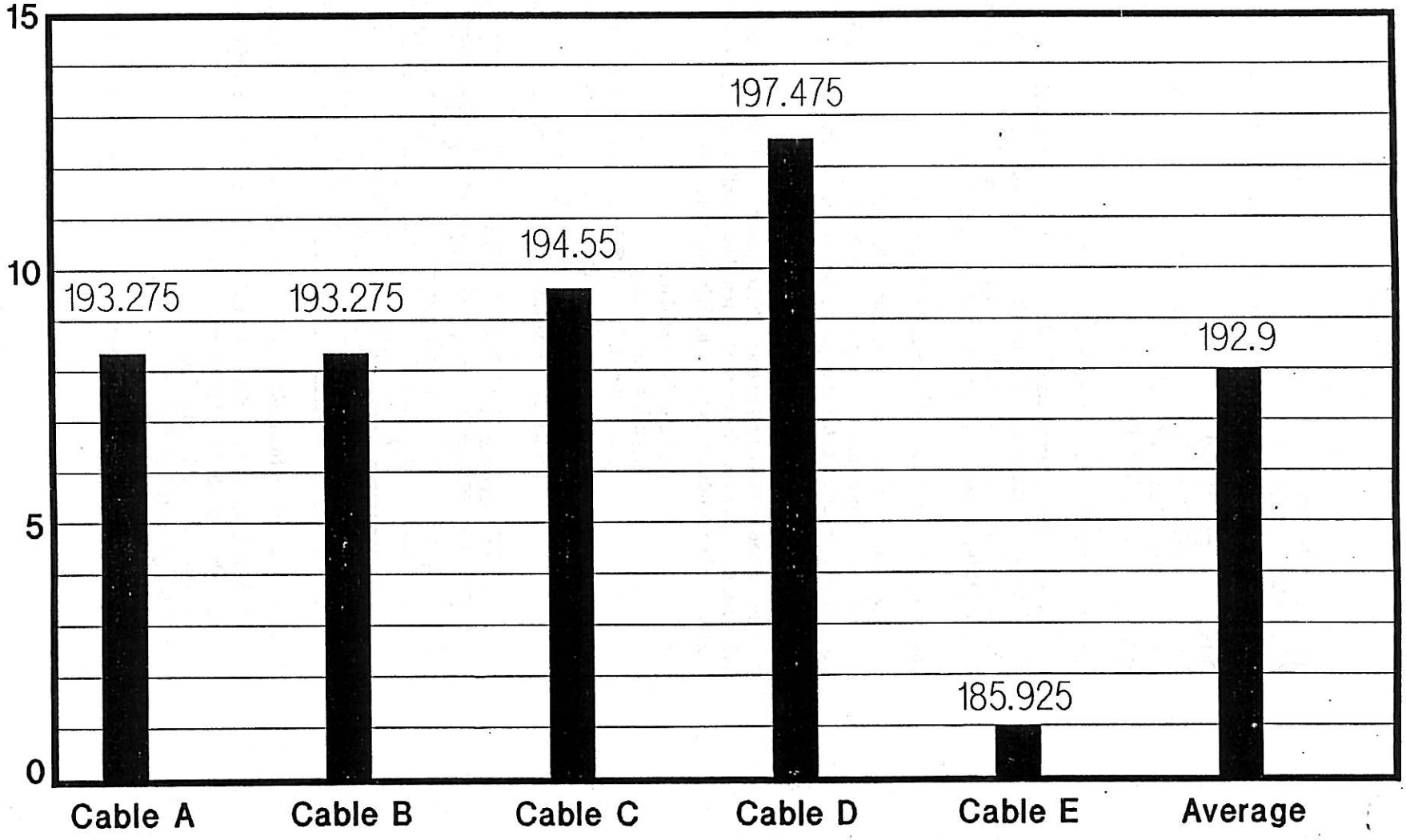
The results are summarized on the next four pages. A complete test description is given in an appendix.

HP Cable Comparison

Shielded, 5 MHz

Sum of avg settling times to 2.0V (relative nanoseconds)

(Sum of three device positions, each averaged over four termination schemes)



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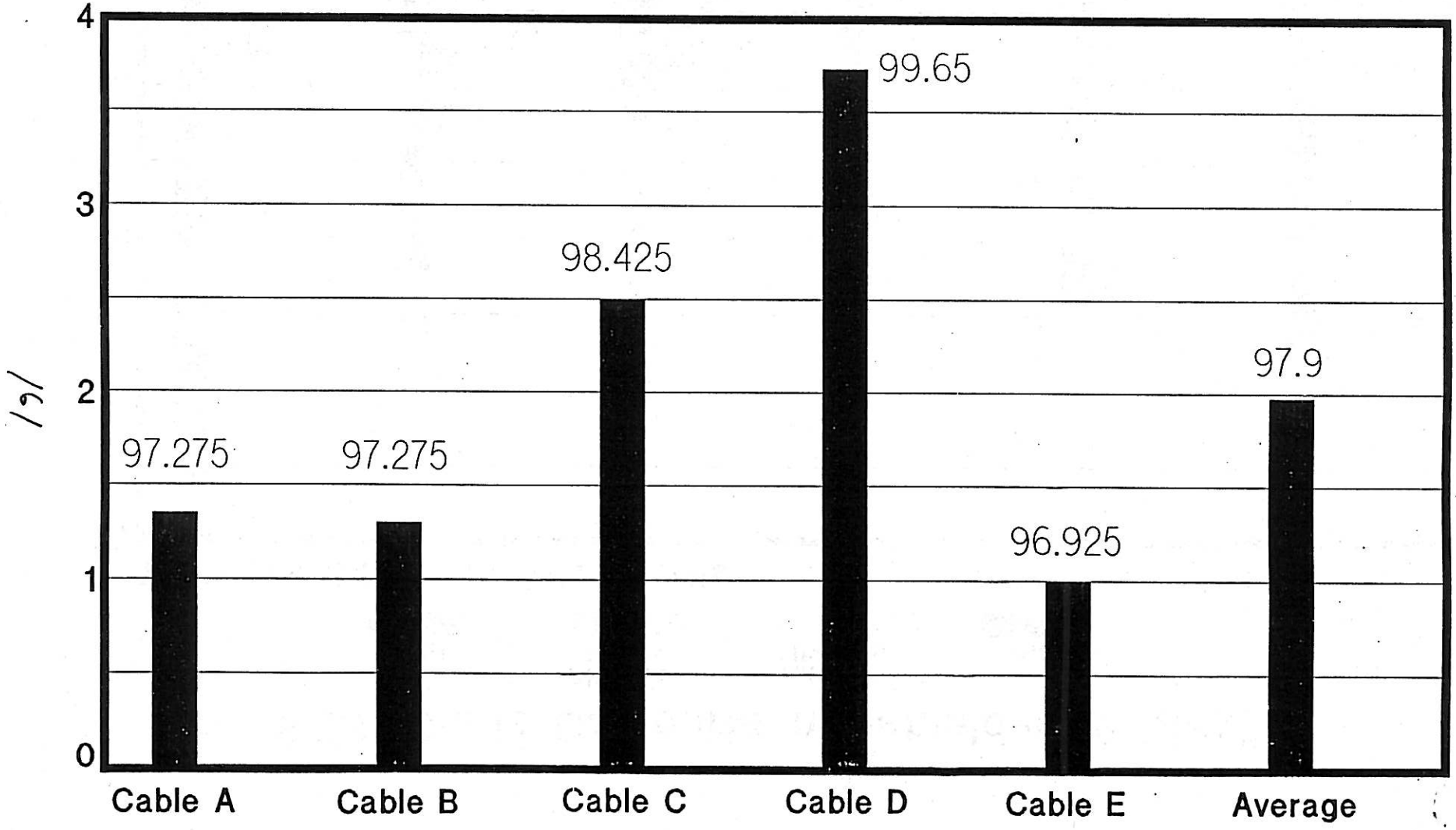
HP Cable Comparison

Shielded, 5 MHz

Sum of avg settling times to 0.8V (relative nanoseconds)

(Sum of three device positions, each averaged over four termination schemes)



SCSI Cable Comparisons (shielded, 5 MHz)

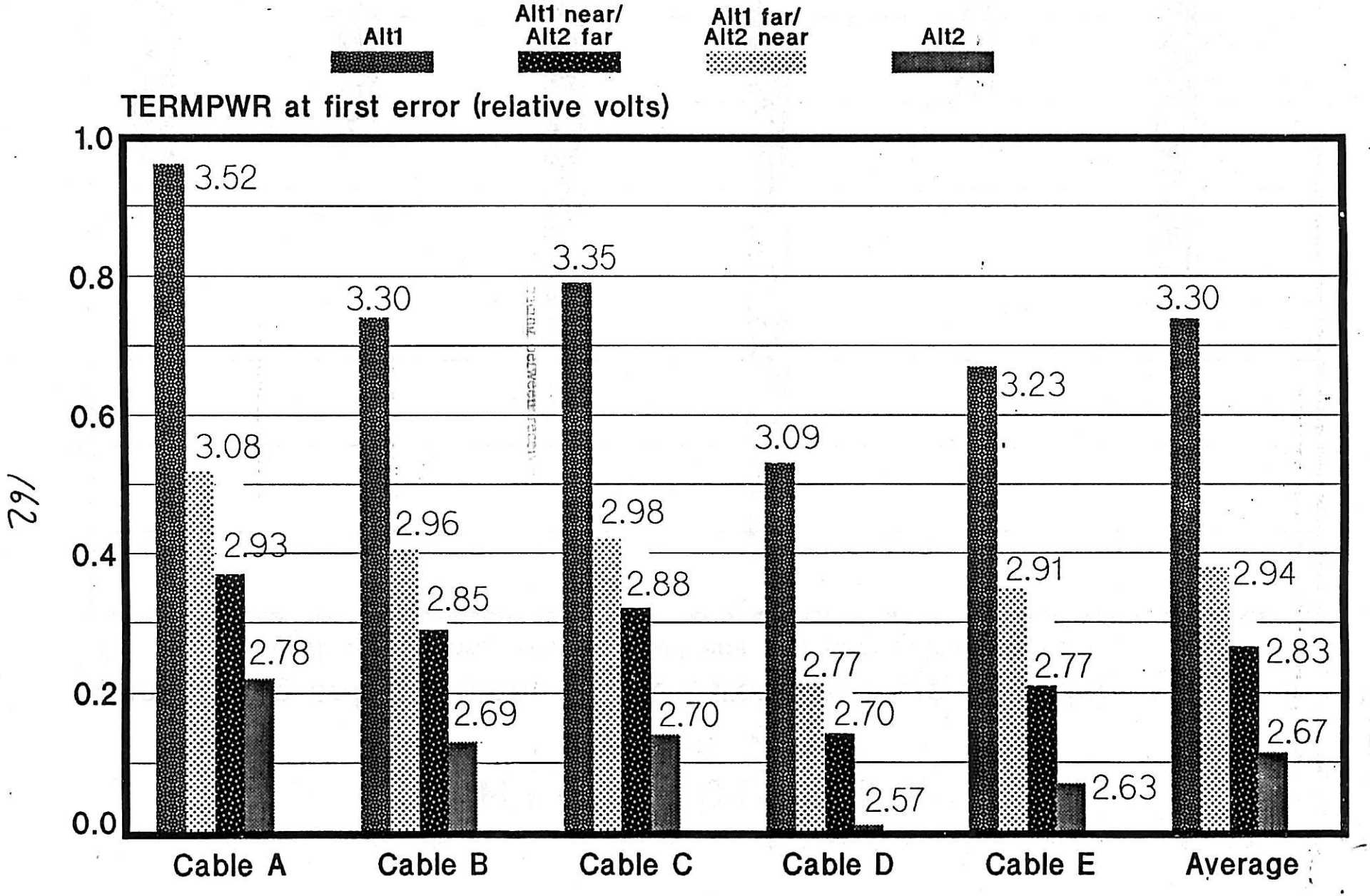
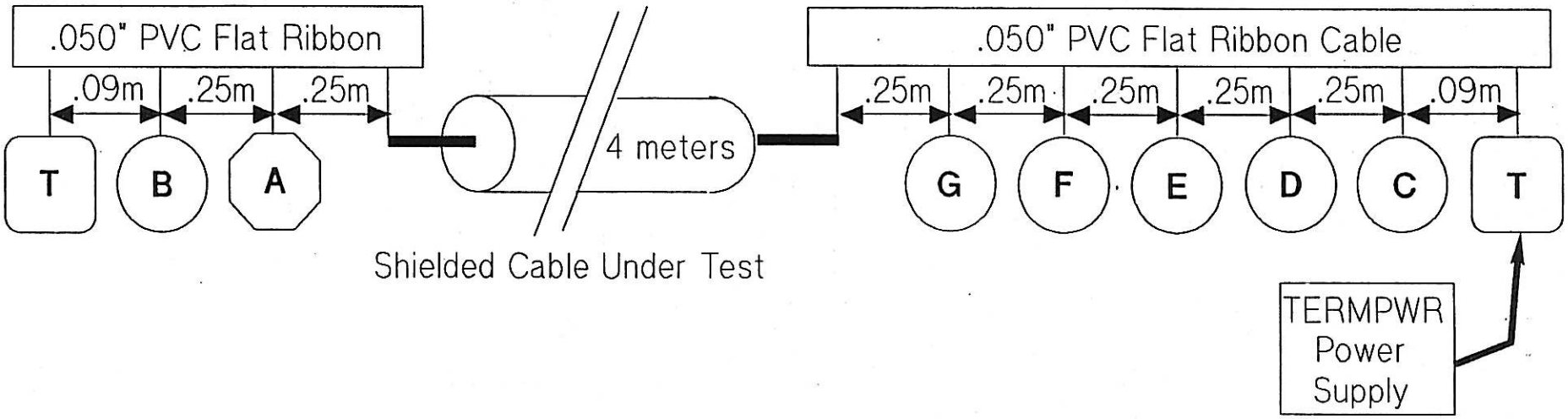


FIGURE 1: CABLE CONFIGURATION

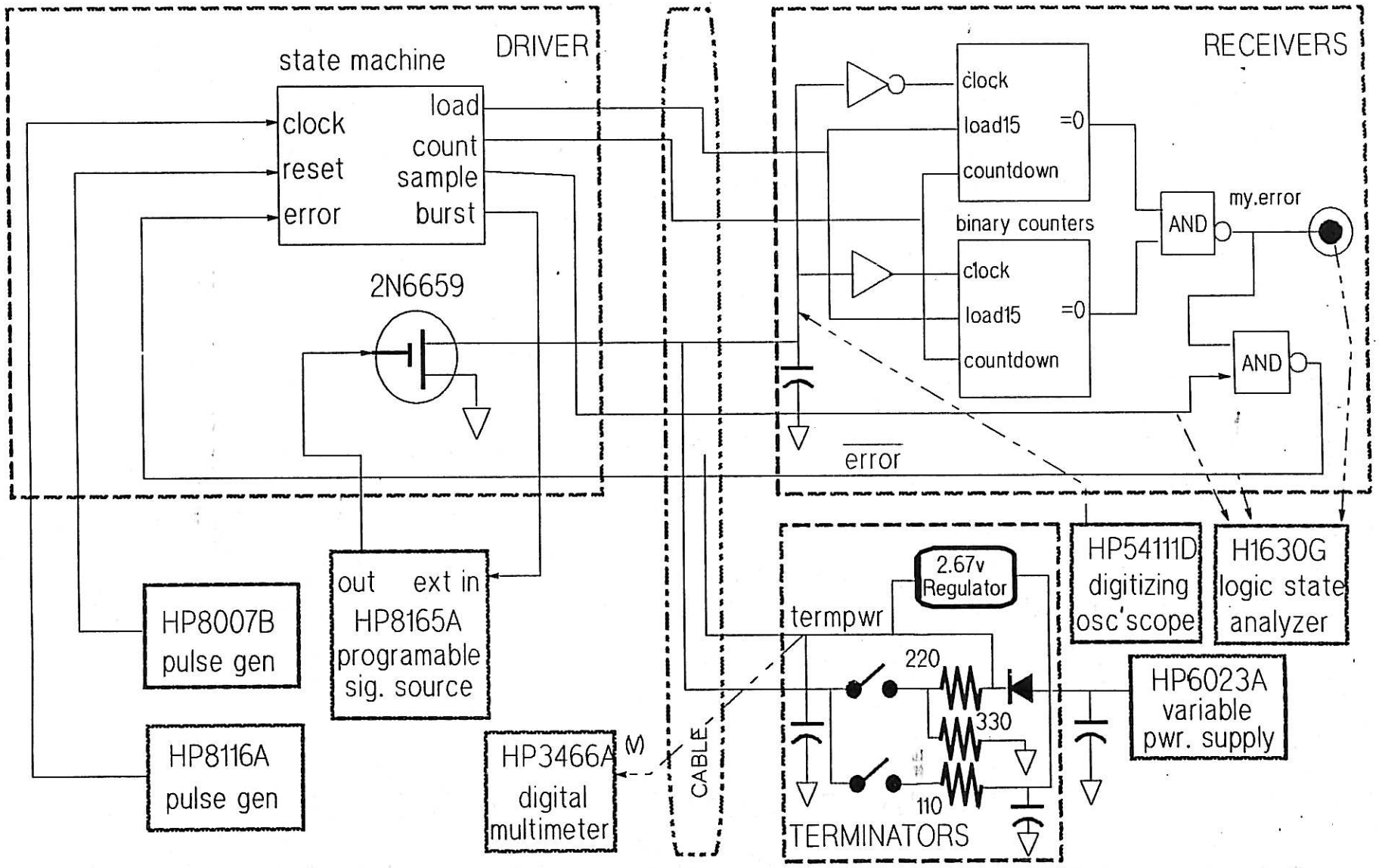


A DRIVER AND RECEIVER

T TERMINATOR

B-G RECEIVER

FIGURE 2: BENCH TEST COMPONENTS



HEWLETT PACKARD SCSI-2 SHIELDED CABLE EVALUATION

- **SAMPLE:** Enables receivers to assert error signals if appropriate.

When powering up, or to recover from selectable halts on errors, an HP8007B pulse generator is manually triggered to send a low **RESET** pulse to the state machine.

When the **BURST** signal is asserted by the state machine, it triggers an HP8165A programmable signal source set to send a burst of 15 square, 50% duty cycle pulses (4.0 v amplitude, 1v offset) to the gate input of an 2N6659 FET, to drive the test signal, ACK, low.

B.2.2 Receiver Board

The receiver boards have two four-bit binary count-down counters, each clocked off opposite edges of the received test signal. A capacitor was added to each receiver board to give it input capacitance around 25pF.

The counters are preloaded to 15 when the **LOAD** signal from the Driver board is asserted. The counters are enabled when the **COUNT** signal is asserted. When **SAMPLE** is asserted, if both counters are not 0, then an error signal is asserted, and a common wire-OR'ed **ERROR** signal is asserted back to the Driver board. An HP1630G logic analyzer monitors all receiver board error signals in continuous trace mode to provide visual indication of errors occurring.

B.2.3 Terminators

The terminator boards have switches to select between alternative terminations, as shown Figure 2. TERMPWR is driven by a variable power supply through a Schottky diode, only at the terminator board at the right end of the cable (adjacent to receiver C). The other terminator receives TERMPWR across the cable. To ensure accuracy in setting the value on the board, regulation is sensed on the TERMPWR side of the Schottky diode.

TERMPWR is set to 4.25V for time and power measurments, but is lowered to measure sensitivity to TERMPWR value.

The first alternative for termination is 220 ohms to TERMPWR, and 330 ohms to ground. In this case, a 2.2μF tantalum electrolytic capacitor is put on the TERMPWR line, with a 0.01μF disc capacitor at the resistors.

The second termination alternative is the low-dropout regulator alternative suggested in Rev 10, except using 2.67V through 110 ohms. The recommended capacitors were used.

B.3 Variables

We performed all measurements at 5 MHz, and tested each cable with each of the four possible termination schemes available by using either 220/330/TERMPWR or 110/2.67V at each cable end.

For TERMPWR sensitivity measurements, TERMPWR was started at 4.25V and decreased slowly until first Receiver-detected error. The power supply we used gave us precision to about 20mV.

B.3.1 Measurements

B.3.1.1 TERMPWR Sensitivity

The HP 1630G logic analyzer was used in continuous trace mode to monitor all error signals on the receiver boards, clocked by the falling edge of the driver's SAMPLE signal. By visually monitoring the display, we could tell when TERMPWR was low enough to cause errors. We were able to pinpoint that voltage to within 20mV by the digital voltage indicator on the power supply.

Before lowering TERMPWR, it was set to 4.25V, and we used TIME INTERVAL OVERVIEW mode on the logic analyzer to count the number of errors reported per second by any board, for 100 seconds. None was ever reported for any cable or termination scheme at 4.25V. That is an error rate of less than $10e^{-8}$, and we are confident we would not see an error at that voltage.

B.3.1.2 Settling Delay to 2.0V

This is measured from the 1.5V level on the output from the programmable pulse generator into the FET driver until the SCSI bus signal achieves 2.00V without falling below it again. It was measured from the middle pulse of the burst of 15, because the first couple of pulses have slightly different waveforms than the later ones in each burst. We used the HP54111D digitizing scope, displaying in repetitive mode with 20 for the number of averages, to minimize jittering observed in real time mode.

B.3.1.3 Settling Delay to 0.8V

This is measured similar to the settling time to 2.00V, except we start from the opposite edge of the drive signal = 1.5 volts and measure to the time that the SCSI signal falls below 0.80V without recrossing.

APPENDIX: TEST PROCEDURE AND CONFIGURATION

A. PROCEDURE

The system tests the cables by sending bursts of pulses on a single signal line and monitoring each SCSI "device" for errors. The SCSI "devices" consisted of one driver board (with receiver), 7 receiver boards, and 2 terminator boards with selectable termination schemes. Controlled by an external clock, the test system followed the following sequence:

- Preset a pair of counters on each receiver to 15.
- The driver board sends a burst of 15 pulses down the bus on one signal.
- Each receiver board counts separately the rising and falling burst edges.
- During a sample period, any receiver whose counters disagree asserts an error signal, detectable by external logic analyzers.
- Repeat the process.

We took the following measurements, as indicators of signal quality and performance of each cable:

- As TERMPWR drops from 4.25V, measure the first voltage at which an error is detected.
- With TERMPWR at 4.25V, measure the voltage drop across the cable of TERMPWR.
- With TERMPWR at 4.25V, measure noise on TERMPWR.
- With TERMPWR at 4.25V, measure the time delay from the driver turn on/off to the driven signal being reliably above 2.00V or below 0.80V, at various points along the cable (rise and fall time).

B. CONFIGURATION

B.1 Cabling

Figure 1 shows our cabling configuration. On the left, there is the driver board, A, next to the shielded cable. Connecting driver A to receiver B and a terminator board is a flat unshielded SCSI-1 cable. Spacing between A and B, and between A and the shielded cable is .25m. Spacing between B and the terminator board is .09m.

On the right of the shielded cable are 5 receivers (C, D, E, F, G) and a terminator board along another flat unshielded SCSI-1 cable. Spacing between receivers, and between G and the shielded cable is .25m. Spacing between C and the terminator is .09m.

B.2 Components

Refer to Figure 2 for the following description of test system components. External instruments are described within the description of the component board to which they attach. TTL power is provided to driver and receiver boards from an adjustable 1A DC power supply set to 5.00V (not shown)

B.2.1 Driver Board

The driver board also contains the elements of a receiver board. An HP8116A pulse generator provides a clock to the driver board (300KHz, 50% square wave). This drives a state machine which generates control signals in the following sequence, repetitively.

- **LOAD:** Presets counters on all receiver boards.
- **COUNT:** Enables counters on all receiver boards.
- **COUNT, BURST:** With receiver counters enabled, trigger external HP8165A programmable signal source to generate 15 pulses.

CONCLUSIONS

a. Parameter variations found in shielded cable influence signal quality at least as much as those of unshielded cable.

b. In general, high Z_0 cables performed better than low Z_0 cables in the TERMPWR test.

c. Alt2-Alt2 termination performed the best on the TERMPWR test, and minimized the differences between the cables.

d. Alt1-Alt1 termination performed the worst on the TERMPWR test, and accentuated the differences between the cables.

e. The average difference in the error voltage between Alt1-Alt1 and Alt2-Alt2 was 0.63V.

f. Alt1 and Alt2 terminations are compatible with one another. Any combination of Alt1 and Alt2 is better than Alt1-only terminators on the TERMPWR test. The average benefit of a "hybrid" termination scheme over Alt1-Alt1 was 0.22V.

g. Alt2 terminations with different output voltages also interoperated, although more testing needs to be done with multiple-signal transitions (see "Future Testing").

h. Alt2-Alt2 termination was the fastest on rising edges, but was the slowest on falling edges (1 to 4 ns slower than Alt1-Alt1 with some cables).

i. Alt1-Alt1 was fastest on falling edges, but was the slowest on rising edges (up to 12 ns slower than Alt2-Alt2 with some cables).

   (This is because the Alt1-Alt1 presents a Thevenin equivalent impedance in the pullup direction of about 132 ohms at 2.55V, versus 110 ohms at 2.67V for Alt2-Alt2. Since the Alt2 terminators pull up through a lower "source resistance," this hurts them slightly on pulldown when compared to the weaker Alt1 terminators).

j. Cable E was the fastest of the five samples, on both rise and fall times. Cable D was the slowest.

k. Cable D was most tolerant of low TERMPWR voltages. Cable A was the ~~is sufficient to prevent voltage sag during signal turn-on~~ least.

3. FUTURE TESTING

Future testing may involve one or more of the following:

a. Multi-signal tests: driving 12 lines simultaneously and observing the voltage levels on undriven signals, as well as the settling times for the 12 driven lines.

b. Investigating the effects of Alt2 termination and high impedance cables on extending the distance and speed of single-ended systems.

c. Repeating these tests for any new, high-impedance cables, or for other wire pairs in the same cables.

d. Repeating these tests with the 68-pin 'B' cable (for the 16-bit data path being discussed in the SCSI-3 working group).