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X3T9.2/89-82 R0

Date: June 14, 1989
To: X3T9.2 SCSI Committee Members
From: Kurt Chan
Subject: Elaboration on TERMPWR decoupling
Ref: Rev 9, 4.4.3

The attached report describes a problem inherent to SCSI systems or any bus which uses termination resistors. Due to transmission line characteristics of the TERMPWR wire itself (the wire cannot instantaneously supply current or voltage to remote terminators) TERMPWR has been observed to fall as low as 2.5 volts and rise as high as 7.2 volts when several signals switch simultaneously on a system which does not decouple its termination networks. When this happens, signals which are deasserted will drop below the 2.0V threshold, or signals which are asserted will rise above the 0.8V threshold at various points along the bus, depending on the polarity of the transient.

Capacitors placed at the terminators have proven to be effective in filtering TERMPWR sufficiently to alleviate this problem. Without these capacitors most systems will be guaranteed of violating the 4.25V TERMPWR specification somewhere along the cable, if only momentarily. Lack of such capacitors has been shown to be a significant source of signal degradation on real HP systems: several non-functioning systems have been restored with the addition of a single capacitor at the remote terminator.

Our key findings are:

1. 2.2 microfarads is the recommended minimum capacitor value which satisfactorily filters the TERMPWR discontinuity on the configurations tested.
2. Solid tantalum capacitors offer superior AC characteristics over aluminum electrolytics of the same capacitance, and are therefore preferred.
3. Decoupling in the middle of the bus is not sufficient - decoupling at the *terminators* is mandatory and sufficient for eliminating the problem, although a capacitor at every device stub on the bus would come close to accomplishing the same objective. For example, if the source of TERMPWR resides in the middle of the bus, steps need to be taken to ensure both terminators are also decoupled.

Manufacturers of terminator networks should include these capacitors in their designs. Device manufacturers may also want to consider including a similar capacitor in their designs to lessen the probability of systems problems should these guidelines be overlooked by the systems integrator.

To help prevent this oversight, we would like to modify the Implementors Note in Revision 9, section 4.4.3 to be more specific:

> IMPLEMENTORS NOTE: It is strongly recommended that the terminator power lines be decoupled at each terminator with at least a 2.2 microfarad capacitor to improve signal quality.

TERMPWR TRANSMISSION LINE EFFECTS ON SIGNAL QUALITY IN SCSI SINGLE-ENDED SYSTEMS

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1. PROBLEM DESCRIPTION

Early HP host adapters showed improved noise immunity in larger configurations when capacitors were placed on the TERMPWR line. Suspicions arose that there could be a significant glitch problem on cables due to TERMPWR glitches coupling onto signal lines at the terminators, because there were no charge-storing circuits specified for the terminators. However, no investigation had been done to demonstrate the severity of the problem, or what components were appropriate as a solution.

Our basic conclusion following this investigation was that TERMPWR can indeed incur large glitches of several volts lasting up to two bus propagation delays, depending on bus configurations. These transients couple directly onto static signals, causing deasserted signals be driven well below 2.0 volts, and asserted signals to be driven well above 0.8 volts at various points along the bus.

The SCSI electrical characteristics that lead to the problem are:

1. TERMPWR is a transmission line which shares many of the same characteristics as the signal lines. Current surges entering this line at the terminators will propagate and reflect exactly as they would on any signal line, except where there is a low-impedance voltage source.
2. TERMPWR is often supplied by only one device on the bus.
3. TERMPWR is usually supplied through a diode so that multiple power supplies are protected from each other; but this also isolates positive surges on TERMPWR from the voltage sources.
4. Having multiple sources of TERMPWR does not guarantee that the sources will share the burden of supplying current to the terminators. Since the TERMPWR supply voltage may differ from device to device, differences in TERMPWR voltage between devices can shift the distribution of current on the TERMPWR line (because of the v/i characteristics of the diodes). If the mismatch is large enough to cause all the diodes of other TERMPWR sources to become reverse biased (5.25V vs. 4.25V, for example) *all* current will end up being supplied by the highest voltage source.
5. TERMPWR may be supplied at any point along the bus, and is not guaranteed to be supplied at or even near the terminators. This is the biggest contributor to the problem.

These facts and other electrical characteristics lead to the conclusion that a current surge waveform propagating down the bus from a point where many data lines are changing simultaneously will couple into other signals through the pullup termination resistors if there is not a TERMPWR voltage source right at the terminator to absorb or provide the current surge needed.

The worst real-life case is when the data lines along with MSG, C/D, and I/O all change at the same time, causing noise on signals of *opposite* polarity (several signals going low causing a deasserted signal to also go low, or several signals going high causing an asserted signal to also go high).

This phenomenon has nothing to do with crosstalk, or driver slew rate, but instead is a function of where TERMPWR is supplied and where the drivers are. There are small differences due to variations in voltage, resistance, and capacitance in different devices.

To understand the the sequence of events that cause this problem, consider two scenarios. In the first scenario, we have TERMPWR supplied locally but not at the remote end, and several drivers are at the remote end of the cable which switch from high to low:

1. The remote drivers conduct at time t=0. At the remote end, the asserted signals go low immediately since they are pulled to ground through the low impedance of the drivers.
2. TERMPWR at the remote end cannot change instantaneously. When the drivers turn on, remote TERMPWR sees a voltage divider between the characteristic impedance of the cable and the network of 220-ohm pullups that are now grounded by the drivers.
3. Before t=0, remote TERMPWR was at 5V. Now, it sees some value less than that due to the voltage divider effect. At t=0 a *negative* voltage waveform propagates down the cable back to the TERMPWR supply. Along with the voltage differential, a current waveform is propagated.
4. In order to satisfy its instantaneous current requirements, the driver begins to pull charge off of adjacent signals through the termination network, causing these signals to drop. This is compounded by the TERMPWR sag which causes the bias point of all remote signals to lower.
5. The result is that previously deasserted signals may drop below the 2.0V threshold momentarily, until the return current and voltage waveforms arrive from the local TERMPWR supply one round trip delay later.

Here's another scenario which describes what happens with TERMPWR supplied locally but not remotely and a local driver which switches from low to high.

1. The driver changes state, propagating a change in current and voltage down its cable wire. Locally, the signal does not swing to the full value of TERMPWR due to a voltage divider effect between the characteristic impedance of the cable and the termination network supplying current to the cable.
2. The waveform hits the terminator at the end of the bus. Some of the current reflects back along original signal path, and most of it goes through the terminators (all, if the termination matches the cable exactly).
3. Some of the current surge goes through the ground-side termination resistor, and some goes through the pullup resistor to TERMPWR.
4. The current going through the resistor to TERMPWR will split among all possible paths. Some will go down the TERMPWR cable line, and some will reflect back down the original signal pullup resistor, and the rest will go down each pullup resistor attached to TERMPWR at that end of the cable. This is the source of the coupling glitch.
5. The current going through the pullup resistors on the other signals will split between the pulldown resistor (330 ohms) and the signal cable line, contributing noise to an otherwise independently driven signal.

2. TEST PLAN

Our investigation used SPICE simulation and bench verification. The first step was to develop a model of the bus system capable of representing accurately a real bus with multiple changing data: a full 18 signal system with 12 changing signals and 6 meters of cable.

Various configurations were set up and run with nominal parameters to find which arrangement of drivers and TERMPWR source exhibited worst coupling situations.

Parameters were varied within allowed margins to cause the worst possible coupling situation on the most sensitive configuration. I was looking for cases where signals being held constant were perturbed. Even if they did not enter the illegal band of 0.8 to 2.0 volts, any perturbations erode the noise margins for SCSI single-ended transceivers.

Finally, possible components and strategies for reducing coupling were tested to measure their effects and to prove whether they were viable solutions.

One of the worse case toplogies was selected to set up on a bench with real components, and measurements taken to verify the model used for simulation. No significant discrepancies were expected between the SPICE simulation and the bench custom test.

2.0.1 SPICE MODEL

A SPICE model was developed to simulate the SCSI bus. I chose as simple a configuration as possible which would still match possible real world environments. That was 3 devices connected by two 3 meter cables. Stubs were ignored, as a model with 38 transmission lines is complicated enough, and would allow us to verify it more readily on the bench. Using the basic model, I created many variations, changing the placement of components and varying their parameters.

The model consisted of all 18 bus lines, with 12 lines changing simultaneously, one signal to be held constant low or passive high, and the other 5 signals passive high.

Figures 1 and 2 show a hierarchical diagram of the SPICE model. Figure 1 shows the arrangement for both the drivers and TERMPWR occuring at the center of the bus. Other configurations were simulated by changing where these components were attached along the bus model.

2.0.1.1 Component Characteristics

The components of the SPICE model had the following fundamental characteristics:

- TERMPOWER = Nominal 5.0v voltage source through a Schottky diode.
- Termination resistances at each end of the bus = nominal 220 ohms to TERMPWR, 330 ohms to ground.
- Cables = Nominal 105 ohm transmission lines, 3m. long, 15.75 nsec. delays (.63 of speed of light). Attenuation was not modeled due to some suspicious behavior of our SPICE program (like 0-delay transmission lines when attenuation was included).
- Receivers = 1.4v. threshold, 0.1ma current source at 0.4v.. 0.1ma leakage maximum above 1.4 v., 25 pf total capacitance, and Schottky clamp diodes for protection against negative voltage swings.
- Drivers = Open collector drivers, with 0.1 ma leakage high, 48 ma at 0.5 v., nominal slew rate = 5v/2nsec.

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2.0.1.2 Variable Parameters

The following component characteristics were varied in the model to attain worst responses under simulation.

- Cable Impedance was either 75 or 105 ohms (105 nominal).
- TERMPWR voltage on bus was nominal 4.72v, varying from 4.25 to 4.95.
- Termination resistances could vary by 5% from 220/330 (nominal).
- Driver rise and fall was 2 nsec. or 10 nsec.
- Capacitance at termination resistors = 1pf, .01uf, 1.0 uf.
- Clamping diode could be removed from devices.
- Test signal could be held low with standard drive circuit or left alone.

2.0.1.3 Bus Configuration

All possible placements of these with respect to each other were tried on the 3-device system. Since the bus layout was symmetric, there were five different ways to arrange the driver and TERMPWR source (D=driver, T=TERMPWR, R=receiver). Note that end devices always had terminators attached, and only the location of the driver and TERMPWR was varied.

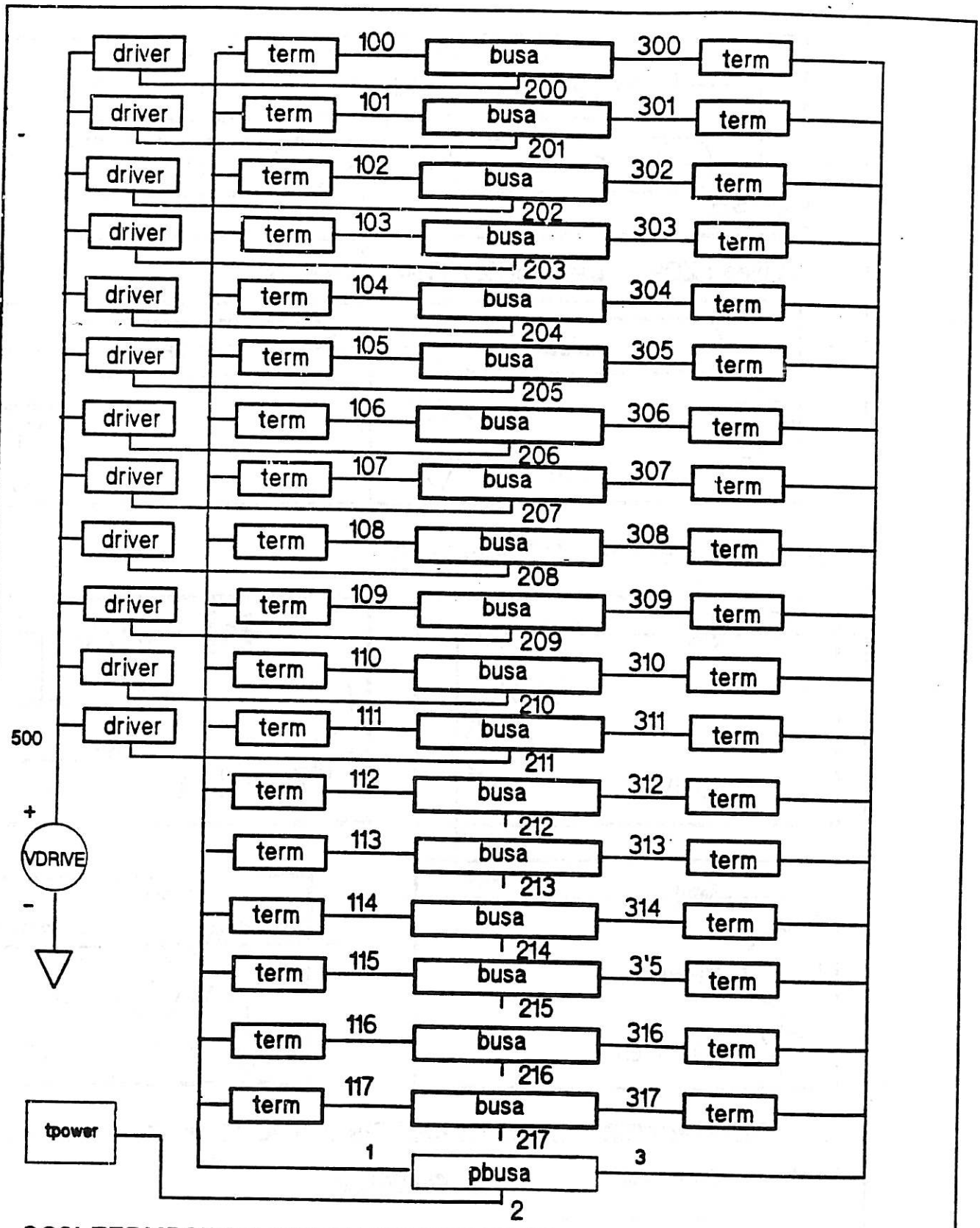
Configuration	Description
DTR---R---R	TERMPWR and Driver on same end
TR---R---DR	TERMPWR at one end, Driver on the other
DR---RT---R	TERMPWR in the middle, Driver at one end
TR---DR---R	TERMPWR at one end, Driver in the middle
R---DTR---R	TERMPWR in the middle, Driver in the middle

2.0.1.4 Stimulation

A piecewise linear voltage source model was used to simulate drivers turning on (low) or off (high) simultaneously at time=0. In cases where drivers were going low to high, a test signal was chosen (corresponding to ACK/ or REQ/ on the bus) and permanently driven low at the same device where the drivers were. In cases where drivers were going high to low, the test signal was undriven. In all cases, the other 5 signals were left undriven.

2.0.1.5 Measurements

The simulations were run for 200 nsec to capture the worst case glitches, except when high terminator capacitance caused lower response frequencies. At each device on the bus, I recorded the voltage waveforms of the TERMPWR signal, the test signal (REQ/), and a driver signal, although the only one apt to be interesting to the reader will be the test signal. Initial values of these voltages were gleaned from the SPICE report. Waveform plots were examined to obtain the magnitude and duration of the worst perturbations appearing on the test signal. As a separate measurement, I recorded the amount of time spent by the test signal between the values 0.8 and 2.0 volts before it stabilized outside that range.



SCSI TERMPOWER GLITCH "SPICE" SIMULATION MODEL -- TOP LAYER

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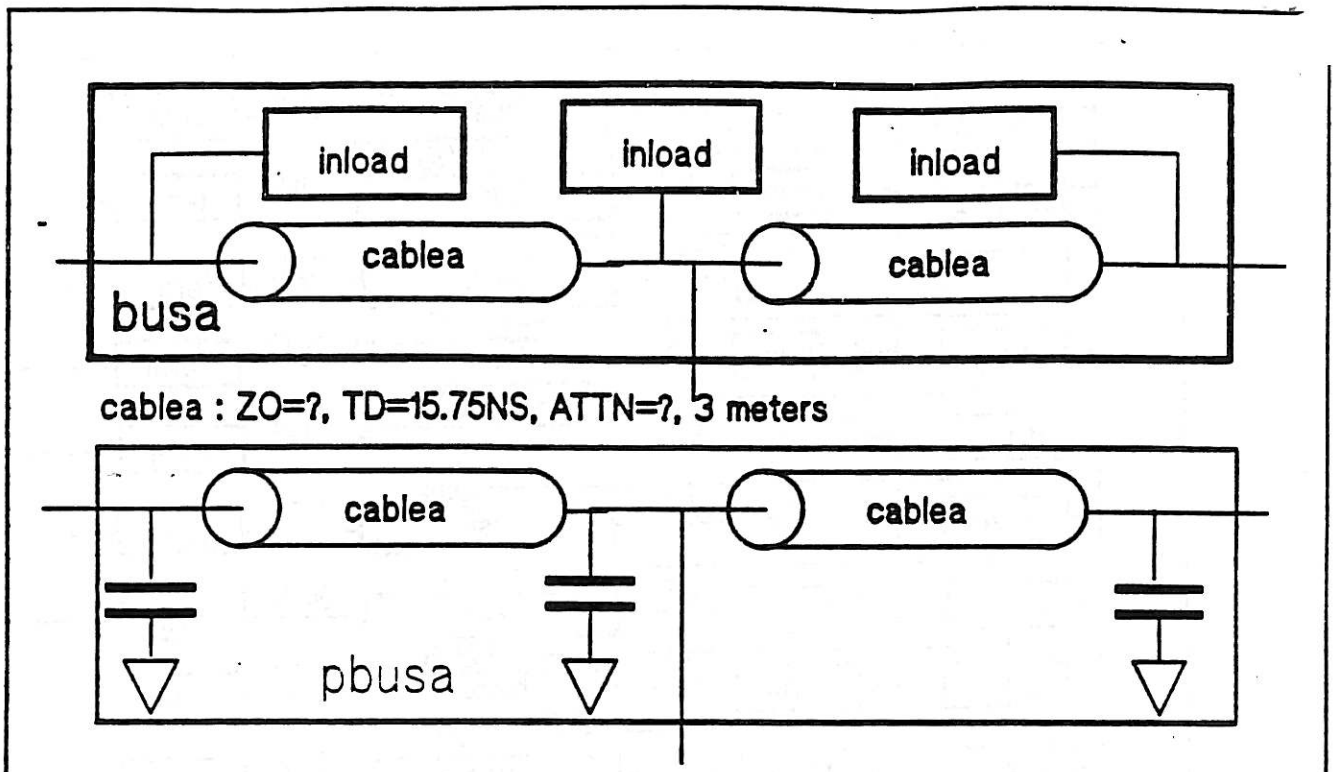
FIGURE 1



SCSI TERMPOWER GLITCH "SPICE" SIMULATION MODEL — SUB-LAYERS

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FIGURE 2

2.0.2 BENCH TEST

2.0.2.1 Circuit Description

I set up a test fixture patterned after the simulation model, using 74AS240 line drivers, driving the bus by applying a square clock to the enable inputs. Terminators were 215 ohms up and 316 ohms down. TERMPWR was applied from a variable power supply through a Schottky diode (1N5817). The REQ/ signal was chosen as the test signal, as for the simulation runs, since it is isolated from the driven signals at the far end of the cable connector (to eliminate crosstalk. Test boards were interconnected with shielded, 105-ohm twisted pair cable (according to specs), which was measured to be closer to 70 ohms, considerably different from its specification.

2.0.2.2 Configuration

The configuration for the bench test was the same as the worst simulation case for falling edges, corresponding to simulation case #9. This was with both drivers and termination power provided at bus midpoint. I developed simulation case #32 based on parameters found on the bench verification circuit, and compared this against the bench results to gauge the accuracy and confidence factor in our simulation runs.

2.0.2.3 Measurements

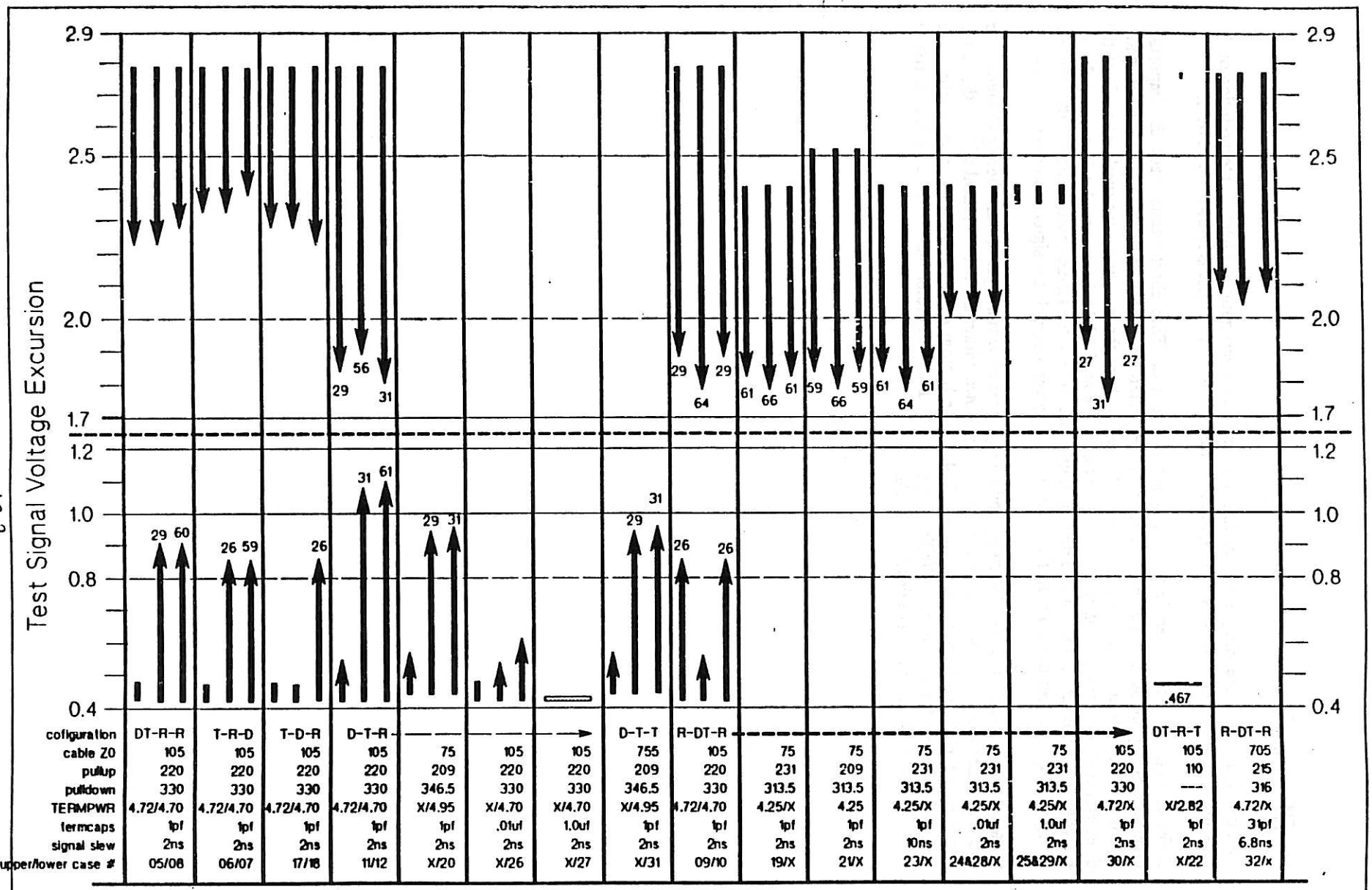
On a digital oscilloscope I recorded the test signal waveform at the middle and ends of the cables for comparison to simulation runs. Appendix C is a plot of the scoped waveform of the test signal. Results are discussed in the next section.

3. RESULTS

This is a summary of the things seen and learned from this investigation. There is interpretation of the measurements, discussion of what seemed to help the problem, and what is known not to help.

Refer to Figure 3 when specific test cases are mentioned. That chart summarizes the important measurements graphically. For each case simulated, there is a horizontal slice three arrows wide. There are three arrows within each horizontal slice to show the measurement made at each of the three physical bus device locations. An arrow tail starts at the initial test signal voltage, and the tip shows how low the signal is perturbed during simulation. Where the signal crosses into the illegal noise voltage band, a number at the arrow tip shows how many nanoseconds the signal is found in that range.

Separate case numbers are used for rising and falling cases of driven signals, but where parameters for two such cases are otherwise identical, the cases are shown within the same vertical slice of the chart. The parameters for each case are summarized along the bottom of the chart. The case numbers are included (falling edge case number/falling edge case number) for reference to the raw data charts in Tables 1, 2 in the section on investigation details.



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SCSI TERMPOWER GLITCH SIMULATION RESULTS

FIGURE 3

3.0.1 GLITCH MAGNITUDE

Even with all parameters nominal and TERMPWR provided at one cable end only, low to high perturbations on the opposite end of the bus from where REQ is held low exceed 0.8 volts for 60 nanoseconds (case #8).

For falling edges, it is not difficult to find cases which spend around 65 nanoseconds near 1.78 volts in the noise band.

Almost every configuration has problems. Even those which do not cause the presumably "static" test signal to enter the noise band force half-volt pulses of 30 nanoseconds or more.

The reason that many systems today work as well as they do with these TERMPWR-related glitches is that none of the glitches simulated hit the more common real world switching threshold of 1.4 to 1.7 volts. There may also be some response time delays in present devices which filter short glitches on REQ and ACK. Situations where fewer than 12 signals change simultaneously will have smaller glitches than those presented here, and it may be that present devices do not change the message control signals with the data and parity signals. Changing only 9 signals at once will produce a glitch of 75% of the magnitude of the ones caused by these simulation cases.

The preceding paragraph is conjectural, as there was not time to investigate in detail any current products or systems. However, it is obvious that there is a very real and serious potential for bus failure if these issues are not kept in mind and dealt with properly.

3.0.2 SIMULATION VERSUS BENCH CASE

The bench case corresponding to simulation run # 32 did exhibit some differences. The simulation predicted a lowest glitch of 2.03v. in the middle and 2.07v. on the ends, with no time actually spent in the noise band. The bench system showed excursion to 1.77v at the middle device, lasting about 30 nsec in the noise band, and a brief 5nsec glitch into the noise band on one end. The scope trace was much more rounded than the simulation predicted, with more bumps. The traces do show very similar general trends. Differences are due to some of the following things:

- No cable attenuation modeled. Measured loss on TERMPWR was 0.09v. across 2.45m. of shielded cable.
- Bench setup had short stubs not modeled in SPICE.
- Driver models were not verified as accurate to bench drivers.
- Bench had short (8.5-13 cm) flat cables between cables, boards, not included in models.
- Grounding of bench system was not ideal: measured 0.4v glitches between ground of different bench system boards.

3.0.3 WORST CASE CONFIGURATIONS

The configurations showing worst magnitudes of perturbation are those where termination power is supplied only at the center of the bus and the drivers are there, too. In this arrangement, there is no voltage source at either terminator to absorb the force of the current surge of 12 signals changing simultaneously, causing the most coupling onto other signals. When a driver and TERMPWR are at the ends, the voltage source smooths the surge, and there is less energy to go back down the cables and into other signals. This is shown in simulation cases 5-8, 17, 18.

3.0.4 WHAT HELPS

3.0.4.1 Capacitors on TERMPWR

Per our recommendation, decoupling capacitors solve the problem. They provide electrical charge storage which prevents sudden changes in voltage on TERMPWR. They do not totally eliminate signal noise, but 1.0 uF capacitors reduce them significantly. Going to the recommended 2.2 uF provides a conservative minimum value. Simulation cases 24 through 29 show the net effect of adding .01uf and 1.0 uf capacitors only at the terminators.

Notice that .01uf capacitors do not reduce the problem sufficiently. The rising edge glitch in case #26 can still reach .61 volts, and the falling edge glitch in case 24 reaches 2.005 volts. These glitches, however, take the form of a damped sinusoid with a period of about 740 nsec, due to the interaction of the capacitors with the transmission lines to which they are attached.

The 1 uf capacitor does a much better job. It leaves only .0094 v perturbations for rising (case # 27), and .064 v. for falling (case #29). These are still damped sinusoids, which now have a period around 2 microseconds.

3.0.4.2 TERMPWR Location

Providing TERMPWR at both bus ends reduces signal noise. However, no matter where it is placed, undesirable levels will still occur. Rising edge glitches decouple the voltage source when the diode becomes reverse biased, so you won't significantly reduce rising glitches without charge storage on the *bus side* of the diode. And you have to have current balancing between the voltage sources or one will dominate, cancelling your benefits. The capacitors are still mandatory.

3.0.4.3 TERMPWR Voltage

Termination voltage variations do not have very much effect on these glitches. Keeping TERMPWR high is therefore not a solution as it was with other signal quality issues. When you increase the termination voltage, you increase the high level margin a bit, which offsets the gain in falling glitch magnitudes. Rising glitches will get worse with rising power voltage, but the difference due to this effect is swamped by the differences due to configuration.

3.0.4.4 Regulated Terminators

Paul Boulay of Laser Magnetic Storage proposed a self-contained regulator/terminator consisting of a low-drop voltage regulator on TERMPWR providing 2.85V through 110 ohm resistors to each signal. The regulator as recommended has heavy (22 uF) filtering on its output, sufficient for decoupling the 110 ohm pullups.

The Boulay regulator was not tried on our test jig and was not characterized as to how much oscillation it exhibits in the presence of many changing signals. Since there are no diodes on the regulator outputs, if there are two such regulators at each end of a quiescent bus, their outputs will be directly connected through the equivalent of 18 220-ohm resistors in parallel (about 12 ohms). Should one source be higher than the other, the lower voltage regulator may shut down. When signals begin to switch, changing the voltages between the two regulators, the regulators may be forced into oscillation in an attempt to match the transient behavior of the bus. More testing needs to be done on this circuit to confirm such behavior.

3.0.5 WHAT DOESN'T HELP

3.0.5.1 Multiple TERMPWR Sources

You can't count on devices at the far ends of a cable to each supply TERMPWR together through diodes. If they are attached this way, and the +5v supply on the devices vary by more than a forward diode drop, then only one of the devices will supply current to the terminators in the steady state. Schottky diodes exacerbate the problem by shifting the entire balance of current through only 0.2-0.3 volts difference. Although falling edge glitches will be reduced by this configuration, rising edge glitches won't, because the diodes isolate each supply when a rising voltage surge occurs (a voltage surge above the supply voltage reverse biases the diode, eliminating the effect of the source).

In a simulation case I ran to verify this, all three devices supplied TERMPWR; the end supplies were at 4.53v and the center was at 5.25 v. The waveforms for rising edge differed insignificantly from that of the case of a single supply at the center position; the glitch exceeded 1.1 v. at the bus ends while the test signal was held low at the center.

3.0.5.2 Receiver Characteristics

Configurations with more devices will experience lower magnitudes of glitching through TERMPWR, since there is some current drain and distributed capacitance along the bus. Stubs on receivers will also lower this, but introduce higher-frequency oscillations.

3.0.5.3 Capacitors on all Devices

Capacitors really only need be attached to the terminators at the ends of the bus cable. Placing capacitors on TERMPWR at intermediate points adds no significant benefit; the capacitors have to be at the energy distribution points to prevent coupling effects, and this occurs only at the terminators. Capacitors at other points will lower the sinusoidal amplitude and frequency somewhat.

4. RECOMMENDATIONS

4.0.1 SCSI-2 SINGLE-ENDED, A-Cable

We strongly recommend at least 2.2 microfarad capacitors between TERMPWR and ground at each terminator, with a .01 microfarad capacitor in parallel with it to help with higher frequency/low voltage noise. This is an inexpensive solution to the problem of TERMPWR glitch coupling. It is vital that any system configuration pay close attention to the problem described here. For cables of significant length, and configurations without TERMPWR at each terminator there is a high probability of signal corruption without such an approach.

Without a requirement to this effect in the standard, responsibility falls to the device and systems designers to compensate for this effect in their own circumstances.

From strictly a signal quality perspective, it is best if terminators get power only from the device to which they attach, and not over the bus, as you cannot totally eliminate these coupling effects by using capacitors, although they can be reduced significantly.

Unfortunately, cable-end devices may be powered down, and then the bus would be inoperative unless the terminators are supplied from other voltage sources along the bus. So you have to balance this desire against signal quality.

Note that this requirement also applies to active termination schemes. The circuit schematic proposed by Paul Boulay has the appropriate filter capacitors on the regulator output.

4.0.2 DIFFERENTIAL SCSI

Termination capacitors are also essential for differential terminators. Simulation work is needed to determine whether a different capacitor is indicated for differential termination. However, since most of the current in a differential system is balanced and comes from the complementary output of the driver rather than TERMPWR, the current surges down the TERMPWR wire will be less, indicating that 2.2 uF is sufficient.

4.0.3 B CABLE

Since the B cable includes four TERMPWR signal wires but has only 3 bytes of data (27 bits), it does not need more capacitance than the single-byte bus, as surges into the terminators have more opportunity to disperse into the TERMPWR wires than into the two control signals. This was verified by one simulation run which had 27 data signals changing at once and four TERMPWR lines. The glitch magnitudes were less than for the similar configuration of the single-byte bus without capacitors.

5. INVESTIGATION DETAILS

The Appendix lists a SPICE input file for one of the simulation cases, and a complete collection of plots of the test signal at each of the three cable positions for each test case.

5.1 SPICE SIMULATIONS

5.1.1 MODEL DESCRIPTION

Figures 1 and 2 show the logical organization of our SPICE model. Node numbers on Figure 1 correspond to node numbers actually used in the SPICE file. Nodes 113, 213, 313 were used as the test signal. That signal was left undriven when the first 12 signals were driven low. The test signal was pulled low with a standard driver model when the first 12 signals went low to high, since this maximizes the coupling glitch.

5.1.1.1 Bus Configuration

To allow for ease of configuration and parameter changes, the cable system was modeled hierarchically. This lets us change the impedance of all 19 cable segments or pullup resistors by modifying a single line in the file.

5.1.1.2 BUSA Subcircuit

This subcircuit defines each signal line as a three-port box. 18 copies of this gives us an 18-signal bus system. Nodes 100-117 correspond to the terminated side of the left cable, nodes 200-217 correspond to the connection between the two 3m cables, and nodes 300-317 correspond to the terminated end of the right cable.

Internally, this subcircuit has two sequential copies of the "cablea" subcircuit, which describe the cable transmission properties, and three copies of the "inload" subcircuit, which represent receivers on the signal lines placed at each cable end.

5.1.1.3 TERM Subcircuit

This subcircuit is used 36 times to provide cable termination on both ends of the cable system. It contains the pullup and pulldown resistor for standard SCSI single-ended termination. The node between the resistors will attach to either end of the "busa" subcircuit, and the other node will attach to TERMPWR by going to node 1 or 3 on the "pbusa" subcircuit.

5.1.1.4 PBUSA Subcircuit

This is the TERMPWR signal subcircuit. It contains just two sequential copies of the "cablea" subcircuit, as it is just another signal on the bus. It has a 1pf capacitor at each node, nominally, to simulate connector capacitance. In simulation cases where .01 or 1uf capacitors are loaded at terminators, the end capacitors of this subcircuit are modified.

5.1.1.5 DRIVER Subcircuit

This subcircuit models a saturated open-collector TTL driver. It consists of a Schottky diode in series with a 5.92 ohm resistor. The driver may be attached to any of the three ports of the "busa" subcircuit,

depending on the bus configuration desired. The low side of the diode is tied to node 500, which is the common voltage souree for all drivers. The diode and resistor are chosen so the signal will be at 0.5v. when node 500 is at 0v and there is 48 ma. flowing through the diode.

5.1.1.6 TPOWER Subcircuit

This is actually incorporated into the "pubsa" subcircuit in the SPICE input file. It is just an adjustable DC voltage source with a Schottky diode. It may be attached to system node 1, 2, or 3 to provide TERMPWR on the bus from anywhere on the cable system.

5.1.1.7 VDRIVE Voltage Source

A copy of this used to be incorporated into each "driver" subcircuit, but that was too complicated for our poor SPICE, so I isolated it and used it for all drivers in common (since it's an infinite current source). It is a piecewise linear source, starting at 0 or 5 volts at time 0, then transitioning to the other voltage in a selected slew time (2ns, nominal).

5.1.1.8 INLOAD Subcircuit

This is a model of a typical receiver with a 1.4v threshold, 25 pf of capacitance, and a clamping Schottky diode at the signal. The load resistor is 9925 to draw .1ma at 0.4 v. None of these parameters are altered for our test cases, except one time when I removed the clamp diode. The receiver has .1ma leakage through the diodes.

5.1.1.9 CABLEA Model

All cable segments use this as a model. It is a transmission line with 15.75 ns. delay and no attenuation (.635 times the speed of light, 3 meters). The impedance is either 105 or 75 ohms, to model two real cable types. Some cases were tried initially with attenuation modeled in, but there seems to be a bug in the way our SPICE handled that (like zero delay across 3m.), so those cases were eliminated for now.

5.1.1.10 D1N5821 Model

All diodes in our simulations use this approximate model of a Schottky diode. I didn't realize it was such a headache to try to create a model from spec sheets, so this does not correspond exactly to a 1N5821, but it comes close in the range of interest, under 1 amp.

Vf	If(1N5821)	If(model)
0.225	0.05	0.063
0.250	0.15	0.132
0.275	0.26	0.278
0.300	0.45	0.565
0.325	0.75	1.146
0.338	1.00	1.65
0.350	1.16	2.37

5.1.2 SIMULATION DETAILS

SPICE transient analysis is performed from 0 to 200 nanoseconds made on stimulation consisting of the independent voltage source VDRIVE rising or falling between 0 and 5V over 2 or 10 nsec. starting at time 0.

Node voltages captured for evaluation were 1, 2, 3, 100, 200, 300, 113, 213, and 313. This gave us views at each device of the TERMPWR voltage, a changing data line, and the test signal, in that order.

POSITION	NODE NUMBER		
	TERMPWR	DRIVEN	MEASURED
left	1	100	113
center	2	200	213
right	3	300	313

5.1.3 EVALUATION

Table 1 contains the summary data extracted from each simulation run, which was used to create the summary chart of Figure 3.

Initial values of the node voltages were obtained from the SPICE output file.

On-screen graphics and paper plots were examined to interpolate duration and magnitude of voltage waveforms. I recorded only the first (and always largest) perturbation of the test signal from its steady state when the data lines changed. The signal usually continued to ring after this first pulse, but these were not noted in the data record or summary. You may look at the plots included in the report for more contemplation and enlightenment. The duration of these glitches was always exactly one or two bus delays (around 31.5 or 63 nanoseconds), and these times are not recorded.

I did take special care to record the total time elapsed from the test signal crossing into the noise band until it left it permanently.

In the table, in addition to information presented in the summary, we also include the size of surges on the TERMPWR signal.

Note that I do not give the time relationships of the undesirable glitches to each other. That would complicate the picture; this information may be gleaned from the plots, and it does not matter when the glitches occur for these discussions, only their magnitudes.

5.1.4 TEST CASE DESCRIPTIONS

Each case will be discussed briefly to explain why it is included and what it was intended to demonstrate.

Some case numbers are skipped (you noticed?). These were they that were numbered before I got the SPICE process nailed down or that had anomalies in their responses that pointed to bugs in our version of SPICE with regard to lossy transmission line modeling.

5.1.4.1 CASES 0-4

Not included: working out the kinks.

5.1.4.2 CASE 05

This is the nominal parameter case for configuration of the drivers and terminator power on the left end and falling data. Although this is a case where the driver and termpower are on the same device, there are still 0.6volt excursions from initial values of 2.79 volts on the undriven test signal. This happens first on the right end of the bus, where lack of termination/regulation on TERMPWR lets coupling occur onto the test signal.

5.1.4.3 CASE 06

This is the nominal parameter, falling data case for a configuration with the driver and TERMPWR source on opposite ends of the cables.

5.1.4.4 CASE 07

This is the complement of case 06 with rising data.

5.1.4.5 CASE 08

This is the complement of case 05 with the same parameters, and a rising data signal set. Despite nominal parameters, the test signal rises to 0.91 volts.

5.1.4.6 CASE 09

This is the nominal parameter case of falling data with the driver and TERMPWR supply at the middle of the cables. It was the worst of the configurations with nominal parameters.

5.1.4.7 CASE 10

This is the complement to case 09, with rising data. Although case 9 was worst for falling data, case 10 was not as bad as some of its cousins.

5.1.4.8 CASE 11

This is the worst of the nominal parameter falling data configurations. It has drivers on one end with termination power provided in the middle of the cable system. Note that .4V signals can rise to around 1.1V due to this configuration.

5.1.4.9 CASE 12

This is the complement to case 11, with rising data, and turned out to be the worst case of rising data I found.

5.1.4.10 CASES 13-16

Not included: SPICE modeling problems.

5.1.4.11 CASE 17

This is the nominal parameter case of falling data with TERMPWR supplied on the right end of the cables and drivers in the middle. This is a fairly typical arrangement for real life, with the host supplying termination power, and intermediate devices driving data. Quake in your boots.

5.1.4.12 CASE 18

This is the complement to case 17, with rising data. It is the best of the nominal parameter cases tried, but still has excursions into the noise band.

5.1.4.13 CASE 19

This is case 09 but with termination perturbed 5% to keep the resistance unchanged but lower TERMPWR to 4.25 v. This is reflected in that the initial test signal value was 2.41 v, down from 2.79v. The glitch got a little worse, and caused extra duration in the noise band on the cable ends. Oh, yes: the cable was switched to 75 ohms for this case, too.

5.1.4.14 CASE 20

This is case 12 with termination resistors skewed 5% to raise the termination voltage, to see if rising glitches would get worse. It raised initial TERMPWR from 4.70 to 4.95 volts, but the glitch magnitude was reduced.

5.1.4.15 CASE 21

This is case 19 with resistors both skewed 5% to decrease the resistance of the termination. This raised TERMPWR and only slightly affected the glitch.

5.1.4.16 CASE 22

This was a control experiment done to verify the model and to show how things would behave if there was self-contained regulation in terminator cases, as proposed by AMP as an alternative. This configuration has 2.85 v supplies right at the terminators, which are replaced by 110 ohms only to the supply itself. This simulates 2.85v regulators running off TERMPWR. The traces show absolutely clean, naturally, since the voltage regulators totally eliminate coupling to other signals. Real components won't be perfect, but with large capacitors on the outputs, they will be close.

5.1.4.17 CASE 23

This is a variation of case 22, but with the driver slew rate changed from 5V/2nsec to 5v/10ns. Since the cable delays are 31.5 nsec, this change makes no difference in the waveforms, except to delay some edges a little; glitch magnitudes and durations remain. This is a modification which would help crosstalk problems, but it doesn't help our cases unless the cables are shorter than the 10 nsec transition time.

5.1.4.18 CASE 24

This is case 19 with .01uf capacitors on each end of TERMPWR. Glitch magnitude is reduced, but only to 2.0 volts, which is right on the noise band boundary. The signal is changed to a slower, damped sinusoid.

5.1.4.19 CASE 25

This is case 19 with 1.0 uf capacitors on each end of TERMPWR. The glitch magnitude is reduced to about 64 mv., peaking at around 1.8 usec.

5.1.4.20 CASE 26

This is case 12, the worst case rising glitch configuration, with a .01uf capacitor on each end of TERMPWR. The glitch is reduced substantially, and becomes a damped sinusoid with long period as the capacitors interact with the transmission lines. We're not there yet.

5.1.4.21 CASE 27

This is case 12 with a 1.0uf capacitor on each end of TERMPWR. The glitch has become a damped sinusoid peaking at about 2 usec only

5.1.4.22 CASE 28

This is just a replot of case 24 in a time scale to show the damped sinusoidal response due to the presence of .01uf capacitors.

5.1.4.23 CASE 29

This is just a replot of case 25 in a time scale to show the damped sinusoidal response due to the presence of 1.0uf capacitors.

5.1.4.24 CASE 30

This is a variation of case 09 with the Schottky clamp diodes removed. Slight rise in waveforms occurred, as diode leakage was eliminated, but differences were insignificant.

5.1.4.25 CASE 31

This is a special version of case 20. TERMPWR was sourced from a 5.25 volt supply at the middle cable position, and sourced it from a 4.53 v. supply at the right, keeping drivers in the middle. The waveform is identical to case 20, because the right supply cannot share in providing TERMPWR. The termination current is dominated by the middle supply, so no benefit incurs from using multiple supplies if they differ more than one or two tenths of a volt, at least for rising edge glitches.

5.1.4.26 CASE 32

This case duplicates as near as possible the real circuits I used to verify SPICE simulations against case number 12. Components available did not match those from other cases, so I customized this case to check against the bench system. Specifically, the important parameter differences were:

- Terminators were 215 ohms pullup and 316 ohms pulldown.
- Driver slew rate was chosen to match scope trace = 6.8 nsec.
- Cable impedance was 70 ohms to match measured value of cable.
- Cable delay was picked to match bench cable delay observed.

- Capacitance for the test signal at each board was measured at 24.5 pf, plus 7.5pf for the scope probes, for a total of 31 pf. (soldered wires).

Table 1: Simulation Case Descriptions and Initial Conditions												
Case	Config	Parameters							Initial Node Voltages			
		Z0	Rpu	Rpd	Vpwr	Caps	Slew	Edge	2	200	212	213
5	DT-R-R	105	220	330	5.0	1pF	2ns	fall	4.72	2.80	2.79	2.79
6	T-R-D	105	220	330	5.0	1pF	2ns	fall	4.72	2.80	2.79	2.79
7	T-R-D	105	220	330	5.0	1pF	2ns	rise	4.70	0.42	2.78	0.42
8	DT-R-R	105	220	330	5.0	1pF	2ns	rise	4.70	0.42	2.78	0.42
9	R-DT-R	105	220	330	5.0	1pF	2ns	fall	4.72	2.80	2.79	2.79
10	R-DT-R	105	220	330	5.0	1pF	2ns	rise	4.70	0.42	2.78	0.42
11	D-T-R	105	220	330	5.0	1pF	2ns	fall	4.72	2.80	2.79	2.79
12	D-T-R	105	220	330	5.0	1pF	2ns	rise	4.70	0.42	2.78	0.42
17	T-D-R	105	220	330	5.0	1pF	2ns	fall	4.72	2.80	2.79	2.79
18	T-D-R	105	220	330	5.0	1pF	2ns	rise	4.70	0.42	2.78	0.42
19	R-DT-R	75	231	313.5	4.53	1pF	2ns	fall	4.25	2.42	2.41	2.41
20	D-T-R	75	209	346.5	5.25	1pF	2ns	rise	4.95	0.45	3.05	0.45
21	R-DT-R	75	209	313.5	4.53	1pF	2ns	fall	4.25	2.52	2.52	2.52
22	T-R-T	105	110	---	3.13	1pF	2ns	rise	2.85	0.47	2.82	0.47
23	R-DT-R	75	231	313.5	4.53	1pF	10ns	fall	4.25	2.42	2.41	2.41
24	R-DT-R	75	231	313.5	4.53	.01uF	2ns	fall	4.25	2.42	2.41	2.41
25	R-DT-R	75	231	313.5	4.53	1.0uF	2ns	fall	4.25	2.42	2.41	2.41
26	D-T-R	105	220	330	5.0	.01uF	2ns	rise	4.70	0.42	2.78	0.42
27	D-T-R	105	220	330	5.0	1.0uF	2ns	rise	4.70	0.42	2.78	0.42
28	R-DT-R	75	231	313.5	4.53	.01uF	2ns	fall	4.25	2.42	2.41	2.41
29	R-DT-R	75	231	313.5	4.53	1.0uF	2ns	fall	4.25	2.42	2.41	2.41
30	R-DT-R	105	220	330	5.0	1pF	2ns	fall	4.72	2.82	2.82	2.82
31	D-T-T	75	209	346.5	5.3/4.5	1pF	2ns	rise	4.95	0.44	3.02	0.44
32	R-DT-R	70	215	316	5.0	1pF	2ns	fall	4.72	2.77	2.77	2.77

Table 2: Simulation Case Transient Results								
Case	Worst Transient Voltage					Time in Noise Band		
	1	3	113	213	313	113	213	313
5	4.72	2.83	2.23	2.23	2.28	0	0	0
6	4.72	3.16	2.33	2.33	2.38	0	0	0
7	4.70	6.36	0.47	0.86	0.86	0	26.4	58.6
8	4.70	5.47	0.48	0.91	0.91	0	28.6	60.0
9	2.83	2.83	1.88	1.78	1.88	28.6	64.3	28.6
10	6.60	6.60	0.86	0.52	0.86	26.4	0	26.4
11	3.16	2.67	1.84	1.89	1.80	28.6	55.7	30.7
12	6.60	7.16	0.55	1.08	1.10	0	31.4	61.4
17	4.72	2.83	2.28	2.28	2.23	0	0	0
18	4.70	6.50	0.48	0.47	0.86	0	0	26.4
19	2.72	2.72	1.82	1.78	1.82	60.7	66.4	60.7
20	6.76	7.09	0.58	0.97	0.98	0	30.0	30.7
21	2.62	2.62	1.83	1.78	1.83	59.3	65.7	59.3
22	none	none	0.47	0.47	0.47	0	0	0
23	2.92	2.92	1.82	1.78	1.82	60.7	66.4	60.7
24	3.51	3.51	2.005	2.005	2.005	0	0	0
25	????	????	2.346	2.346	2.346	0	0	0
26	5.80	5.85	0.48	0.54	0.614	0	0	0
27	4.86	4.86	0.429	0.429	0.429	0	0	0
28	3.51	3.51	2.005	2.005	2.005	0	0	0
29	4.14	4.14	2.346	2.346	2.346	0	0	0
30	2.54	2.54	1.73	1.90	1.73	27.2	31.4	27.2
31	6.76	7.09	0.58	0.97	0.98	0	30.0	30.7
32	2.95	2.95	2.07	2.03	2.07	0	0	0

5.2 BENCH CIRCUITS

5.2.1 Test Board

There were three "flavors" of boards built for bench verification, to allow re-creation of any of the configurations in the simulation set.

5.2.1.1 Terminated Driver Board

This board mounts on the left end of the cable system. It has two 74AS240 tri-state buffers driving the 8 data lines, parity, and the three bus phase control lines "I/O", "MSG", and "C/D". The signals are driven as open collector signals by tying the input pins high and driving the enable pins with a square wave clock.

The REQ signal is the test signal. It can be driven low statically or left undriven. This is selected by a switch on the enable pin of the 74AS240. The remaining signals are left undriven.

All 18 signal lines are terminated with packs of 215/316 resistor divider pairs.

There are posts for mounting a capacitor on TERMPWR if desired.

There is a jumper for connecting TERMPWR to a variable DC power supply through an 1N5817 schottky diode, if desired.

5.2.1.2 Unterminated Driver Board

This board mounts at the center of the cable system. It has the same data drivers as the first board.

It has no resistor terminators on the SCSI signal lines.

It has jumpers for connecting TERMPWR like the first board.

5.2.1.3 Terminator Board

This board has only terminators like the first board and TERMPWR connections like the second. It mounts at the right end of the cable system.

5.2.2 TEST CONFIGURATION

The bench system was set up to match the configuration of case number 12, with TERMPWR supplied and drivers located at the center. Shielded cables were 2.3 meters long, attached to boards using short (8.5 to 13 mm) flat ribbon cables, so that total cable length was 4.925m.

5.2.3 MEASUREMENT

I observed the waveforms of the REQ signal on the test boards at each cable position using a high speed digital oscilloscope with 1 megaohm, 7.5 picofarad probes (HP54111D).

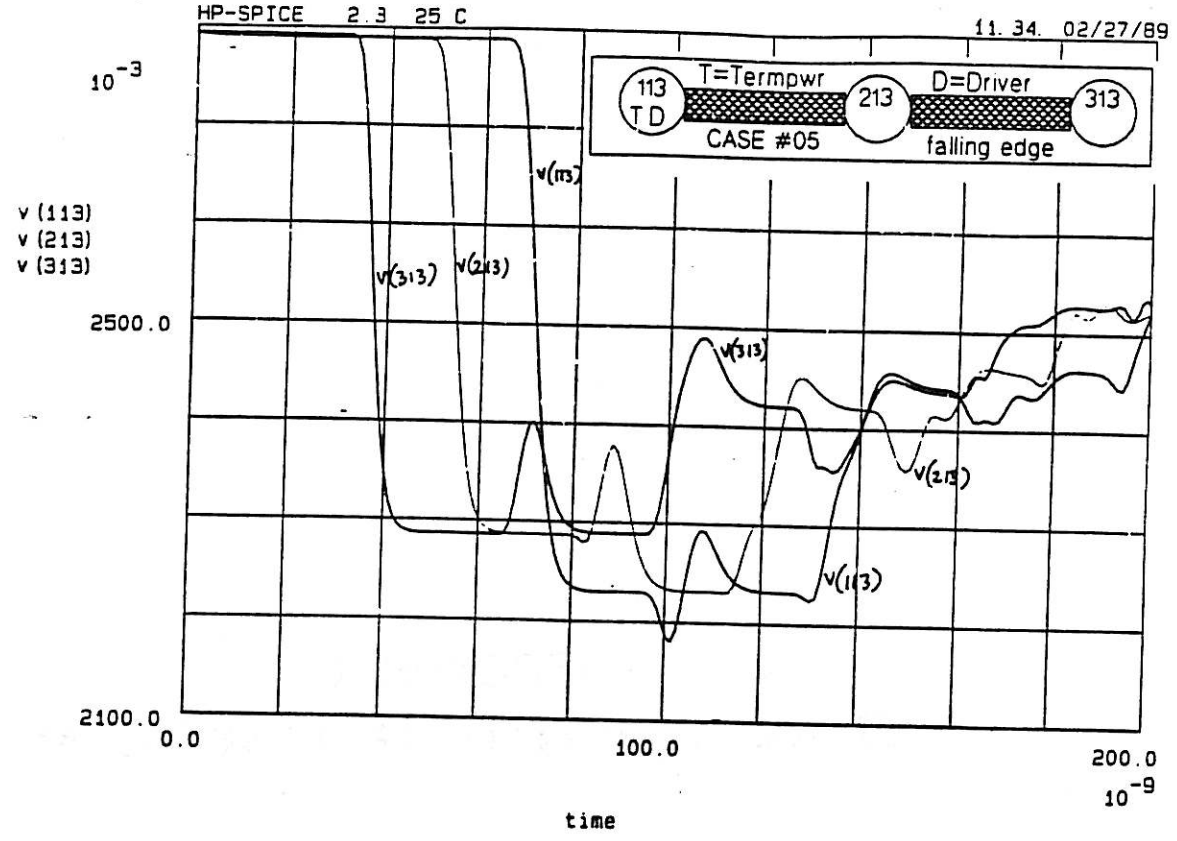
APPENDIX A
SAMPLE SPICE INPUT FILE -- CASE #9

```
SCSI Termpower Glitch Simulation (scsim09.cki rev 890227:1000)
#
#This version: copy of scsim05.cki with driver, termpwr in center.
#
#   Simulating all 18 lines.
#Bus type A: Two 3m. cables, loads at left, center, right.
#Termpwr = +5v,diode=1N5821, cap= 0 , center.
#"a" cables (long):  3 m, Z0=105, no stubs.
#"b" cables (short): none
#"c" cables (stubs): none
#Drivers on center, open collector, 2ns rise/fall time.
#Receivers = 25 pf, .1ma @ .4v, 1.4v switching, 100ua leak.
#Term = 220 up, 330 down, diode=none, cap=none.
#Test signal undriven.
#Data bus, MSG, I/O, C/D driven high to low.
#Other control signals undriven.
#
#                              Define bus as set of cables with left,right
#                              and middle positions for attachment.
Xpwr   1   2   3 pbusa           # Termpower
Xdb0 100 200 300 busa            # Data bus
Xdb1 101 201 301 busa
Xdb2 102 202 302 busa
Xdb3 103 203 303 busa
Xdb4 104 204 304 busa
Xdb5 105 205 305 busa
Xdb6 106 206 306 busa
Xdb7 107 207 307 busa
Xdbp 108 208 308 busa
Xmsg 109 209 309 busa
Xcdx 110 210 310 busa
Xiox 111 211 311 busa
Xatn 112 212 312 busa
Xreq 113 213 313 busa
Xack 114 214 314 busa
Xbsy 115 215 315 busa
Xsel 116 216 316 busa
Xrst 117 217 317 busa
Xdr0 200 500 driver                  # Drivers at center.
Xdr1 201 500 driver
Xdr2 202 500 driver
Xdr3 203 500 driver
Xdr4 204 500 driver
Xdr5 205 500 driver
Xdr6 206 500 driver
Xdr7 207 500 driver
Xdrp 208 500 driver
Xdrmsg 209 500 driver
Xdrcdx 210 500 driver
Xdriox 211 500 driver
VDRIVE 500 0 PWL(0 5 2N 0) # common source for drivers.
Xt001 100 1 term
Xt011 101 1 term
Xt021 102 1 term
Xt031 103 1 term
Xt041 104 1 term
Xt051 105 1 term
Xt061 106 1 term
Xt071 107 1 term
Xt081 108 1 term
```

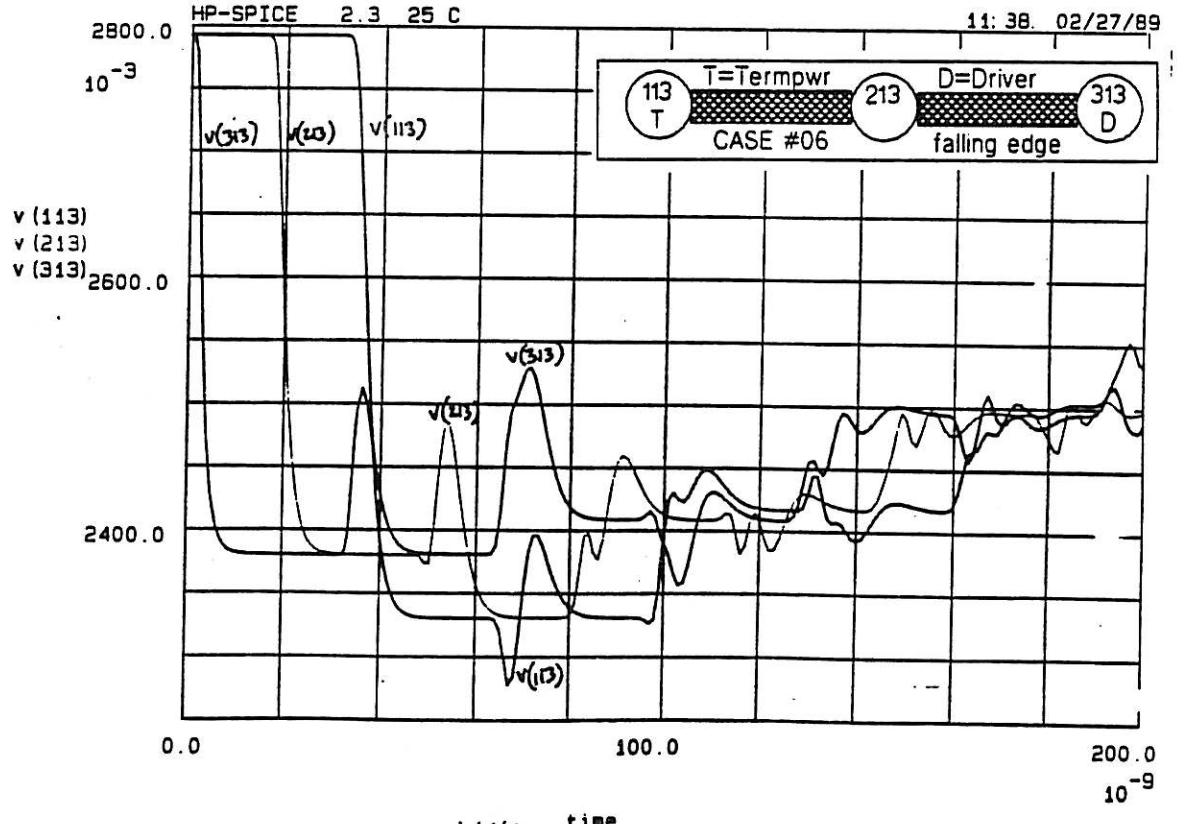
```
#
.MODEL cablea T TD=15.75N Z0=105
#
#
#                                   Describe open collector driver.
.SUBCKT driver %z %v
RDR %z 51 5.92
DDR 51 %v D1N5821
.ENDS
#
#
#                                   Describe termination nets.
.SUBCKT term %z %v
RPU %v %z 220
RPD %z 0 330
.ENDS
#
#                                   Diode models.
.MODEL D1N5821 D N=1.353 IS=.0001 IBV=1E-30
.TRAN 1N 200N 0
.GRAPH TRAN V(113) V(213) V(313) V(1) V(2) V(3) V(100) V(200) V(300)
.END
```

APPENDIX B
SIMULATION PLOTS OF TEST SIGNAL

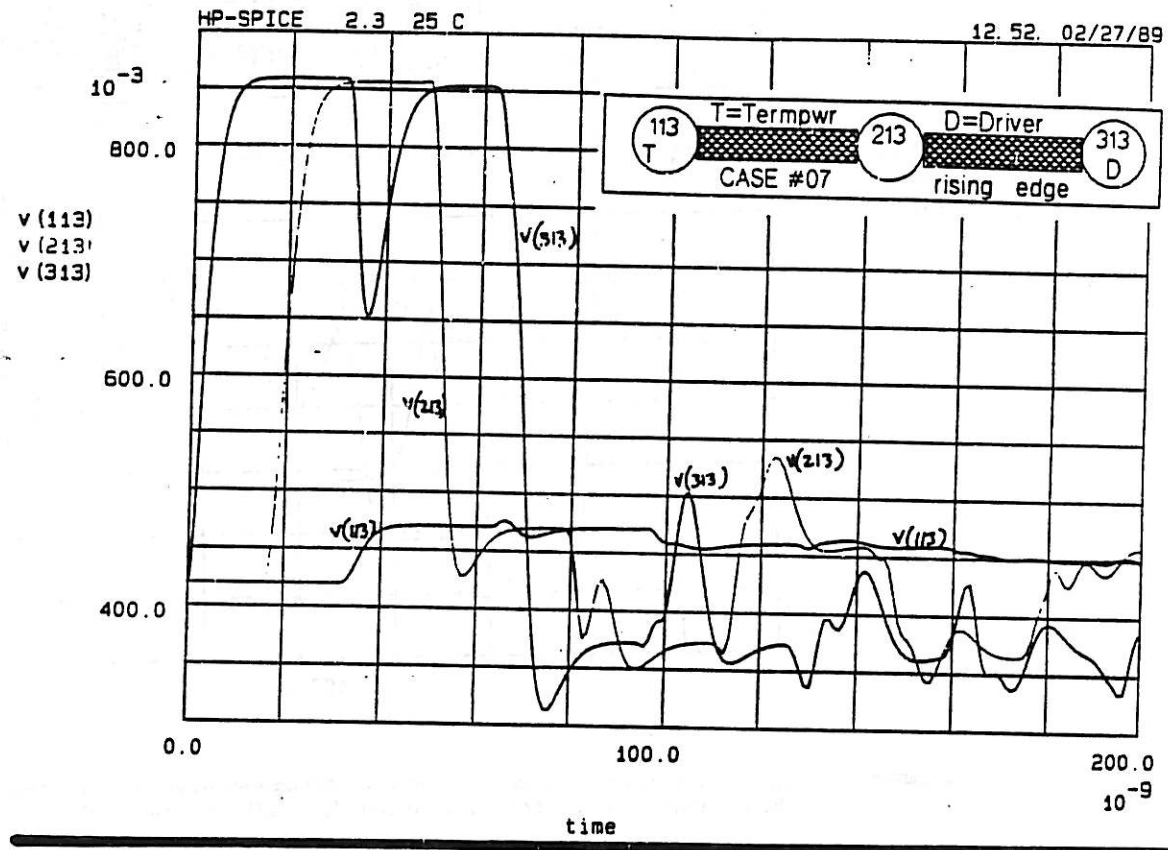
SCSI Termpower Glitch Simulation (scsim05.cki rev 890227.0900)



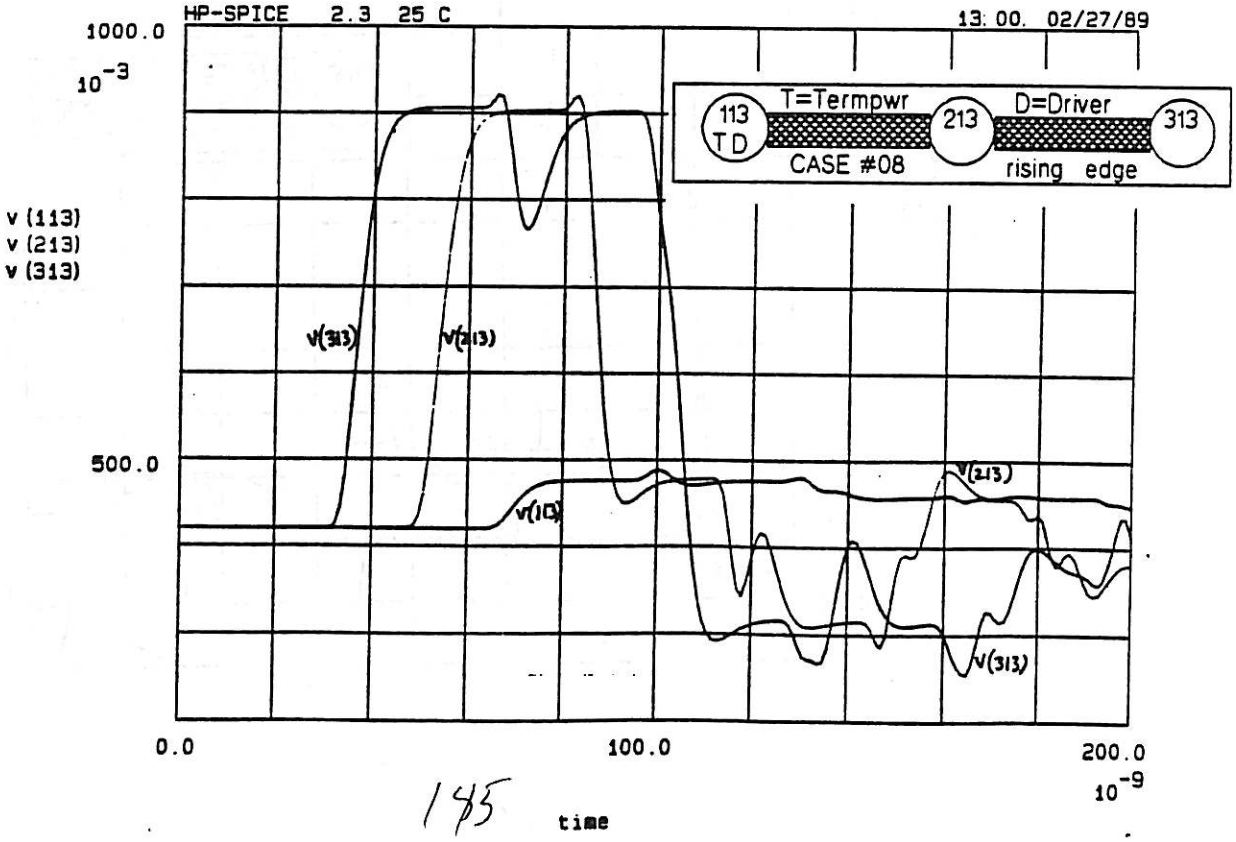
SCSI Termpower Glitch Simulation (scsim06.cki rev 890227:0940)



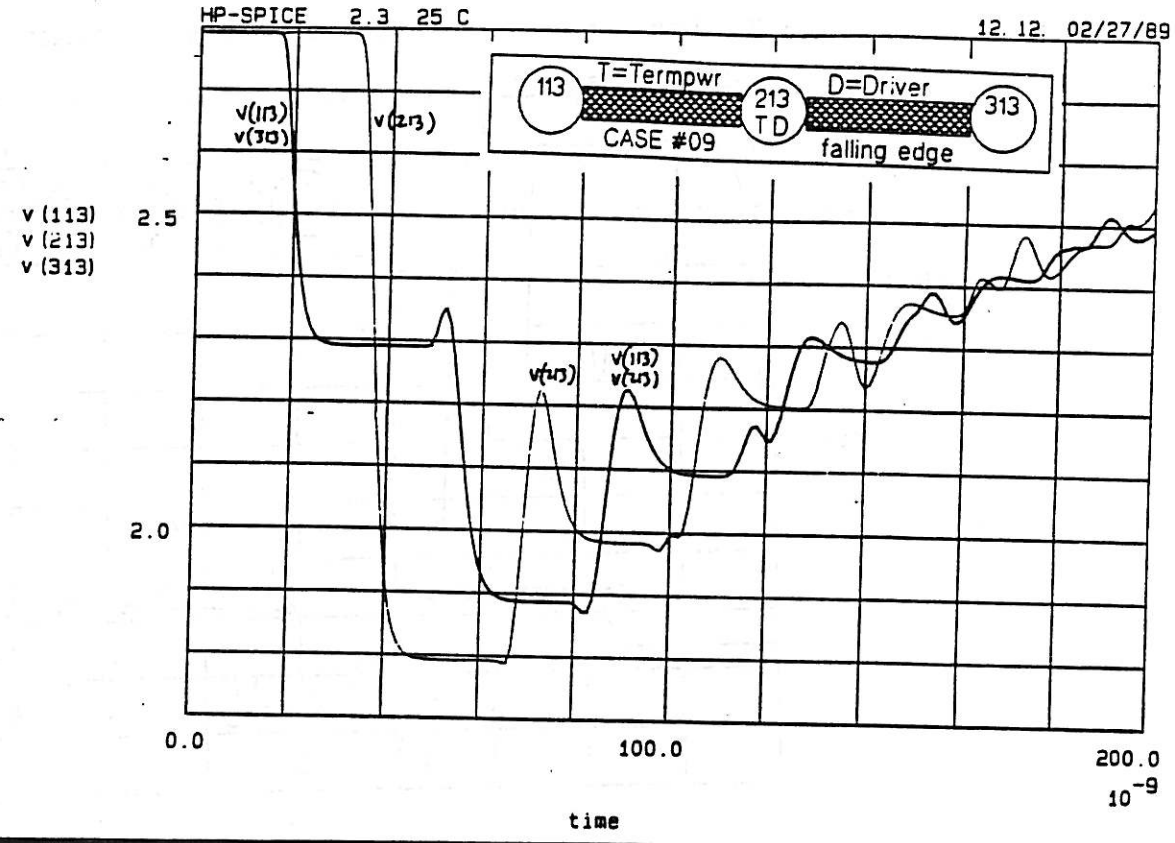
SCSI Termpower Glitch Simulation (scsim07.cki rev 890227: 1245)



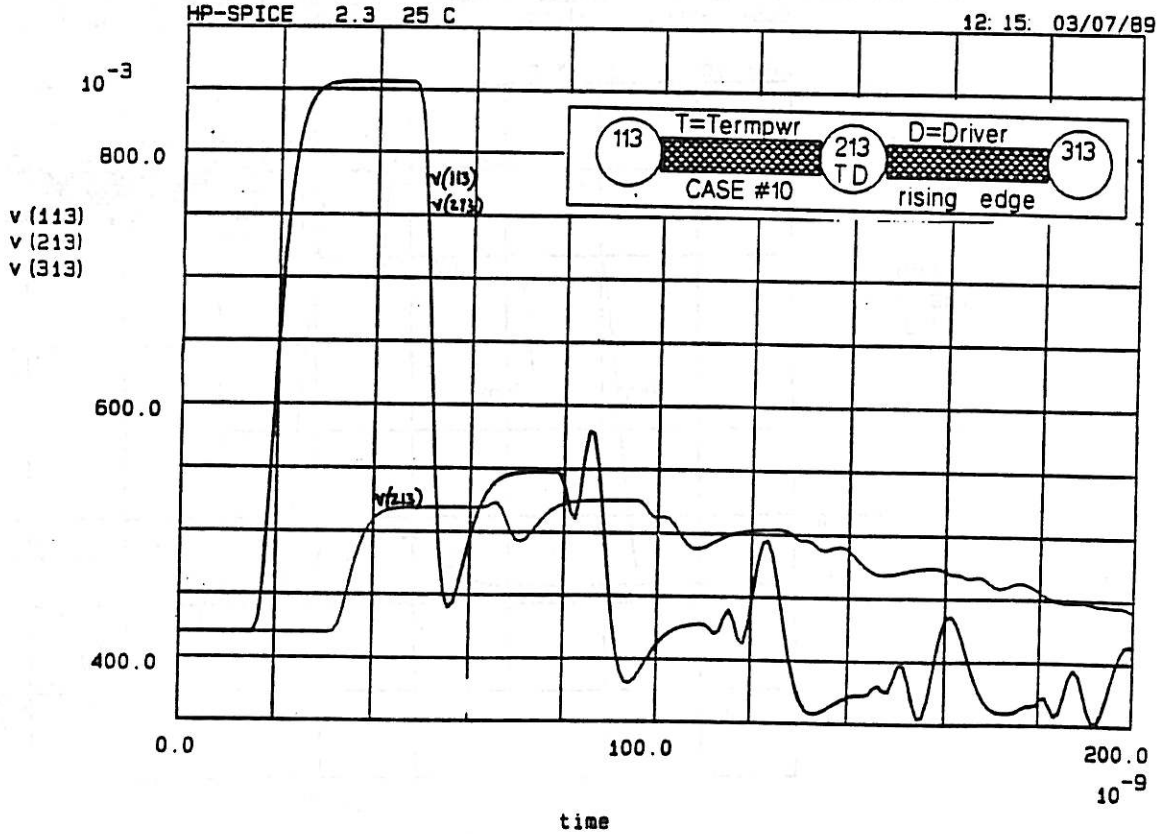
SCSI Termpower Glitch Simulation (scsim08.cki rev 890227: 1240)



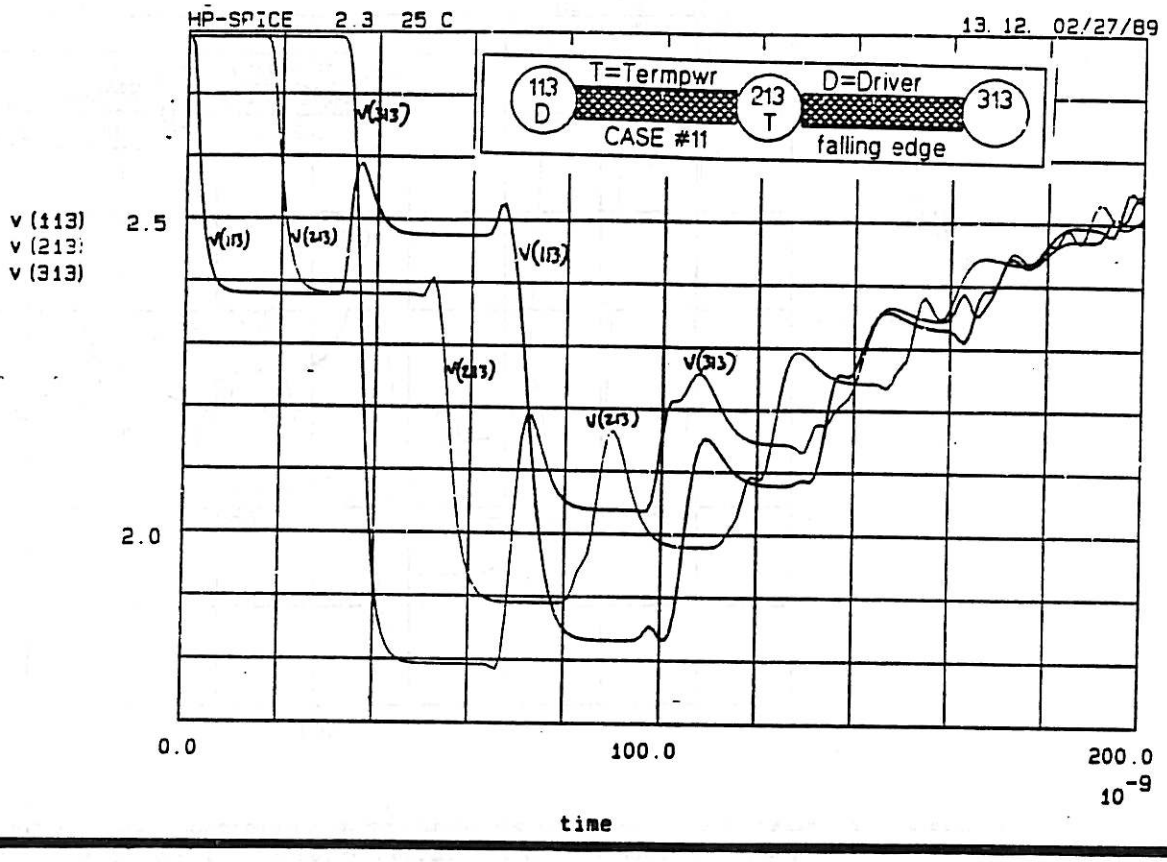
SCSI Termpower Glitch Simulation (scsim09.cki rev 890227.1000)



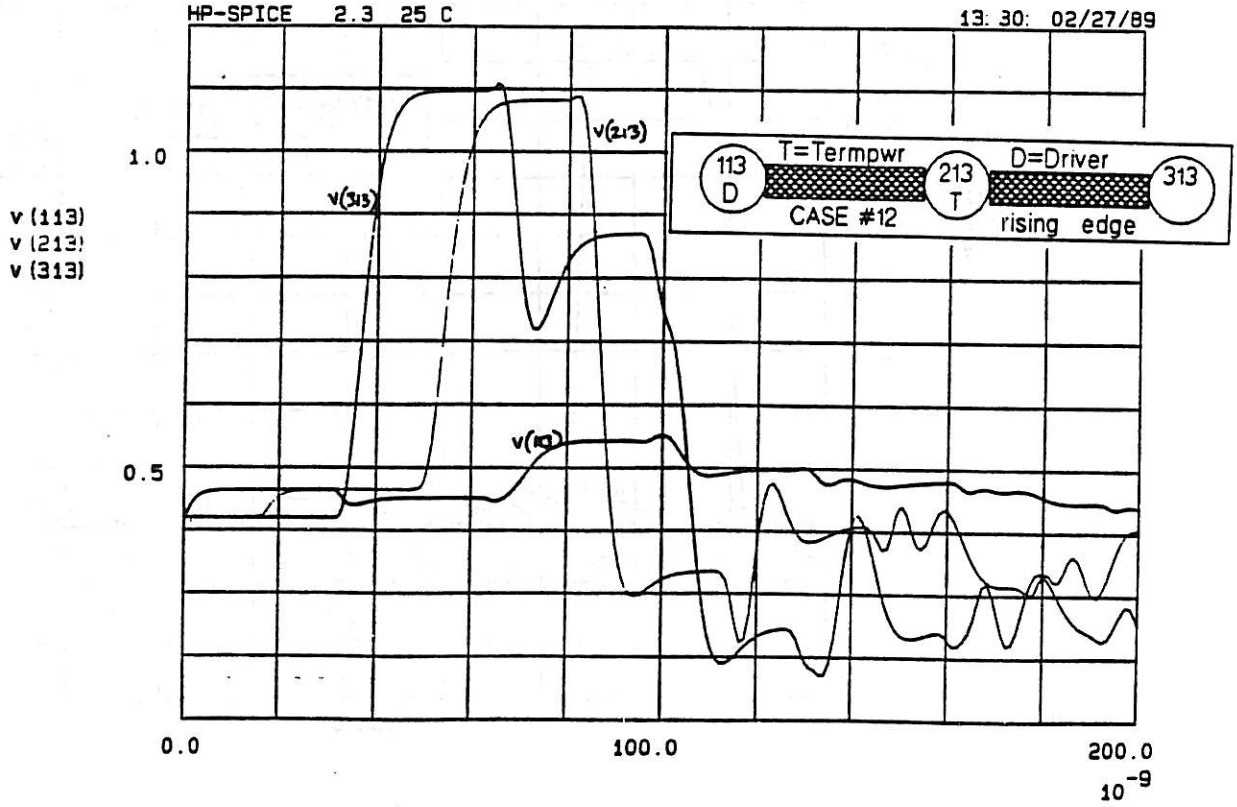
SCSI Termpower Glitch Simulation (scsim10.cki rev 890307.1215)



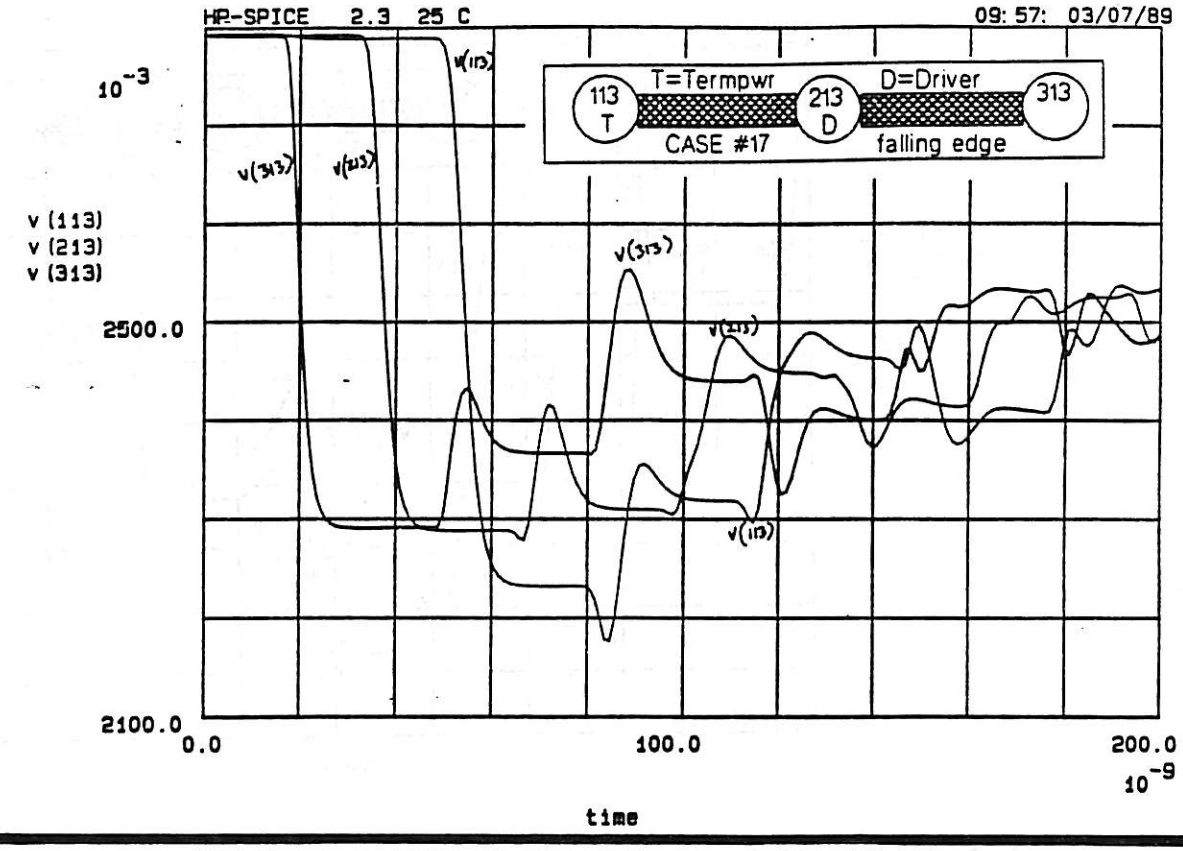
SCSI Termpower Glitch Simulation (scsim11.cki rev 890227.1300)



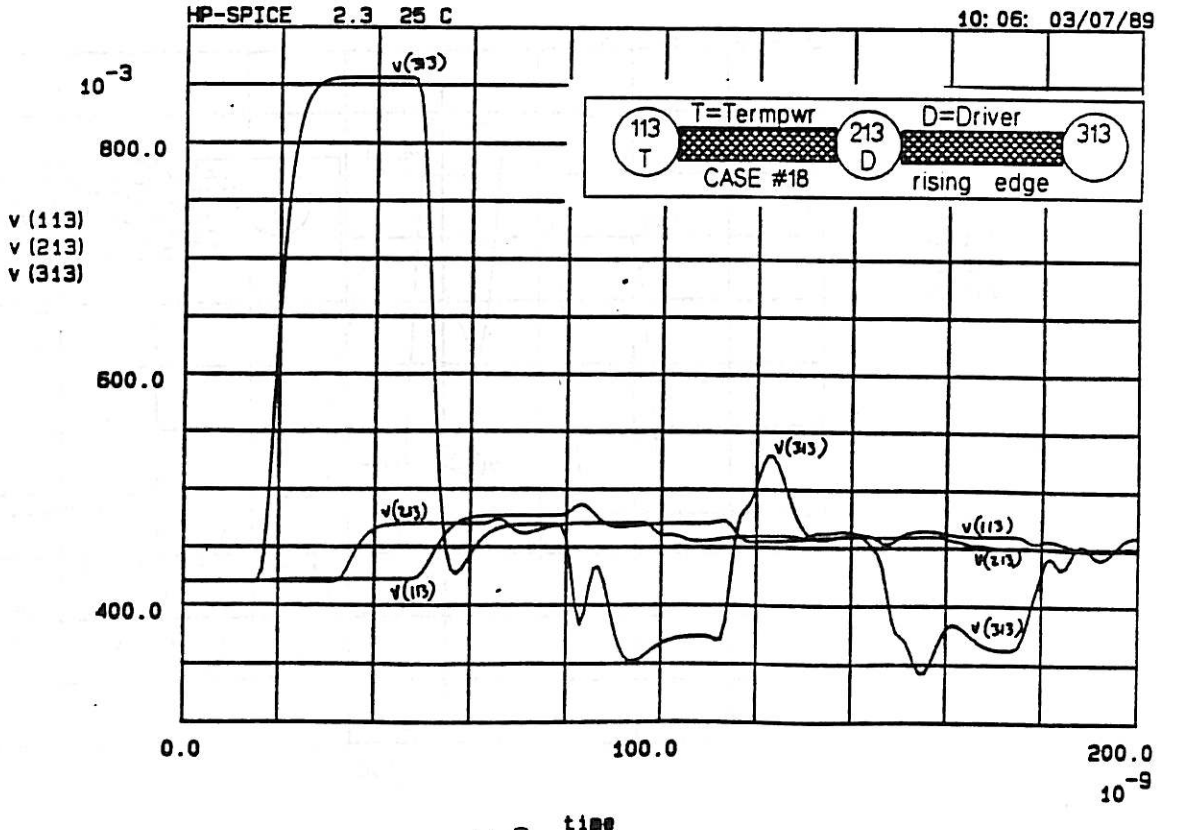
SCSI Termpower Glitch Simulation (scsim12.cki rev 890227.1305)



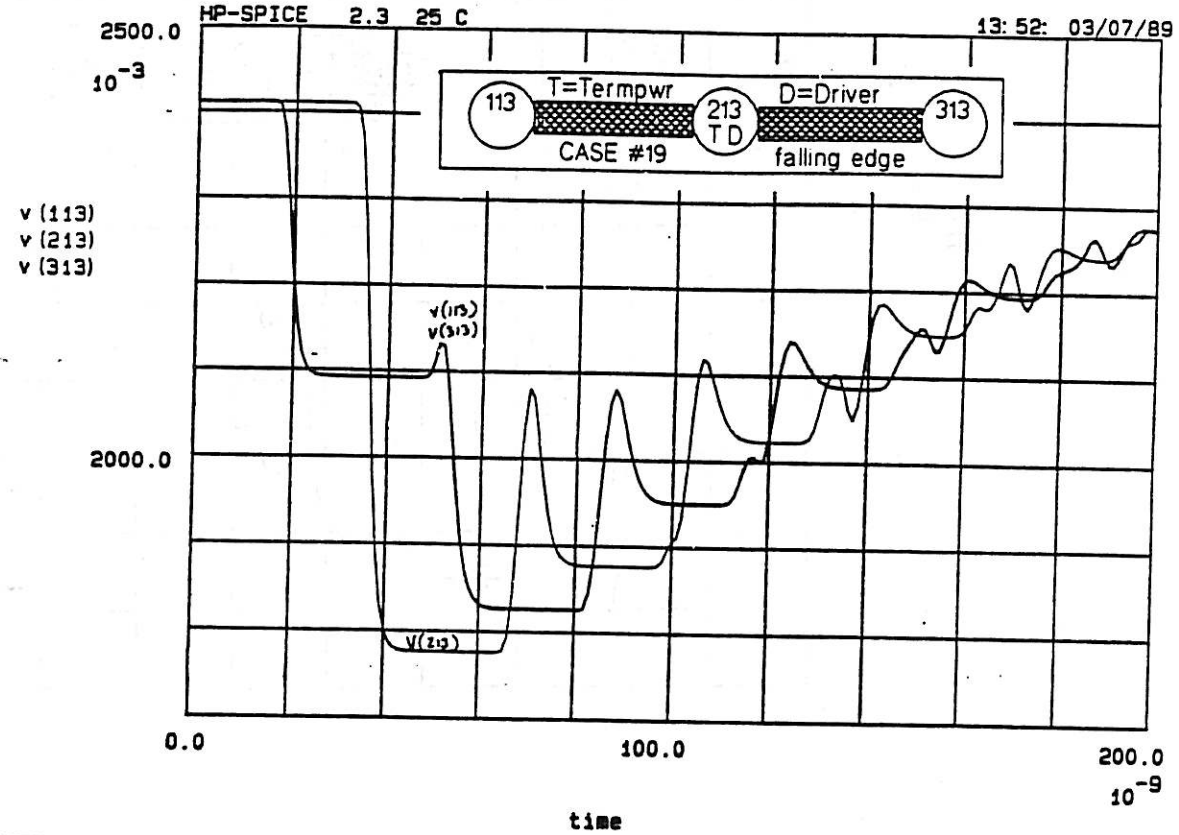
SCSI Termpower Glitch Simulation (scsim17.cki rev 890307: 0945)



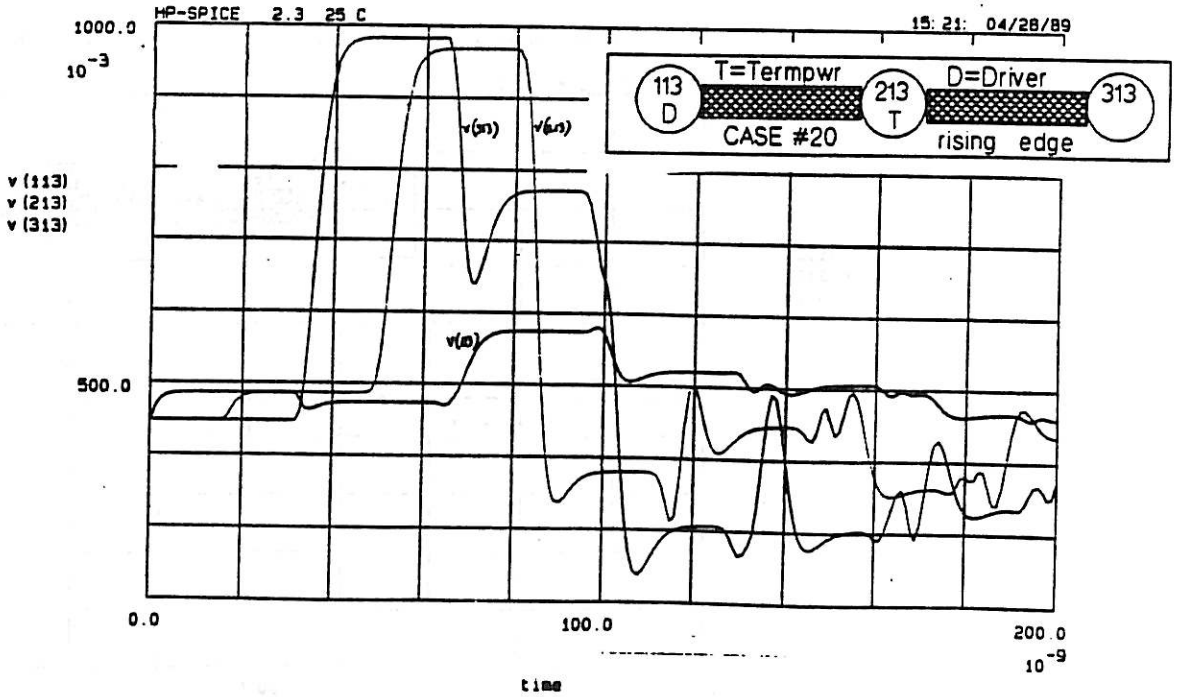
SCSI Termpower Glitch Simulation (scsim18.cki rev 890307: 0955)



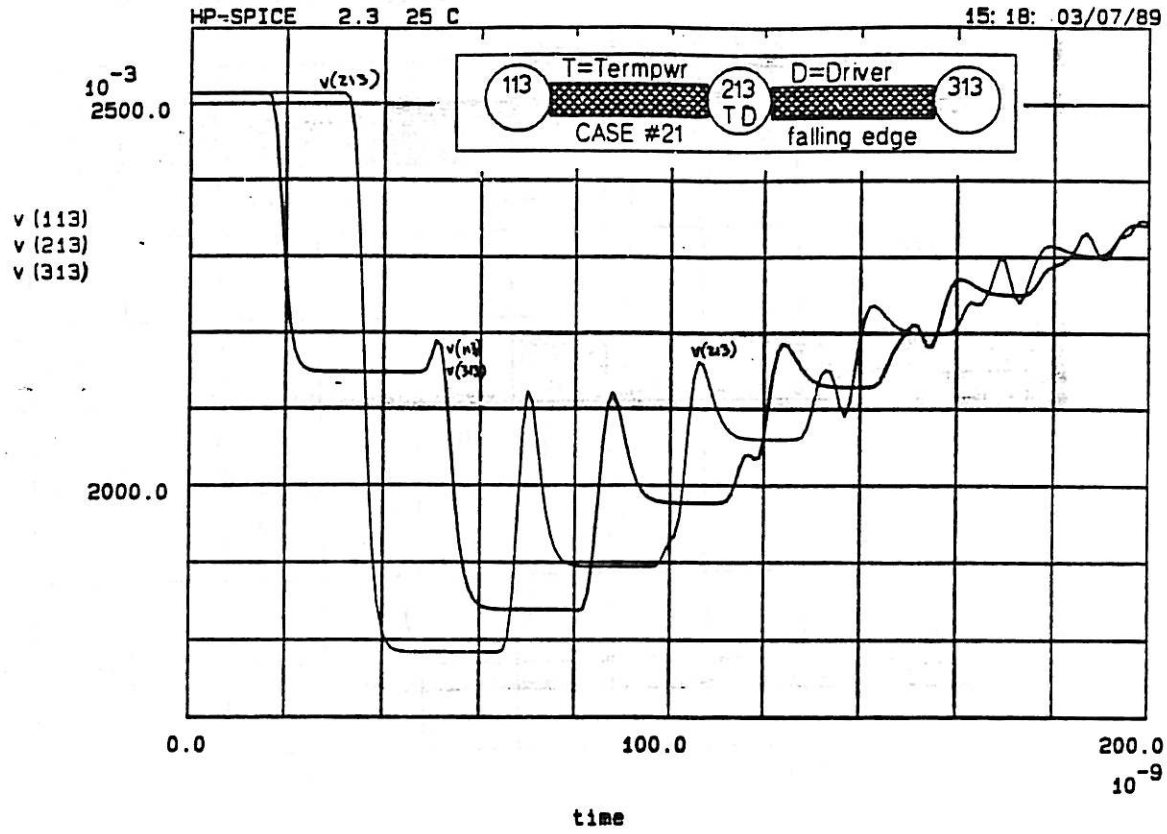
SCSI Termpower Glitch Simulation (scsim19.cki rev 890307: 1340)



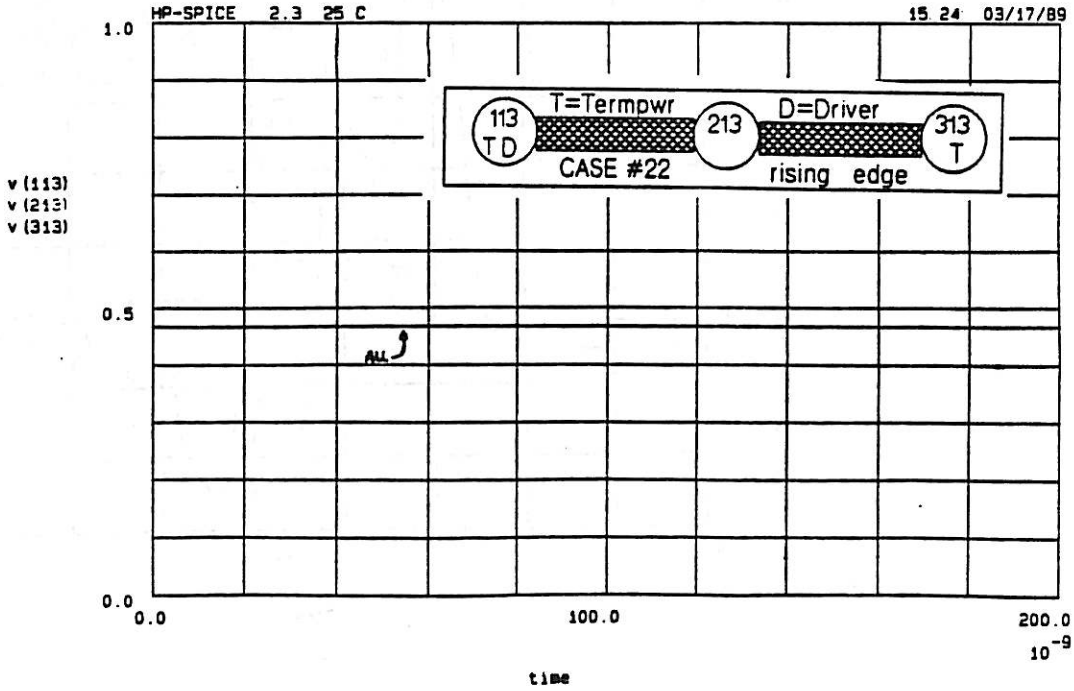
SCSI Termpower Glitch Simulation (scsim20.cki rev 890428. 1520)



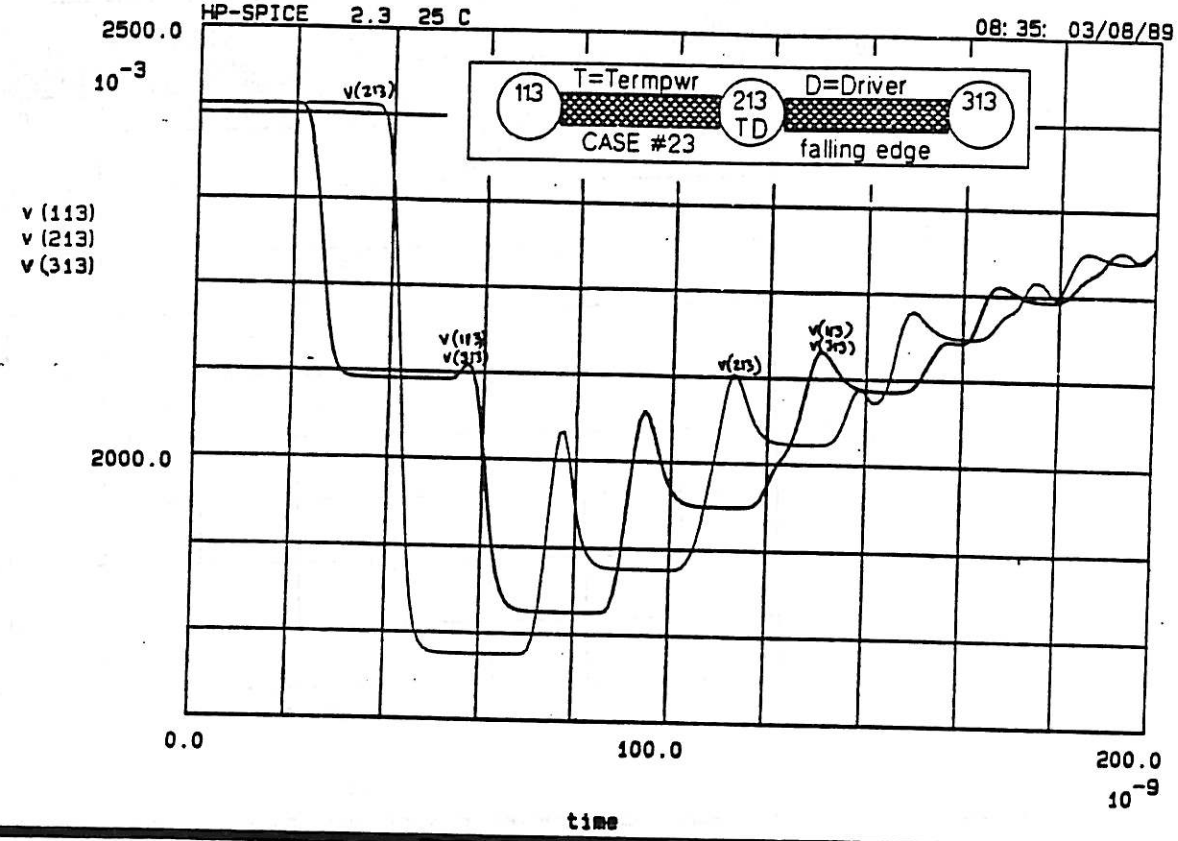
SCSI Termpower Glitch Simulation (scsim21.cki rev 890307: 1520)



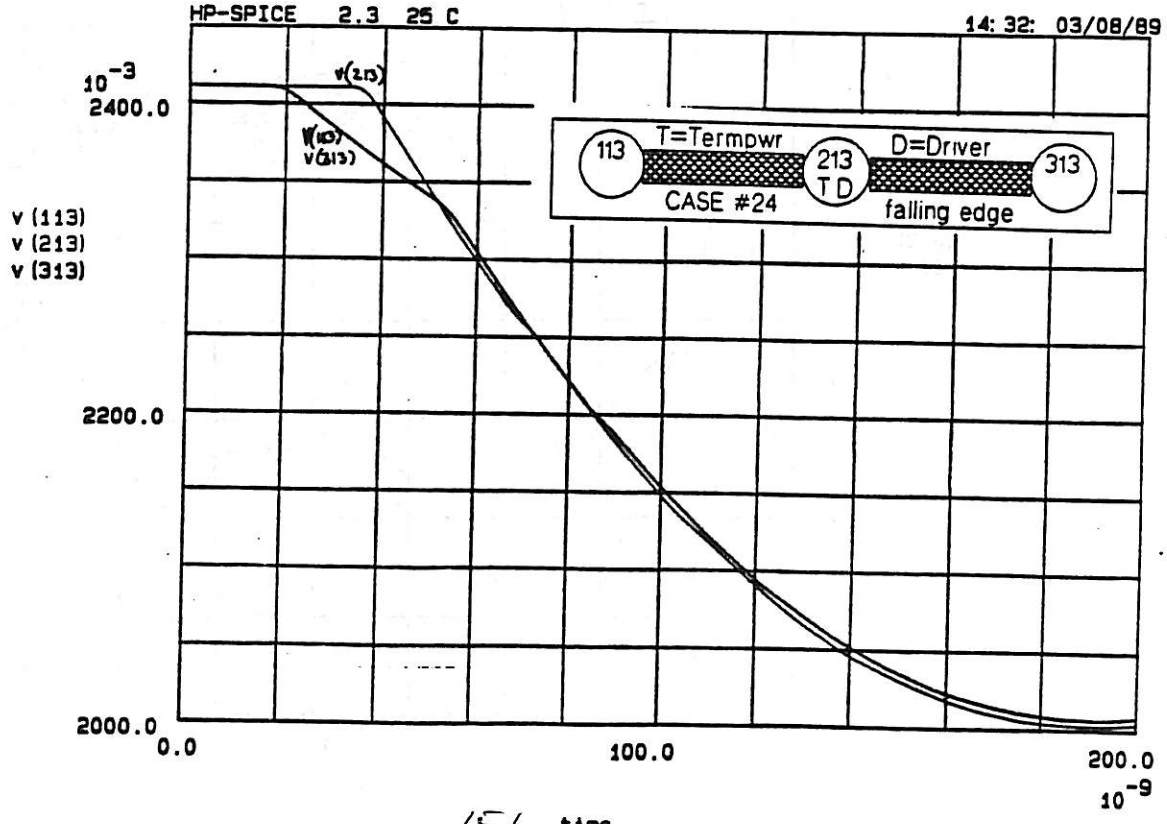
SCSI Termpower Glitch Simulation (scsim22.cki rev 890318. 1510)



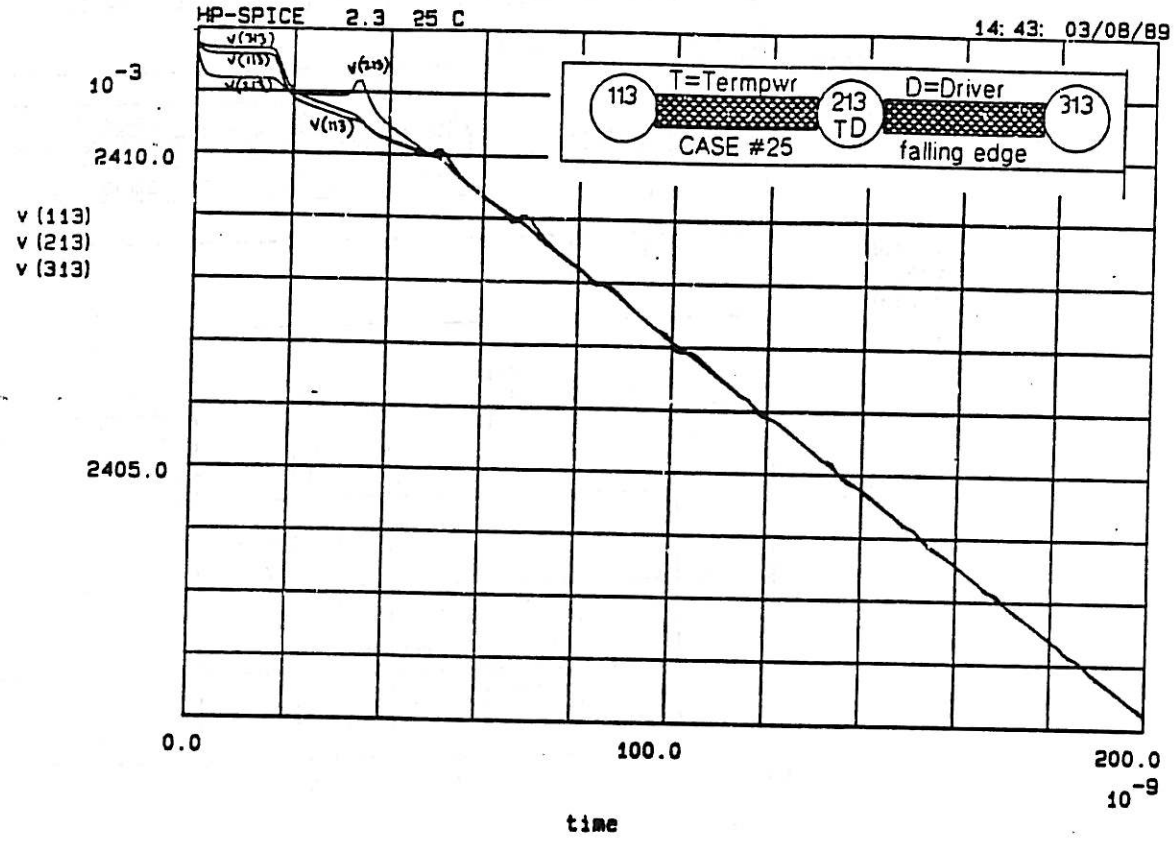
SCSI Termpower Glitch Simulation (scsim23.cki rev 890308: 0830



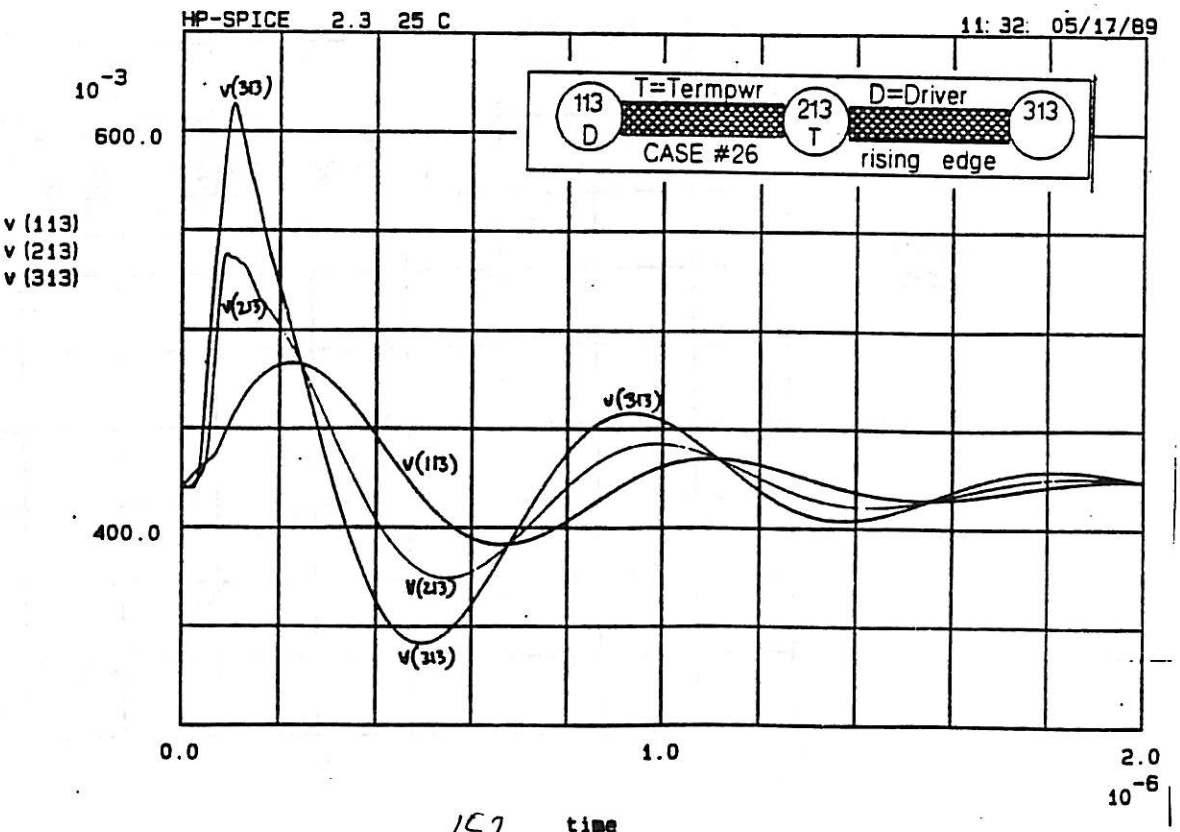
SCSI Termpower Glitch Simulation (scsim24.cki rev 890308: 1430)

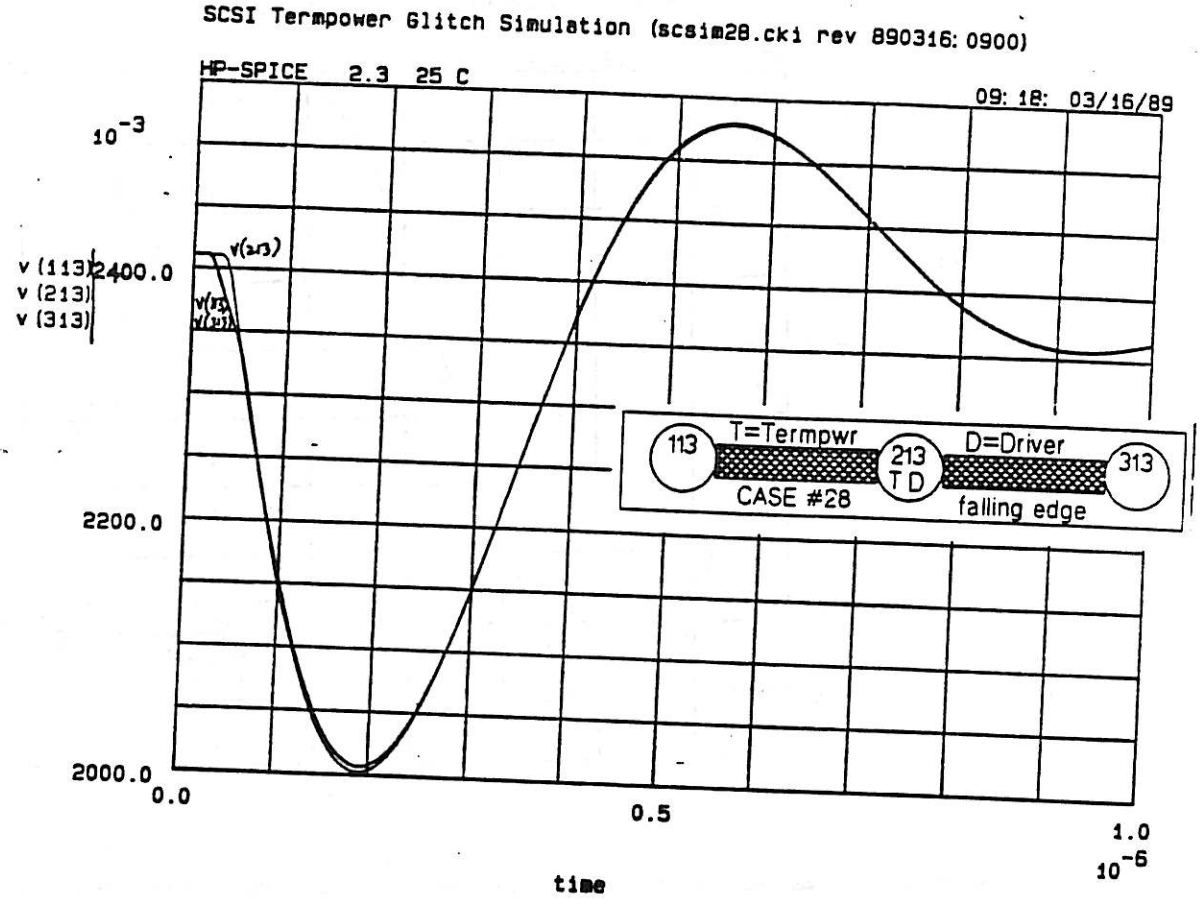


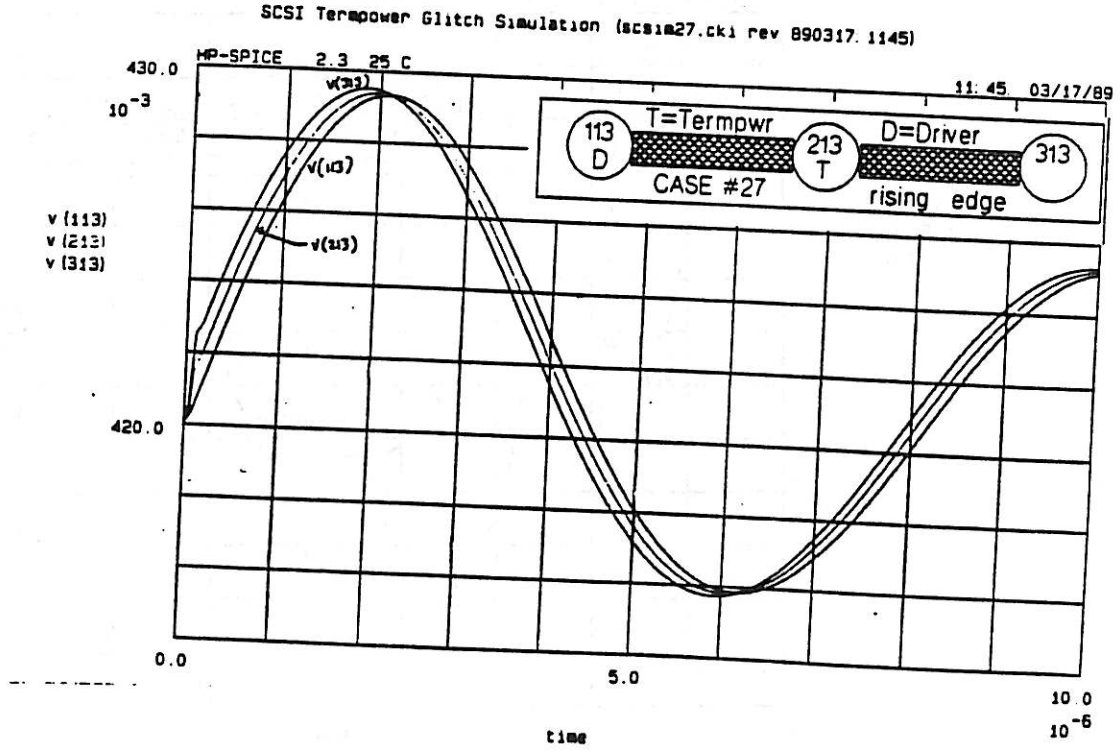
SCSI Termpower Glitch Simulation (scsim25.cki rev 890308: 1430)



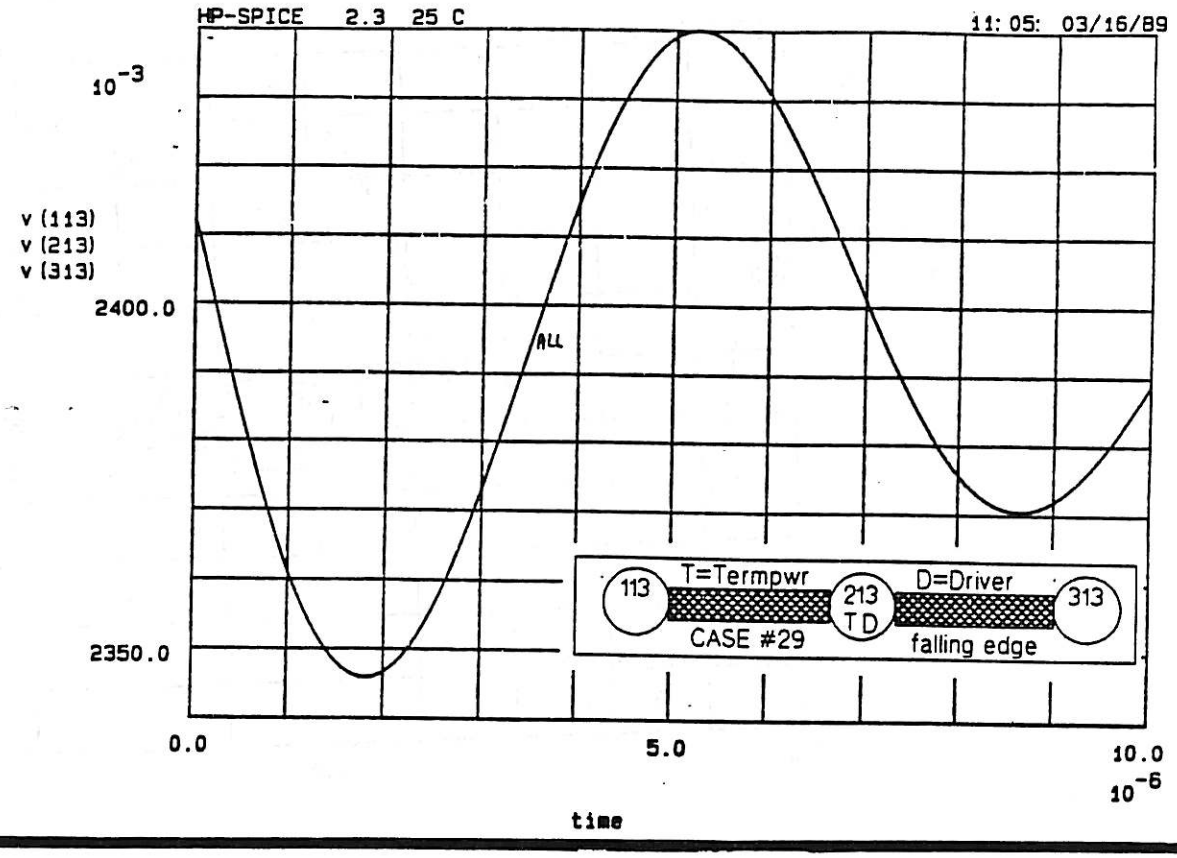
SCSI Termpower Glitch Simulation (scsim26.cki rev 890317: 1205)



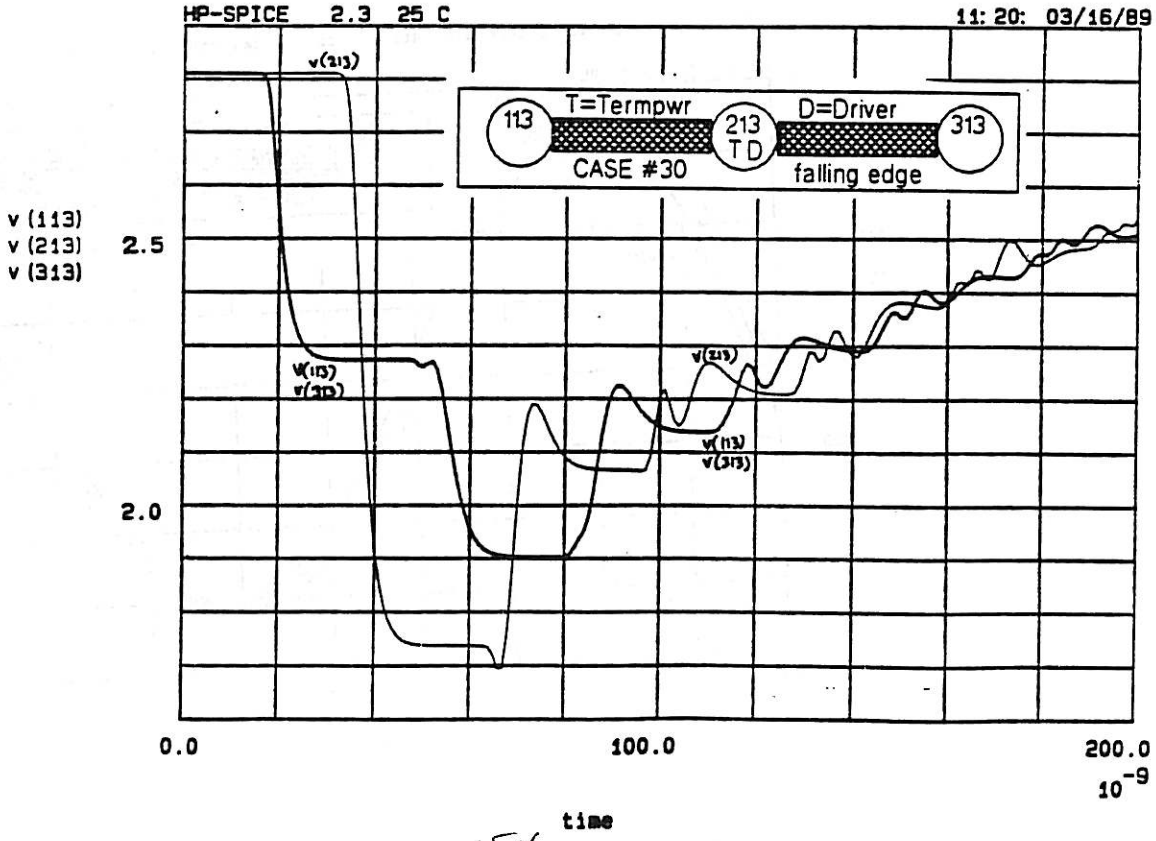

SCSI Termpower Glitch Simulation (scsim28.cki rev 890316: 0900)
HP-SPICE 2.3 25 C
09: 18: 03/16/89
10^-3
v (113)
v (213)
v (313)
2400.0
2200.0
2000.0
0.0
0.5
1.0
10^-6
time
113
T=Termpwr
213
T D
D=Driver
313
CASE #28
falling edge


SCSI Termpower Glitch Simulation (scsim27.cki rev 890317. 1145)
HP-SPICE 2.3 25 C
11: 45 03/17/89
430.0
10^-3
v (113)
v (213)
v (313)
420.0
0.0
5.0
10.0
10^-6
time
113
D
T=Termpwr
213
T
D=Driver
313
CASE #27
rising edge

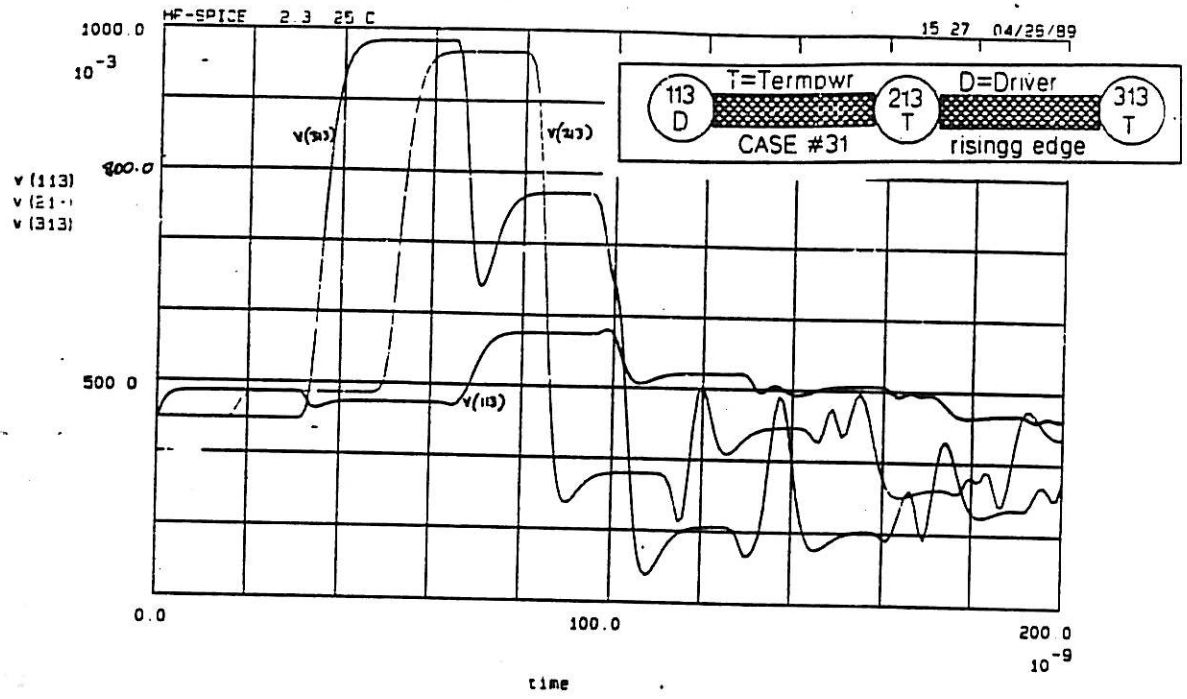
SCSI Termpower Glitch Simulation (scsim29.cki rev 890316:0930).



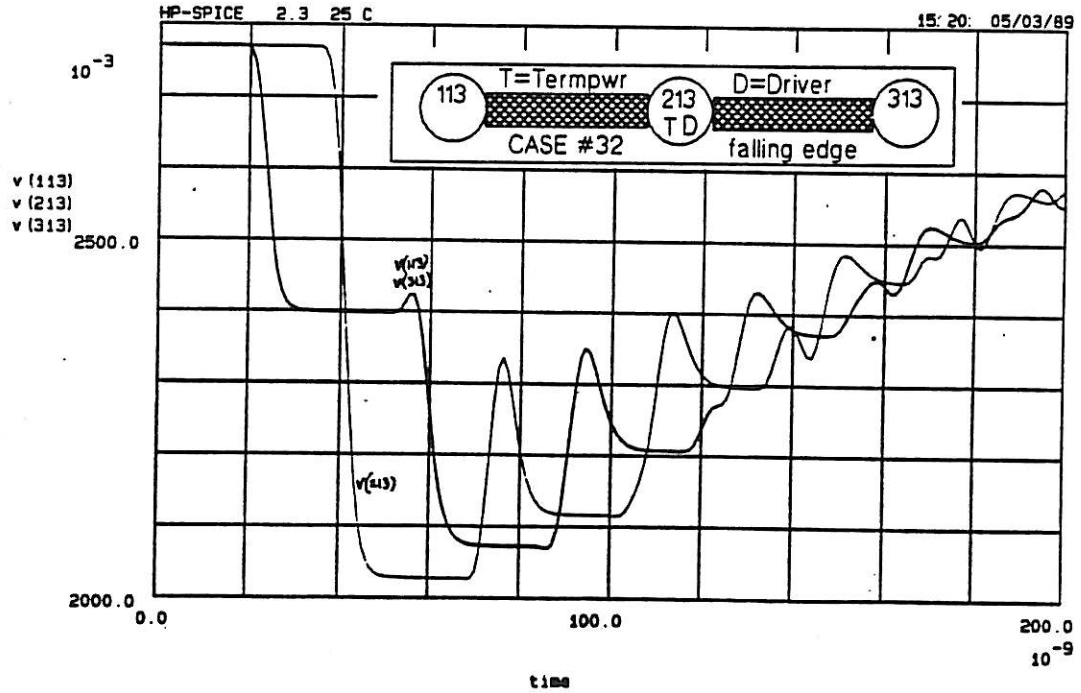
SCSI Termpower Glitch Simulation (scsim30.cki rev 890316:0910)



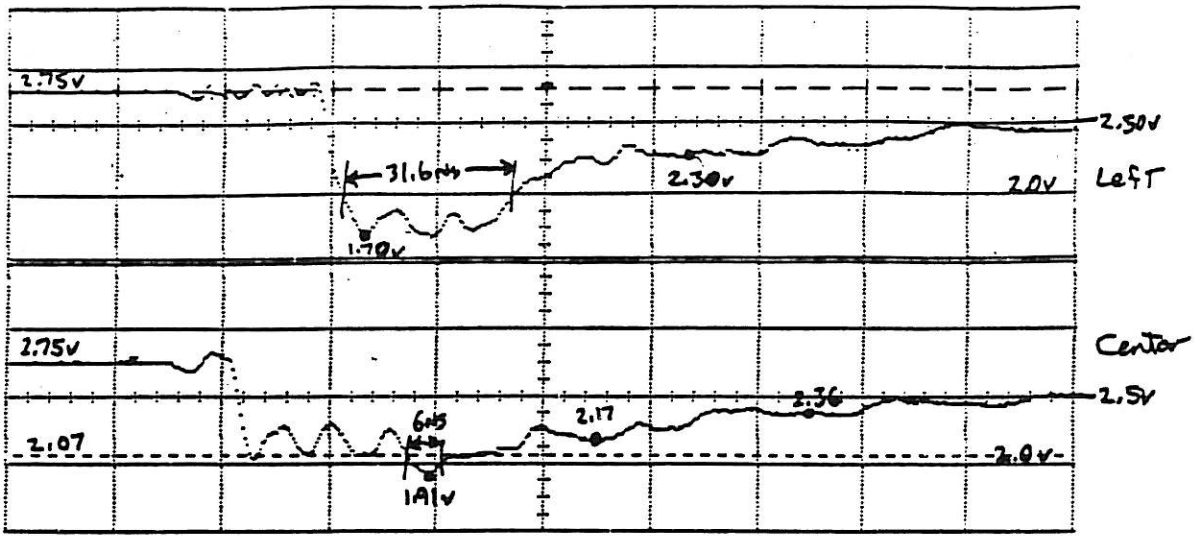
SCSI Termpower Glitch Simulation (scsim31.ckt rev 890428 1525)



SCSI Termpower Glitch Simulation (scsim32.ckt rev 890503.1500)



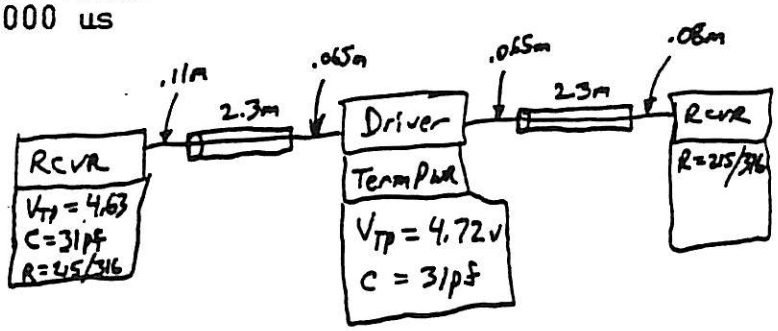
APPENDIX C
SCOPE PLOT OF BENCH TEST SIGNAL



-35.600 ns 64.400 ns 164.400 ns

Ch. 1	= 50.00 mVolts/div	Offset	= 250.5 mVolts
Ch. 2	= 50.00 mVolts/div	Offset	= 250.0 mVolts
Timebase	= 20.0 ns/div	Delay	= -35.600 ns
Delta V	= -68.50 mVolts		
Vmarker1	= 275.0 mVolts	Vmarker2	= 206.5 mVolts

Trigger mode : Edge
On Neg. Edge on Trig3
Trigger Levels
Trig3 = 0.000 Volts
Holdoff = 4.00000 us



BENCH TEST SCOPE PLOTS 890503:14/gm

890503:14
C_{RCVR} = 31pf (Incl. scope probes)
V_{TP} = 4.72 center
4.63 left