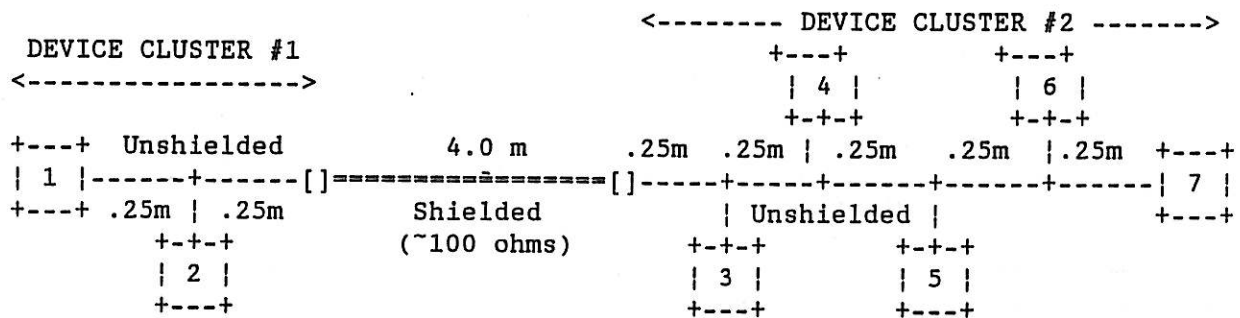


TO: X3T9.2 Committee
 FROM: Kurt Chan, Hewlett-Packard
 SUBJECT: Preliminary Cable Test Results

X3T9.2-89-018 R0
 1/12/89

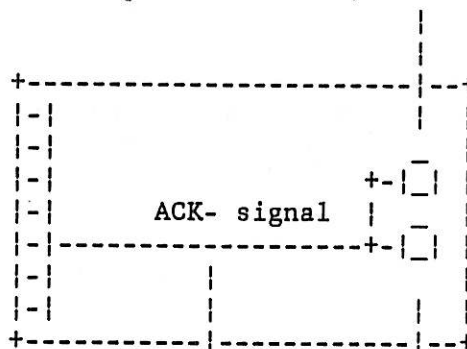
In document 88-150 I outlined some tests that would be performed on SCSI-2 cables (single-ended, open-collector). The objective was to make a comparison under worst-case conditions between SCSI-1 cables and new SCSI-2 proposed cables.

The configuration under test consisted of 7 "devices":



Each device consisted of:

Switchable termination network (potentiometers) ---+



SCSI-1 device connector ---+
 (2 rows, 25 pins/row)

3.5" 30 AWG wire over ground plane ---+

Fixed capacitor (12 pF - 22 pF) -----+

When testing the high-density cables, cluster 1 was connected using 30 AWG AMP cable (labelled "75 ohm"), and cluster 2 was connected using 28 AWG AMP cable (labelled "93 ohm"). All of the SCSI-1 cable was standard 50-mil ribbon cable (approx 90 ohms).

TERMPWR was initially fixed at 3.9V across the entire bus per my worst-case TERMPWR analysis found in document X3T9.2-88-165. Termination resistors initially were set to 220/330. The driver consisted of an open-drain 2N6659 FET with 5ns rise time driven by an HP 8165A Programmable Signal Generator. The signal under test is pin 38 (ACK).

After building instrumentation to measure "faults" on the bus, the following observations were made:

1. It was difficult to make hysteresis of the ECL receivers immune to variations in frequency, especially at the high end, and especially because such tight control over the hysteresis voltage was necessary.
2. In most cases, errors were either continuous or never occurred. Therefore, our hope to come up with error rate metrics to evaluate cable schemes showed little promise. Errors nearly always occurred on every clock cycle, or not at all. Also, both subtle (50 millivolt) and gross (>.5V) violations of the spec are interpreted identically using the counter approach.

Oscilloscope traces proved to be the most useful tools for showing signal quality. An HP 54111D sampling scope (1 GHz) was used to document the results.

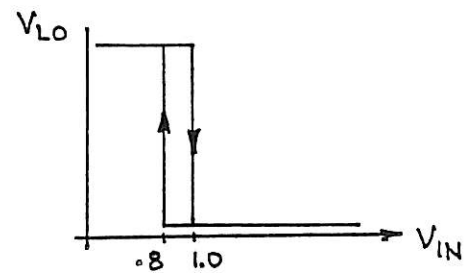
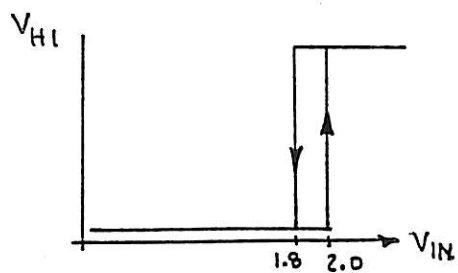
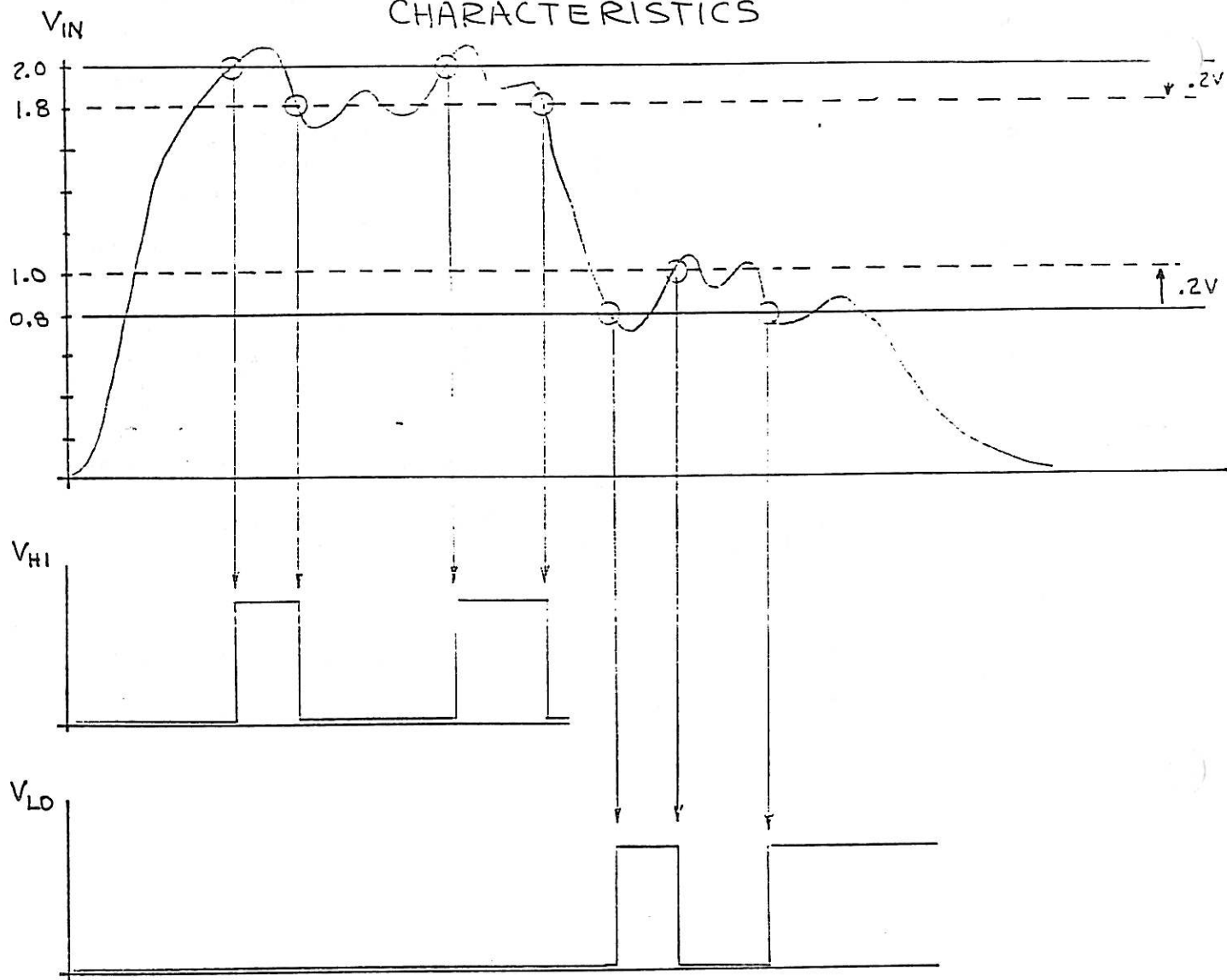
CONCLUSIONS

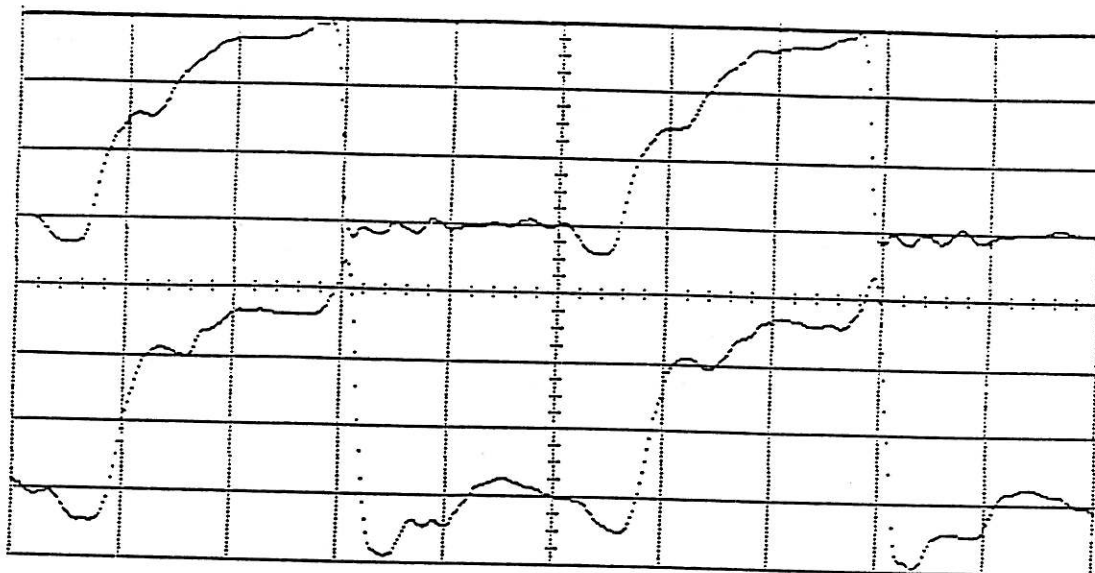
Some preliminary conclusions can be made, even before other cables are submitted for testing:

1. Neither one of the cable systems passes 50 ns (10 MHz) pulses reliably, even with only one target and one initiator connected. However, 10 MHz signals CAN be passed reliably if worst-case parameters are not used (shorter cable lengths, higher TERMPWR, fewer devices, shorter stubs, etc.). All subsequent tests were performed at 5 MHz unless otherwise specified. Margin testing was not done to determine the combination of parameters that yielded reliable 10 MHz operation.
2. Device capacitance differences of 10 pF makes a measurable difference in the signal quality. In some cases devices with 17 pF passed where devices with 27 pF failed.
3. Introducing worst-case 10% resistors caused the system to fail. If a system is experiencing worst-case TERMPWR along with worst-case receiver thresholds, 242/297 terminators will reduce the high noise margin enough to make the system unreliable. See 88-165 for an analysis - 1% is preferred, 5% should be mandatory.
4. The devices experiencing the worst reflections seemed to consistently be those two devices nearest to the border between the shielded and unshielded cables (devices 2 at .25 meters and device 3 at 4.75 meters). Other configurations may differ - the waveform shape is highly dependent on (and sensitive to changes in) device spacing, device capacitance, etc.

5. Paul Boulay's 2.6V TERMPWR scheme with 100 ohm pullups showed significant improvement in some cases. More testing will be made on this recent proposal by Paul.
6. Most modern TTL receivers have an intrinsic (Schottky) diode at their inputs which helps to clamp negative-going signals. However, MOS parts lack this intrinsic diode and therefore may experience voltages as low as -2 Volts. By clamping the large initial negative swing, the subsequent positive reflection is also subdued, which may prevent spurious assertions. It is HIGHLY recommended that some form of high-speed clamping diode (in discrete form - 1N5711 or 1N6263) be used with MOS devices which do not have this intrinsic diode.
7. TERMPWR should be kept as high as possible. In 89-165, I showed that with 5% resistors and .1 mA sink current, bus signals will only release to 2.09 volts DC (under worst-case conditions). Keeping TERMPWR as high as possible is one method of improving the high-level noise margin.
8. The AMP cables tested were negligibly more sensitive to some worst-case parameters than the SCSI-1 cables. However, the results will continue to be preliminary until other vendors submit samples for testing so I can do A-B-C comparisons. Future testing will focus on:
 - o crosstalk sensitivity,
 - o 2.6V to 100 ohm termination,
 - o sensitivity to stub length (on real copper foil traces over ground plane)
 - o repeating existing tests with samples from other vendors.

SCSI SINGLE-ENDED RECEIVER CHARACTERISTICS





10MHz
.5m, AM

#1

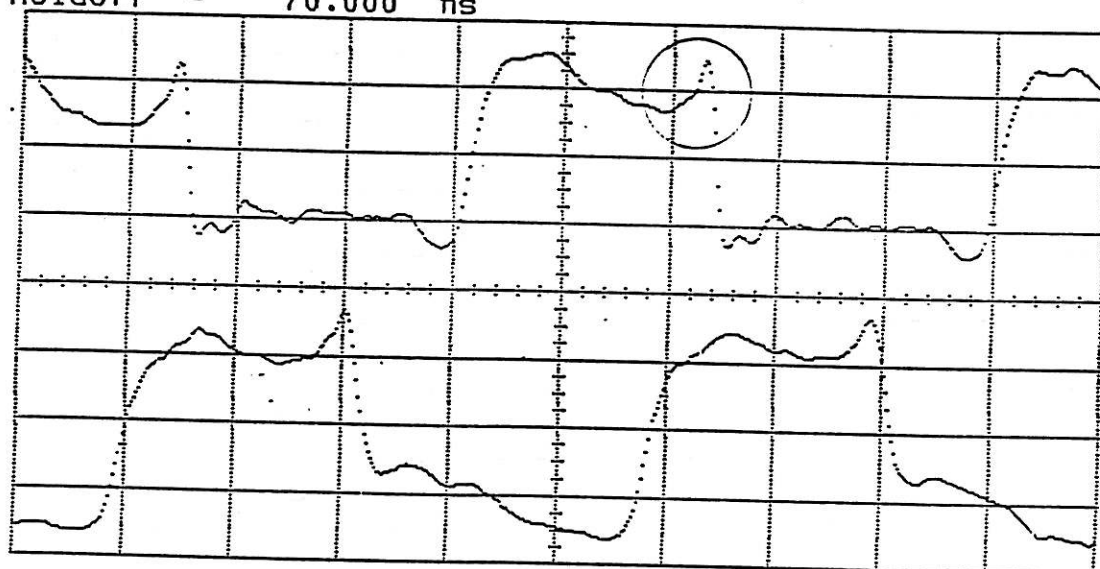
#7

-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 20.0 ns/div

Offset = -100.0 mVolts
Offset = 300.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 90.00 mVolts
Holdoff = 70.000 ns



10MHz
Config #2, Am
Two devices on
(no loads)

#1

#7

-20.000 ns 80.000 ns 180.000 ns

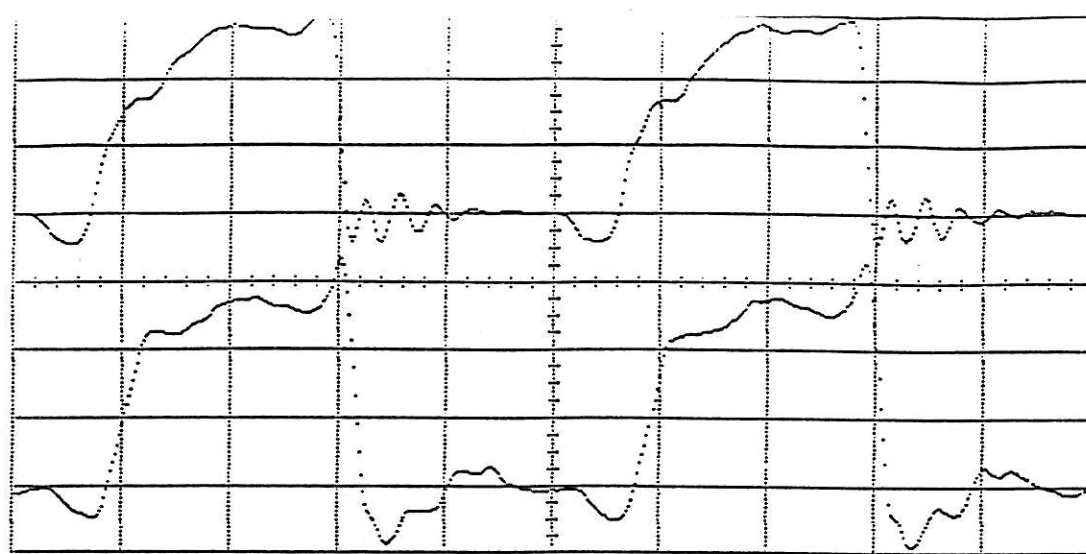
Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 20.0 ns/div

Offset = -100.0 mVolts
Offset = 300.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 90.00 mVolts
Holdoff = 70.000 ns

145

10MHz
.5m STD

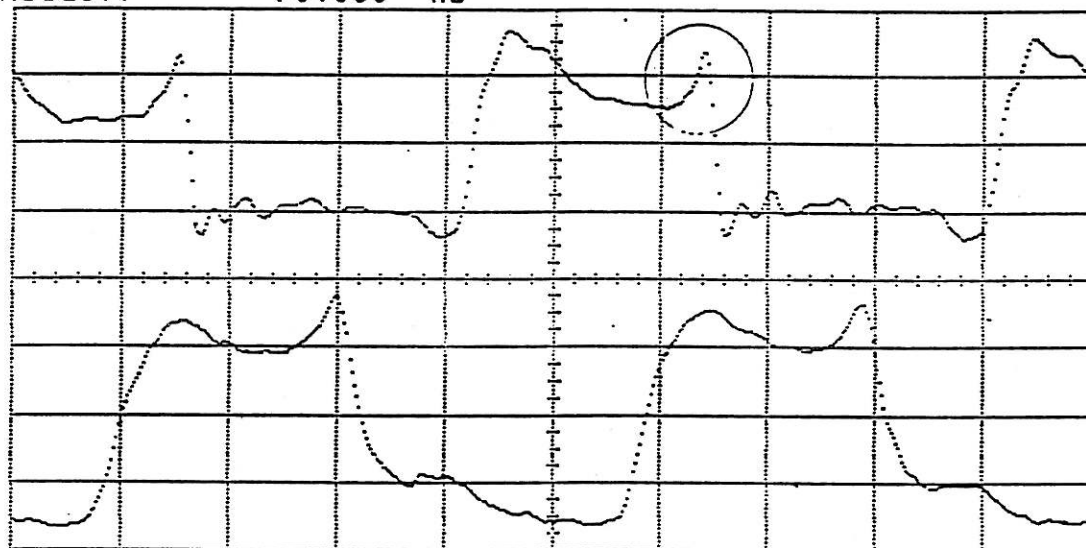


-20.000 ns 80.000 ns 180.000 ns

Ch. 1	=	100.0 mVolts/div	Offset	=	-100.0 mVolts
Ch. 2	=	100.0 mVolts/div	Offset	=	300.0 mVolts
Timebase	=	20.0 ns/div	Delay	=	-20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 90.00 mVolts
Holdoff = 70.000 ns

10MHz
Config #2, D
Two devices onl

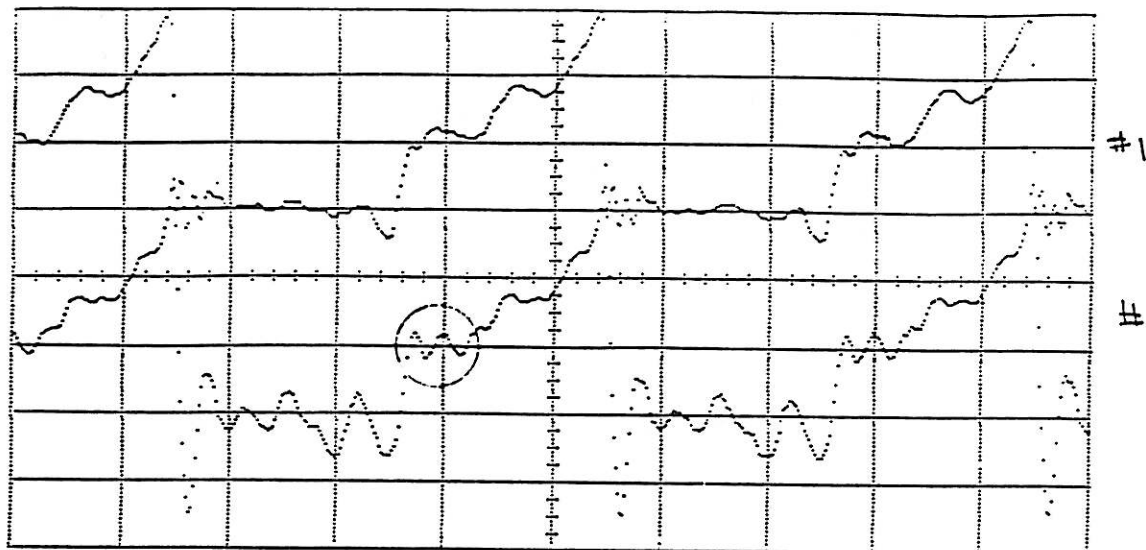


-20.000 ns 80.000 ns 180.000 ns

Ch. 1	=	100.0 mVolts/div	Offset	=	-100.0 mVolts
Ch. 2	=	100.0 mVolts/div	Offset	=	300.0 mVolts
Timebase	=	20.0 ns/div	Delay	=	-20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 90.00 mVolts
Holdoff = 70.000 ns

5 MHz
Config #2 (full)
STD
Type 1 loads

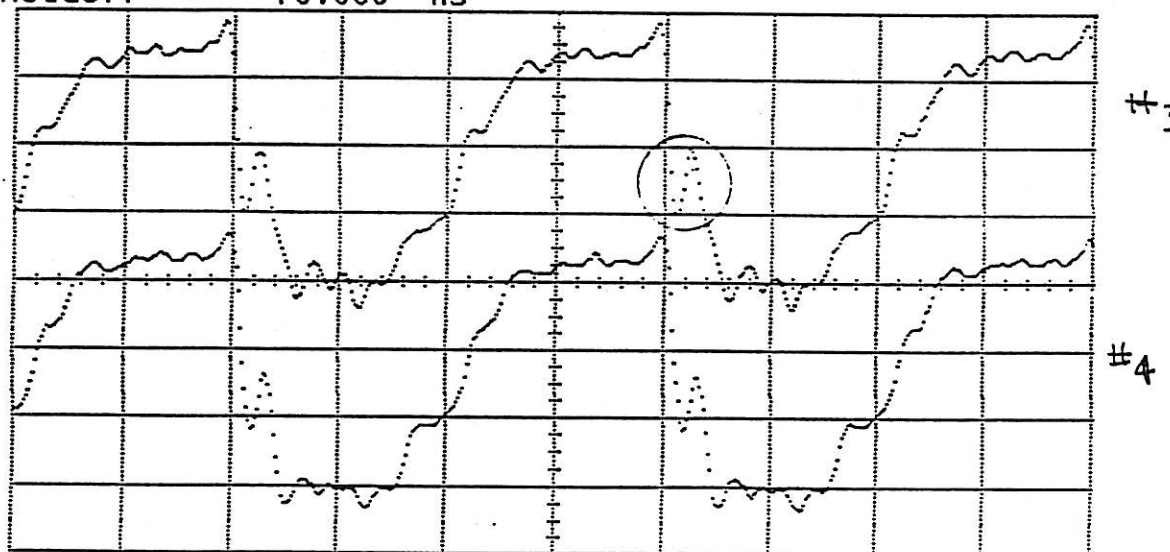


-20.000 ns 230.000 ns 480.000 ns

Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 50.0 ns/div

Offset = -100.0 mVolts
Offset = 200.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

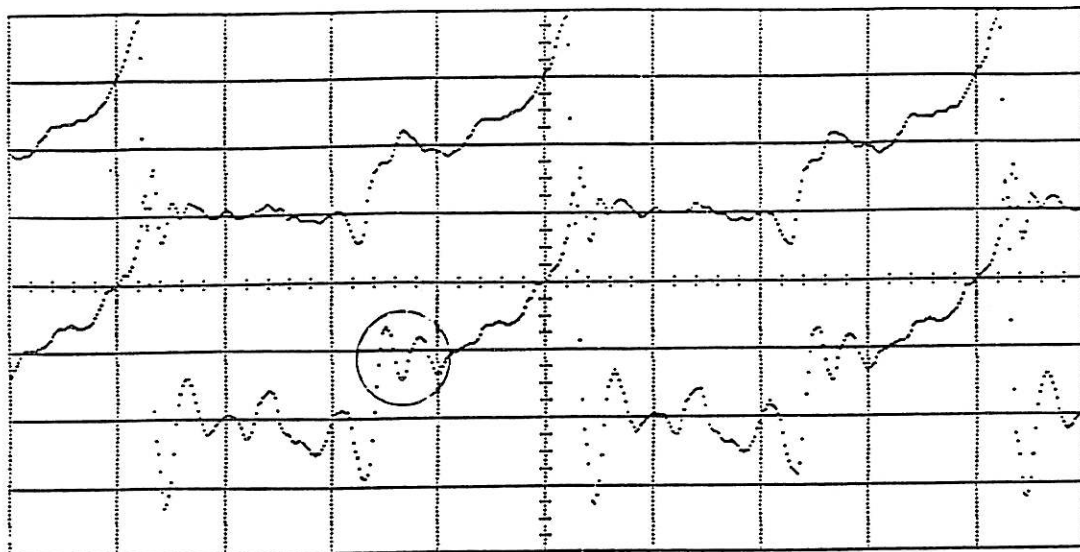


-20.000 ns 230.000 ns 480.000 ns

Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 50.0 ns/div

Offset = -100.0 mVolts
Offset = 200.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

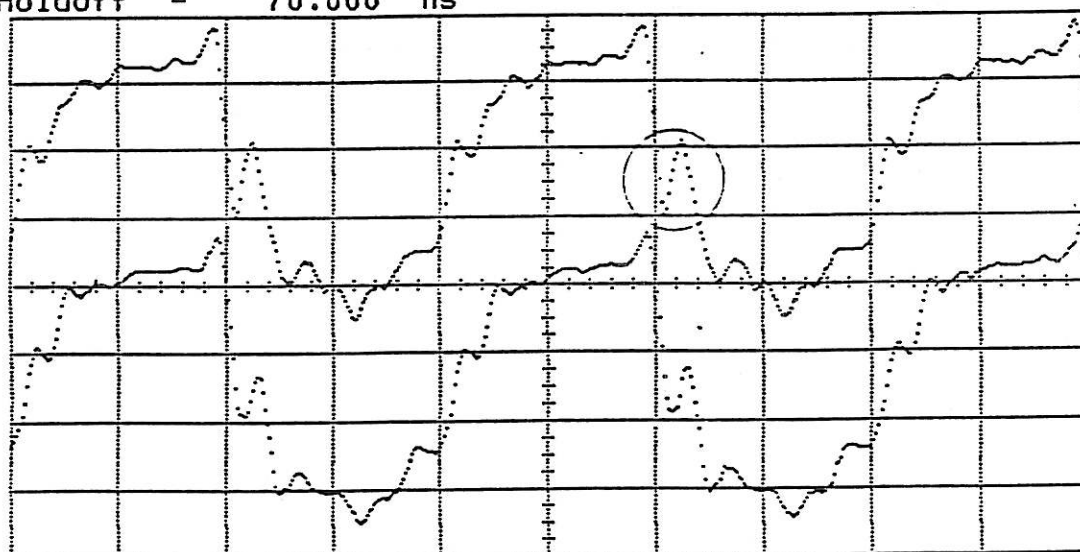


5 MHz
Config #2 (full)
AMP
Type 1 loads

-20.000 ns 230.000 ns 480.000 ns

Ch. 1	=	100.0 mVolts/div	Offset	=	-100.0 mVolts
Ch. 2	=	100.0 mVolts/div	Offset	=	200.0 mVolts
Timebase	=	50.0 ns/div	Delay	=	-20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

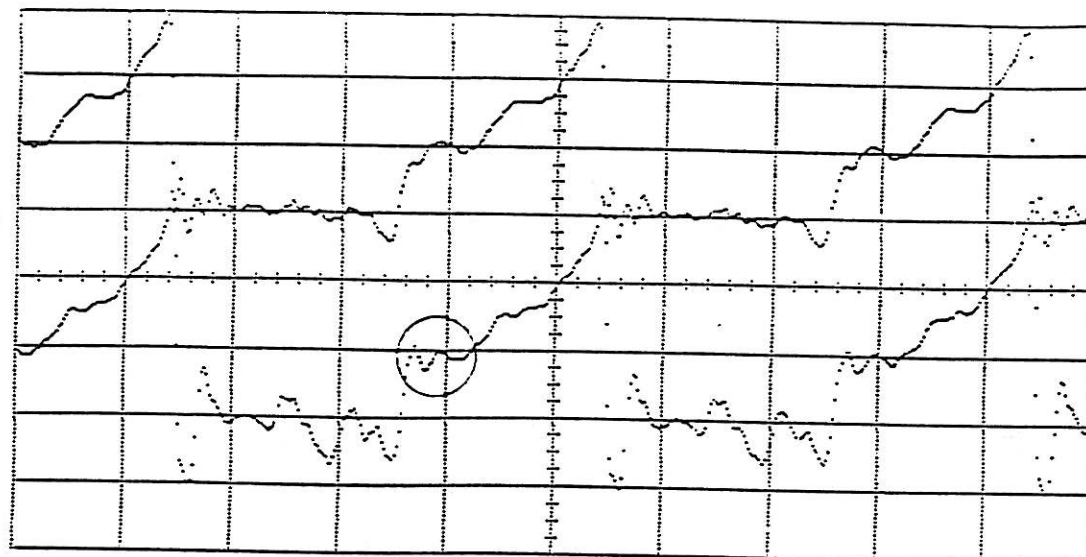


-20.000 ns 230.000 ns 480.000 ns

Ch. 1	=	100.0 mVolts/div	Offset	=	-100.0 mVolts
Ch. 2	=	100.0 mVolts/div	Offset	=	200.0 mVolts
Timebase	=	50.0 ns/div	Delay	=	-20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

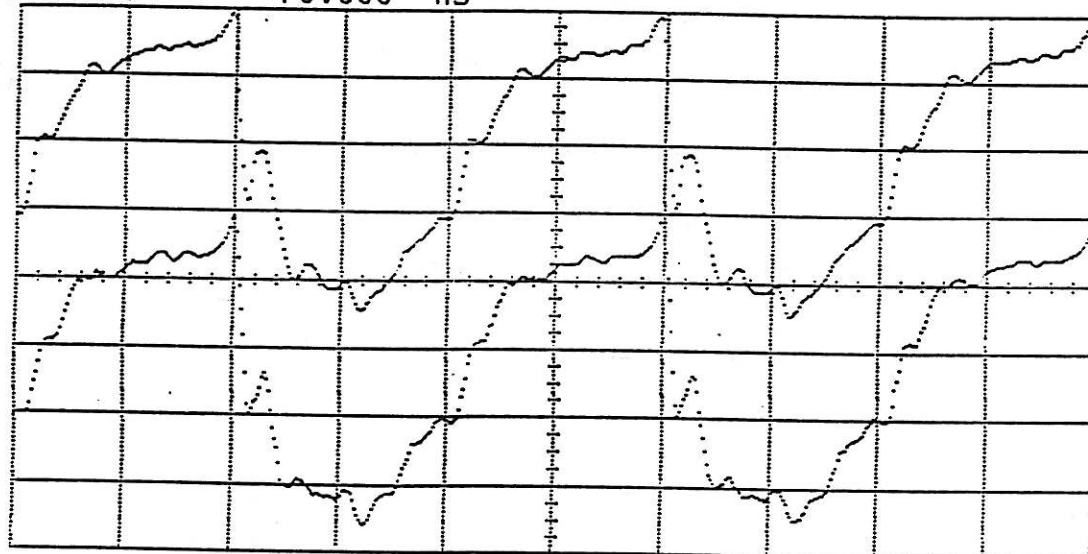
5 MHz
Config #2 (F
AMP
Type 2 loads



-20.000 ns 230.000 ns 480.000 ns

Ch. 1 = 100.0 mVolts/div Offset = -100.0 mVolts
Ch. 2 = 100.0 mVolts/div Offset = 200.0 mVolts
Timebase = 50.0 ns/div Delay = -20.000 ns

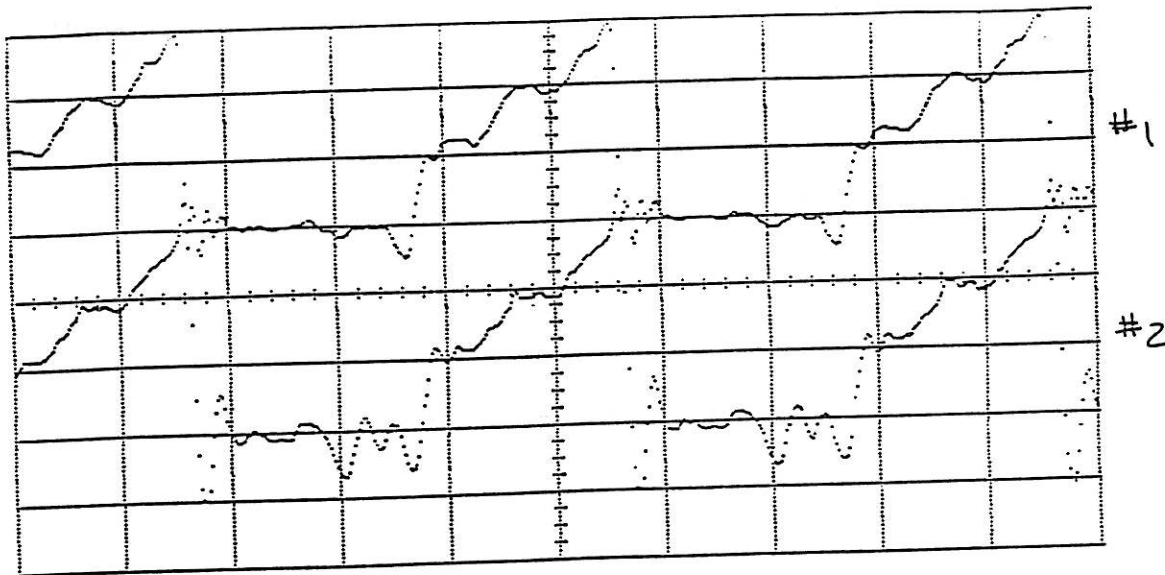
Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns



-20.000 ns 230.000 ns 480.000 ns

Ch. 1 = 100.0 mVolts/div Offset = -100.0 mVolts
Ch. 2 = 100.0 mVolts/div Offset = 200.0 mVolts
Timebase = 50.0 ns/div Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

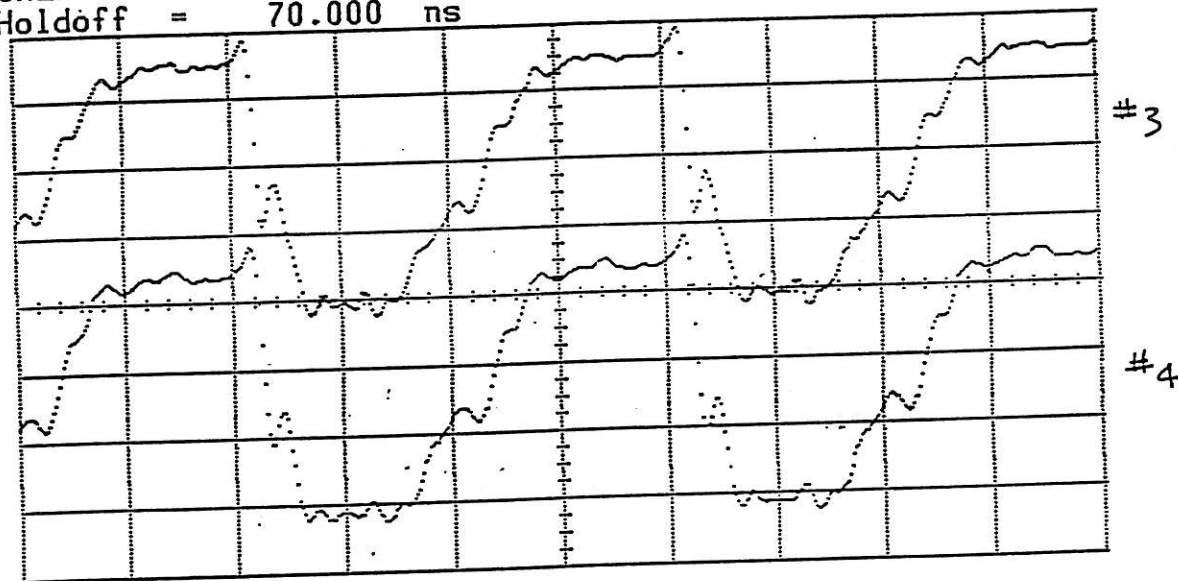


5MHz
Config # 2 (full)
STD
Type 2: loads

-20.000 ns 230.000 ns 480.000 ns

Ch. 1	= 100.0 mVolts/div	Offset	= -100.0 mVolts
Ch. 2	= 100.0 mVolts/div	Offset	= 200.0 mVolts
Timebase	= 50.0 ns/div	Delay	= -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

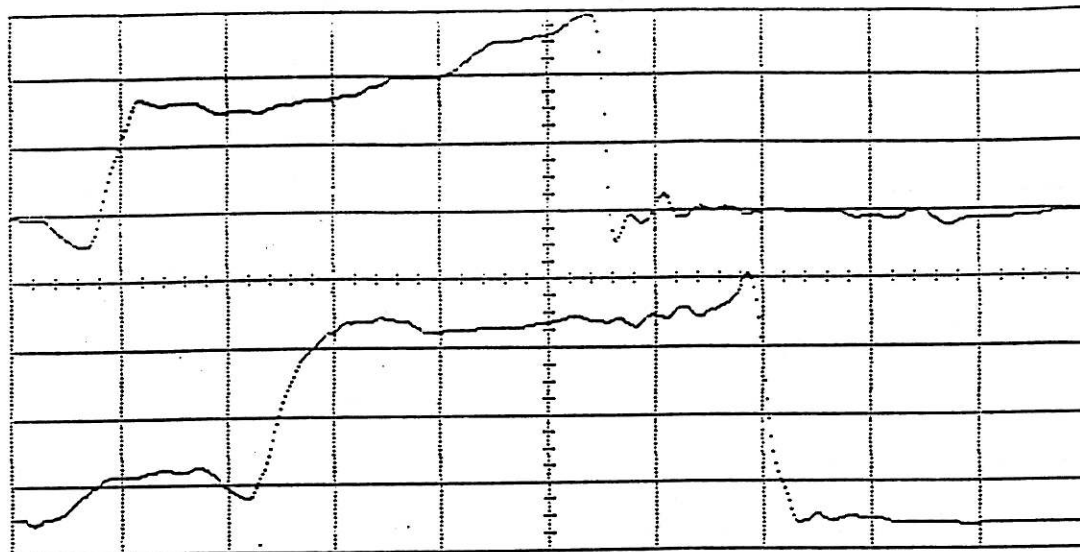


-20.000 ns 230.000 ns 480.000 ns

Ch. 1	= 100.0 mVolts/div	Offset	= -100.0 mVolts
Ch. 2	= 100.0 mVolts/div	Offset	= 200.0 mVolts
Timebase	= 50.0 ns/div	Delay	= -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 124.0 mVolts
Holdoff = 70.000 ns

150



5MHz
Config #2, ST
Two devices

#1

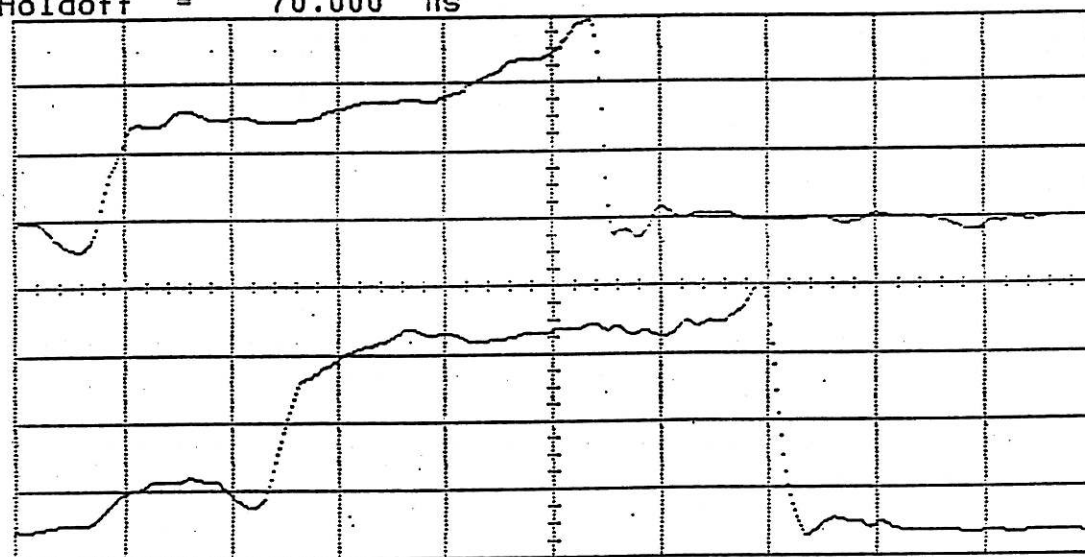
#7

-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 20.0 ns/div

Offset = -100.0 mVolts
Offset = 300.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 100.0 mVolts
Holdoff = 70.000 ns



5MHz
Config #2, AMP
Two devices only

-20.000 ns 80.000 ns 180.000 ns

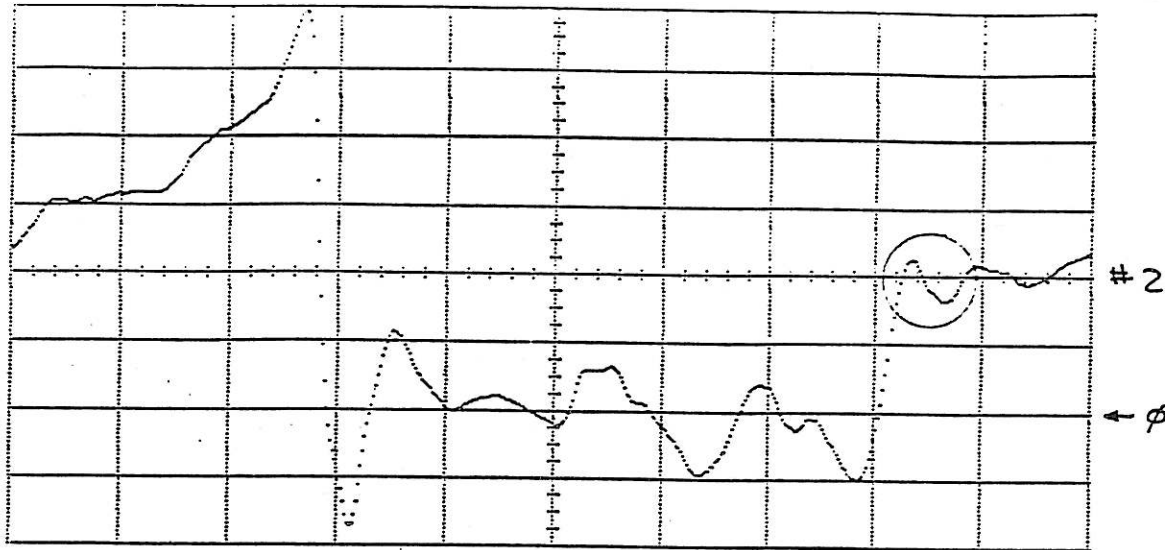
Ch. 1 = 100.0 mVolts/div
Ch. 2 = 100.0 mVolts/div
Timebase = 20.0 ns/div

Offset = -100.0 mVolts
Offset = 300.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 100.0 mVolts
Holdoff = 70.000 ns

151

5m-2
Amp
242/297 Terminz
Type 2

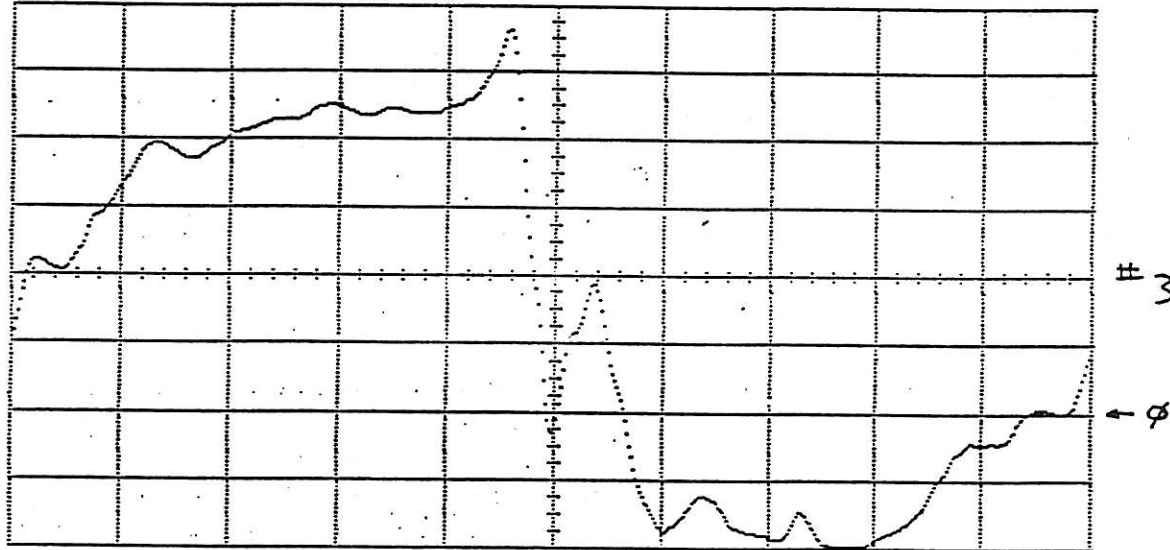


-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div
Timebase = 20.0 ns/div

Offset = 100.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns



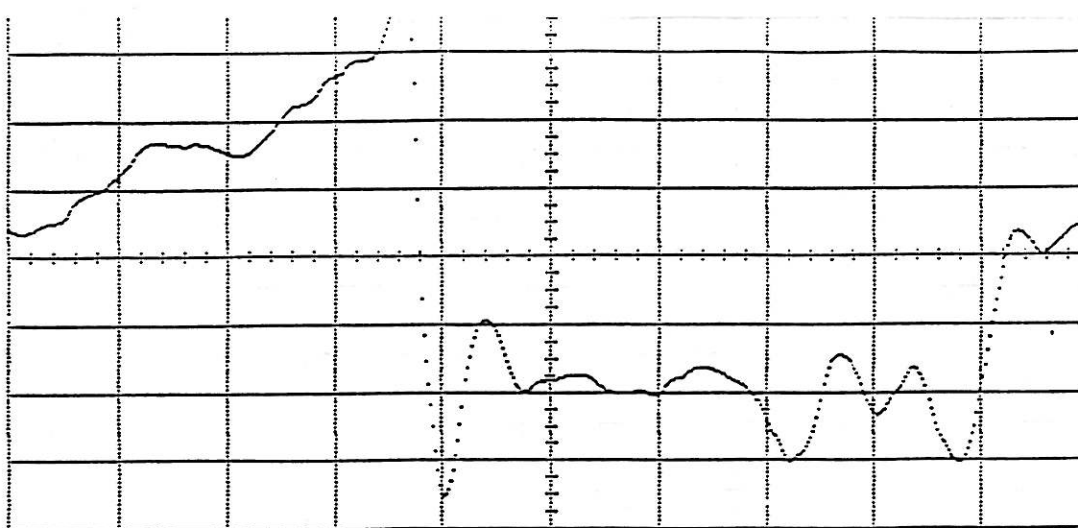
-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div
Timebase = 20.0 ns/div

Offset = 100.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns

5MHz
STD
242/297 Terminator
Type 2



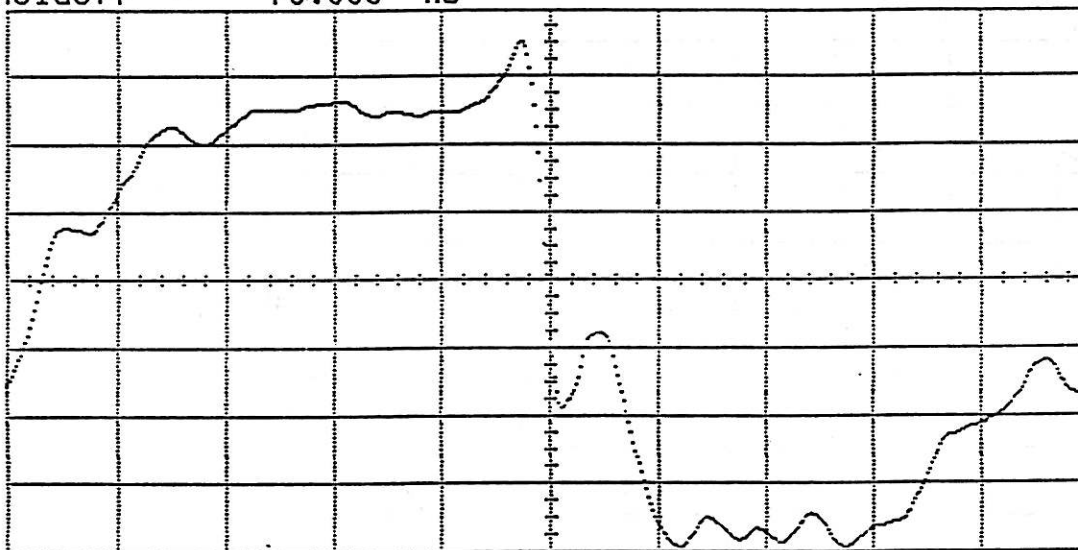
#2

← ϕ

-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div Offset = 100.0 mVolts
Timebase = 20.0 ns/div Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns



#3

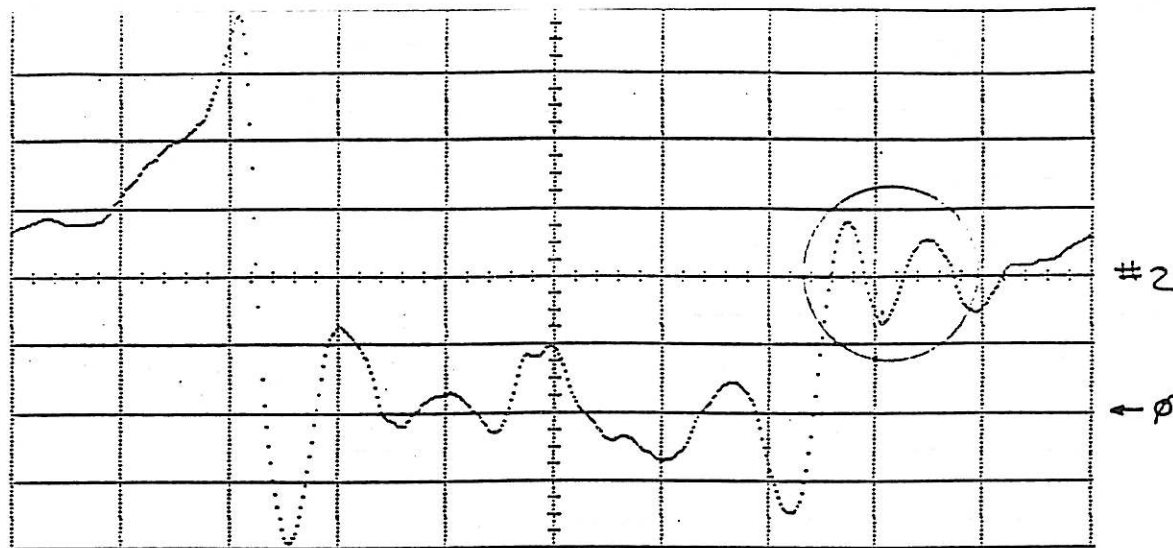
← ϕ

-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div Offset = 100.0 mVolts
Timebase = 20.0 ns/div Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns

5MHz
AMP
242/277 Termi
Type 1

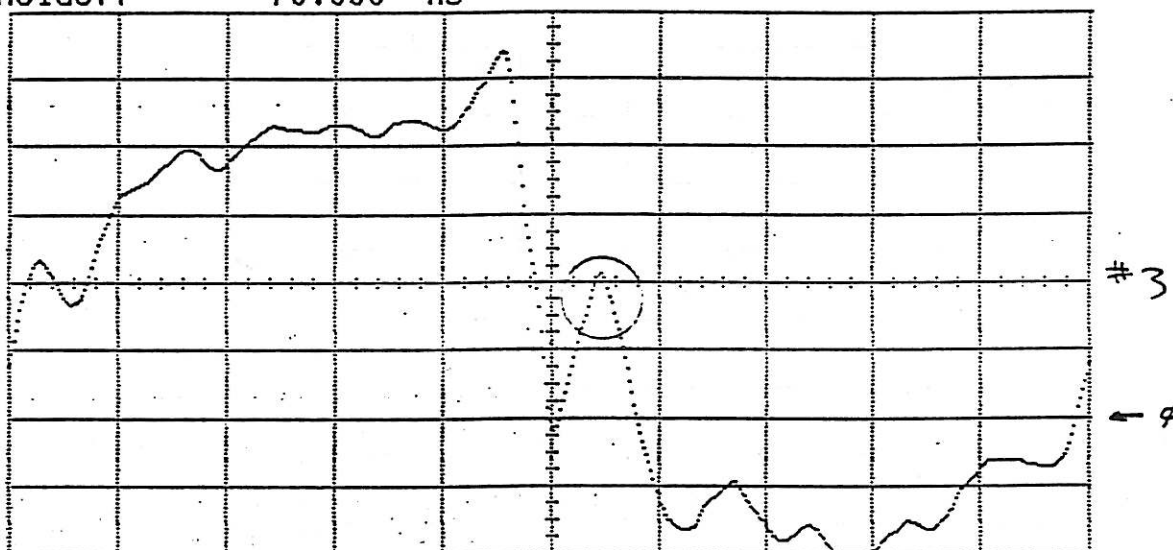


-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div
Timebase = 20.0 ns/div

Offset = 100.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns



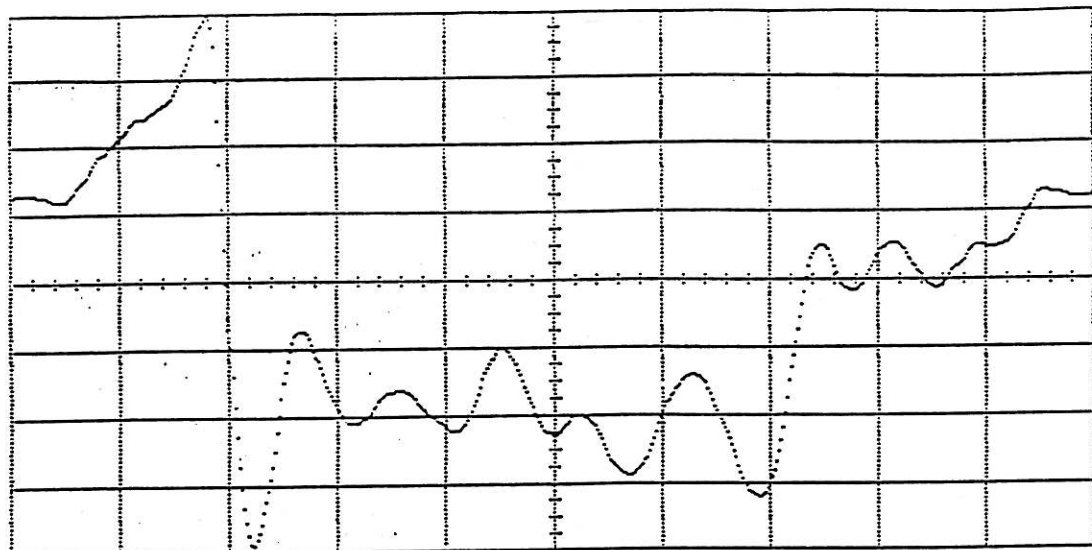
-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div
Timebase = 20.0 ns/div

Offset = 100.0 mVolts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 149.0 mVolts
Holdoff = 70.000 ns

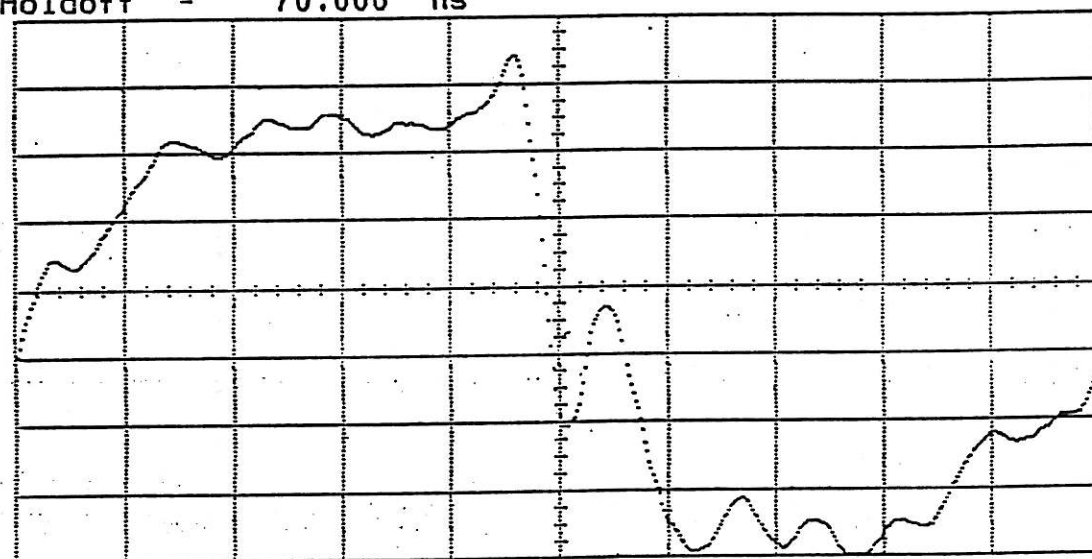
5MHz
 STD
 242/297 termin
 Type 1



-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div Offset = 100.0 mVolts
 Timebase = 20.0 ns/div Delay = -20.000 ns

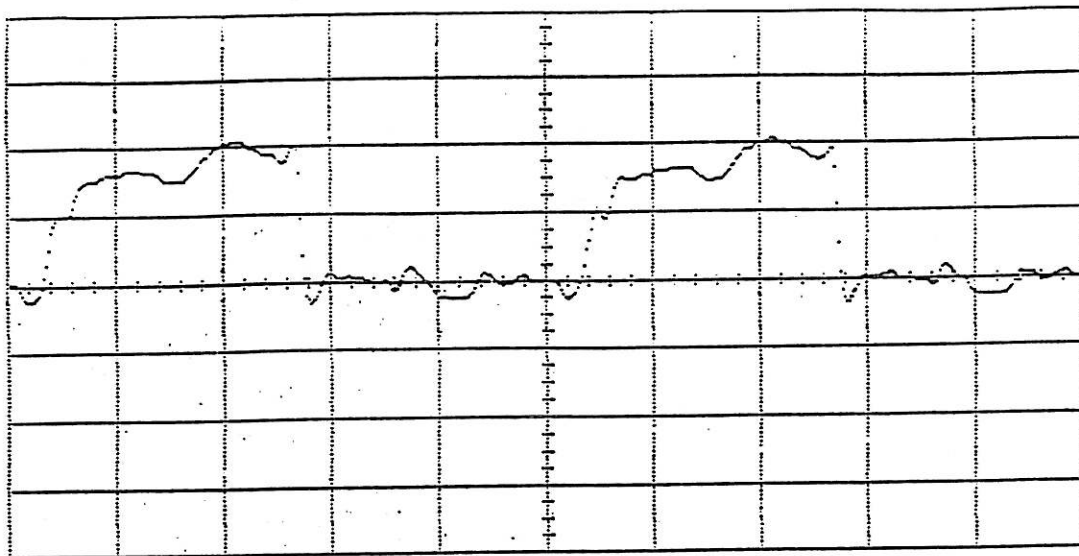
Trigger mode : Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = 196.0 mVolts
 Holdoff = 70.000 ns



-20.000 ns 80.000 ns 180.000 ns

Ch. 1 = 50.00 mVolts/div Offset = 100.0 mVolts
 Timebase = 20.0 ns/div Delay = -20.000 ns

Trigger mode : Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = 149.0 mVolts
 Holdoff = 70.000 ns



STD, w/dic

1002 +

2.6'

#2

Type 1/2

-20.000 ns

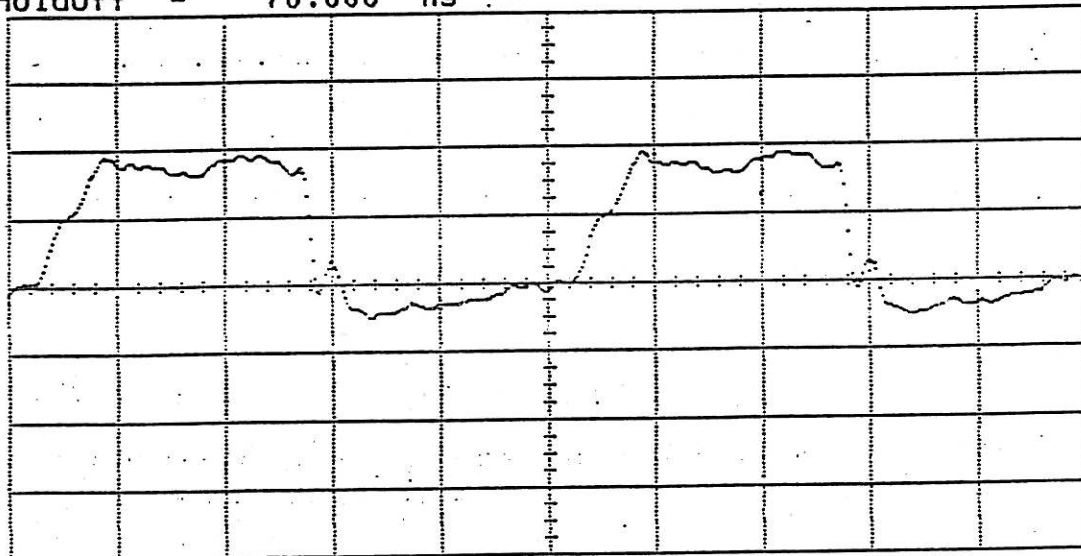
230.000 ns

480.000 ns

Ch. 1 = 200.0 mVolts/div
Timebase = 50.0 ns/div

Offset = 0.000 Volts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 114.0 mVolts
Holdoff = 70.000 ns



#3

-20.000 ns

230.000 ns

480.000 ns

Ch. 1 = 200.0 mVolts/div
Timebase = 50.0 ns/div

Offset = 0.000 Volts
Delay = -20.000 ns

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 114.0 mVolts
Holdoff = 70.000 ns

156