X3T9.2/88-147

EMULEX

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To: X3T9.2 Committee (SCSI)

Date: November 4, 1988

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Fremont, CA 94538

Subject: SCSI Bus Transmission Line Analysis

ABSTRACT:

As SCSI bus performance has increased past 4 MBytes/sec, the SCSI standard is gaining more widespread market acceptance and is becoming the largest installed base of peripheral interfaces in the computer industry. Although the original SCSI electrical specification was adequate for early low performance systems, higher transfer rates mandate tighter restrictions on system design.

Included here are the results from SPICE simulations and bench verification of several SCSI bus configurations. The effects of transmission line impedance, termination, and stub clustering were studied. The results show that the signal integrity on the bus can be marginal (perhaps even unusable) with long unmatched cables and clustering of several stubs at points on the bus. Furthermore, trying to push the current single-ended bus to higher speeds ("fast SCSI") is on shaky ground. The SCSI-2 standard should include tighter restrictions on cable impedance, termination, and bus topology.

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SPICE CIRCUIT:

The basic SCSI driver model is an NMOS open drain driver with a 10 pF capacitive load. Although very simplistic, this model does compare reasonably well with laboratory observations of actual drivers. The model is accurate enough to produce relative data that can be used to draw some general conclusions.

The configuration used for each run is indicated on each figure. Refer to the following legend:

	SPICE element	Lab equivalent
──	100 or 105 ohm cable	normal flat cable
═══	70 ohm cable	shielded round or flat cable
x	10 pF load	inactive SCSI device
I	10 pF load	initiator
T	10 pF load + NMOS driver	target

Where present, scope pictures are of the SCSI REQ/ signal which is driven by the target device. Since a low capacitance scope probe was not available, the waveforms are somewhat more rounded than in the corresponding SPICE waveforms.

OVERVIEW OF RESULTS:

For all plots and photographs, the scale is 20 nS/division horizontally and 1 V/division vertically.

Figures 1-1 through 1-5 illustrate the ideal case, with termination matched to the cable impedance and no stubs or clustering. The waveforms look good in this perfect (alas unrealistic!) transmission medium. Scope pictures for Figures 1-3 through 1-5 were obtained by changing the termination resistor network to 175/240 ohms. This corresponds to a Thevenin equivalent termination of approximately 100 ohms (to match the cable) with a 2.9 V voltage source (which limits the current requirements of the driver to 48 mA at Vol=0.5V). This might be a possible solution to the problem, if tighter restrictions can be made on cable impedance and the termination voltage.

Figures 2-1 through 2-5 illustrate the typical case, which combines 132 ohm termination mismatched with 100 ohm and/or 70 ohm cables. Since impedances are not matched, the signal is reflected back at each point of impedance change. The reflections rob the signal of energy and distort its shape.

Figures 3-1 through 3-14 investigate the effects of adding stubs and stub clustering. Most examples use 132 ohm termination and 100 ohm cables; the effects are worse with lower impedance cables. The stubs present additional impedance mismatches on the bus which further degrade the signal.

Figures 4-1 through 4-6 attempt to send fast synchronous assertion and negation pulses across a 100 ohm cable terminated with 132 ohms.

PRELIMINARY RECOMMENDATIONS:

These results demonstrate that unmatched cables, clustering, and non-ideal bus termination can severely degrade signal integrity on the SCSI bus. Some preliminary recommendations are listed below. These should be substantiated with further work (see CONCLUSIONS).

1. An absolute minimum cable impedance for all cables (shielded and unshielded) should be specified. The impedance should be 90 ohms or greater, with greater than 100 ohms recommended.

2. An absolute maximum load capacitance per node should be specified. The total capacitance off the mainline connection should be 20 pF or less.

3. Implementors note: Stub clustering should be avoided. Stubs should be spaced at least .3 meters apart.

4. For fast synchronous transfer mode, the cable impedance should be 100 to 132 ohms, with an impedance as close as possible to the termination impedance recommended.

5. Implementors note: Single-ended mode is not recommended for fast SCSI.

CONCLUSION:

The results point out some important considerations but suggest a lot more work could be spent. The committee should very carefully consider tasking someone with a more complete analysis that includes correlating simulation results to observed conditions on practical configurations.

In developing the specification for the electrical bus the following should be included and their combined effects modeled or analyzed:

Transmission line impedance and tolerance

Practical stub configurations and stub clustering effects

Bus topology permitted, perhaps computed based on the total length, the number, length, and clustering of stubs and desired operations modes (sync/async etc.)

Termination resistors and equivalent Thevenin voltage and tolerance

Receiver implementation, sensitivity, accuracy and hysteresis both in absolute and percentage of termination voltage

Driver implementation, rise time, and impedance control, with consideration of differential and/or active three state drivers

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Fig. 1-1 Ideal (100Ω, no stub capacitance)

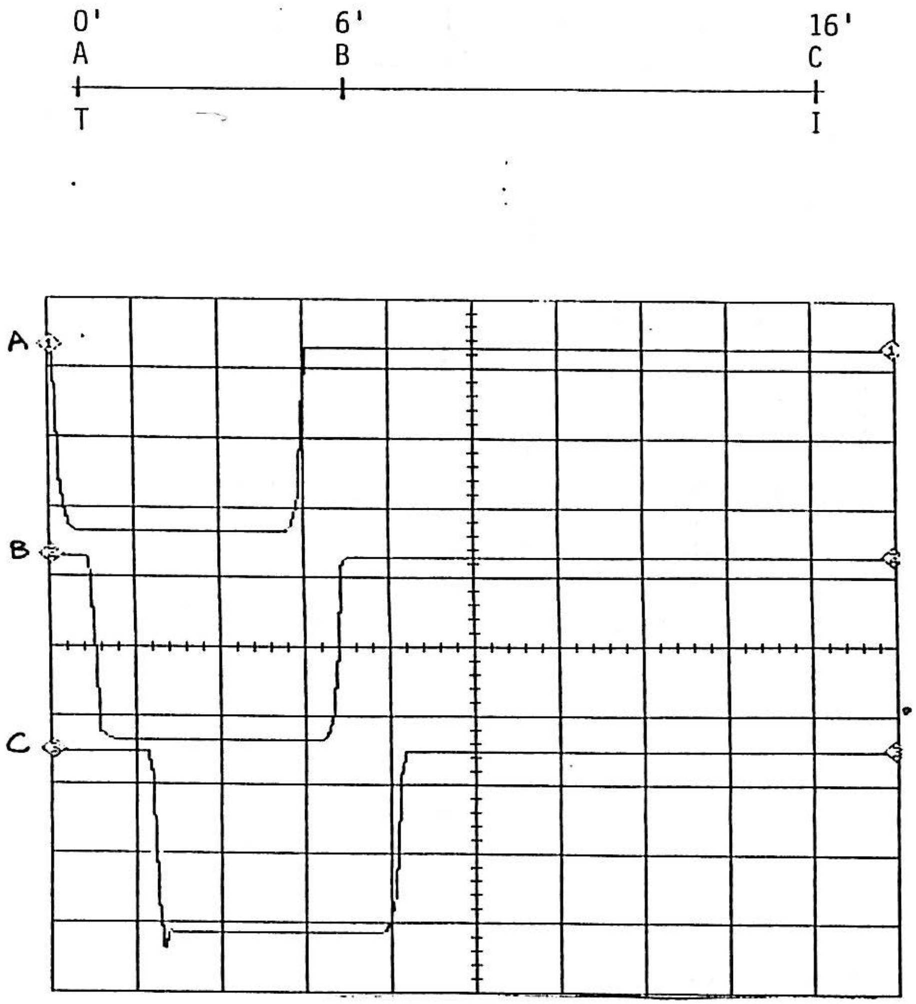


Fig. 1-2 Ideal (132Ω, no stub capacitance)

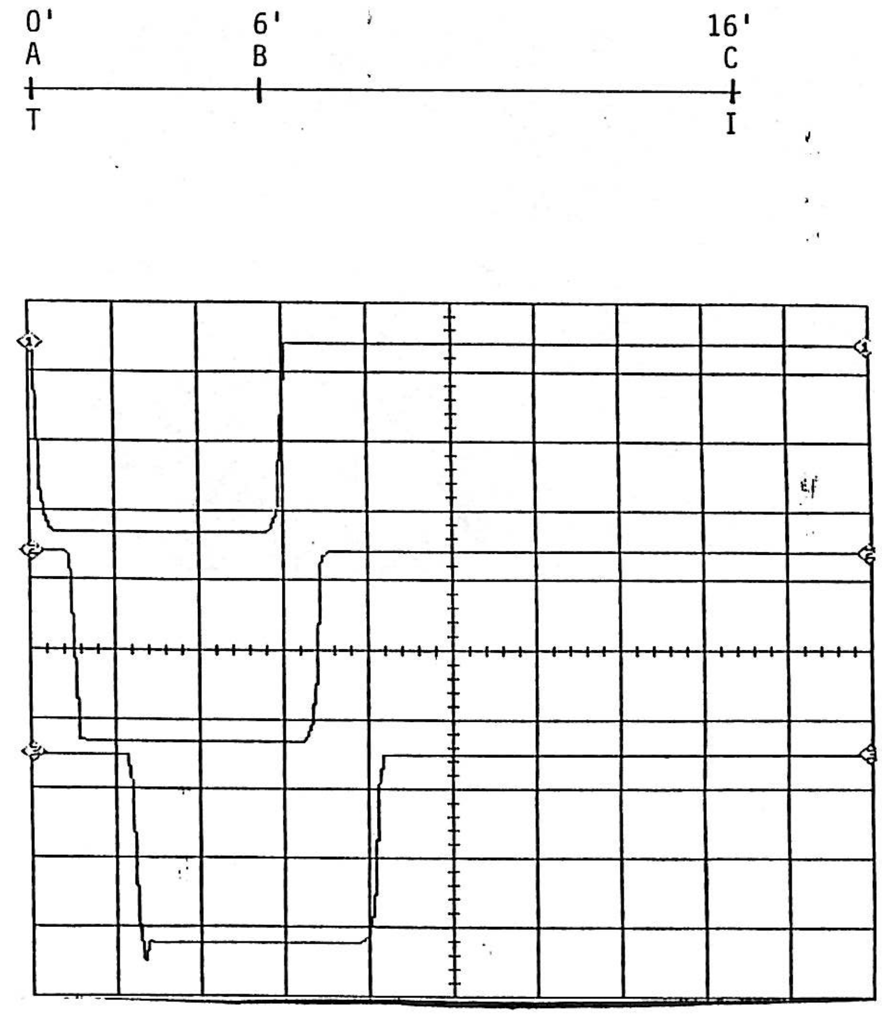
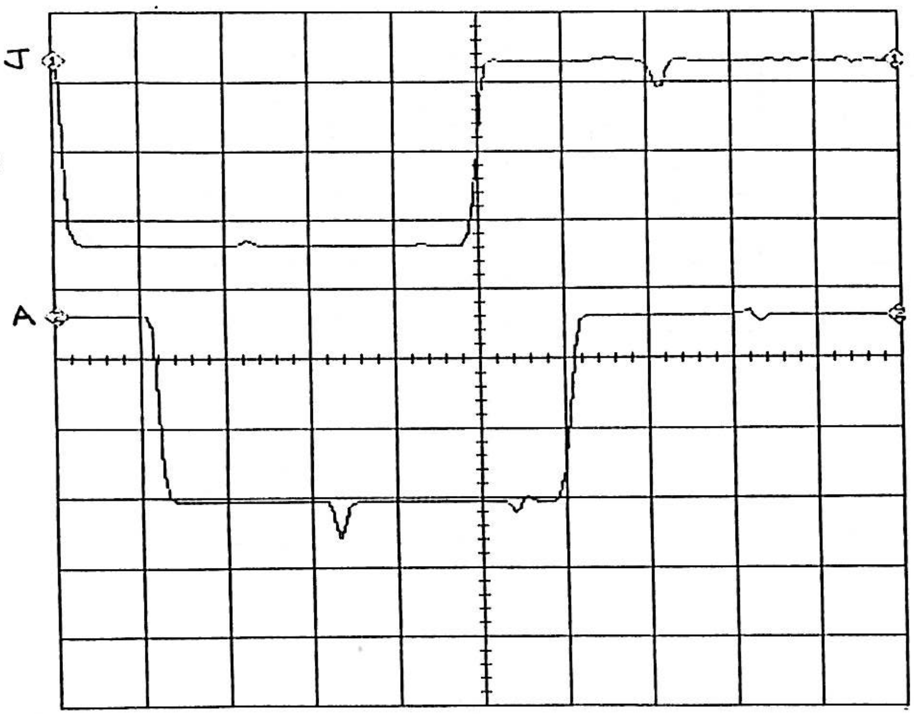


Fig. 1-3 100Ω Termination



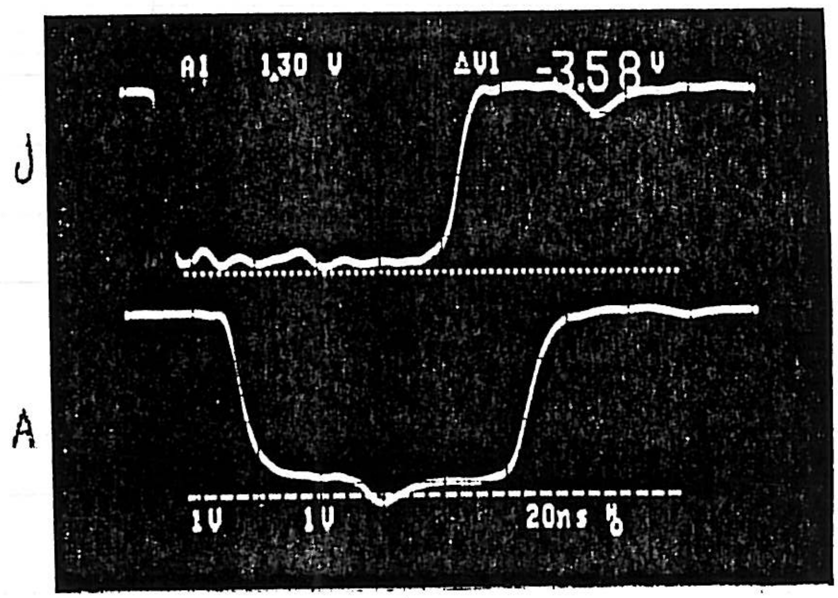
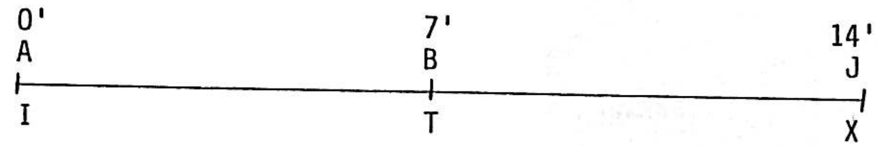
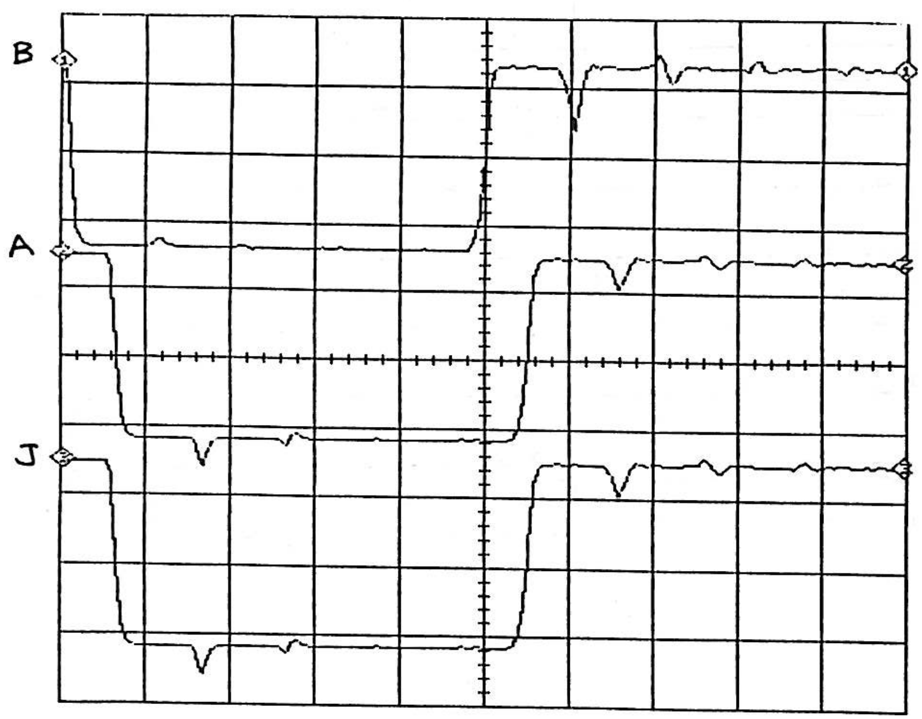
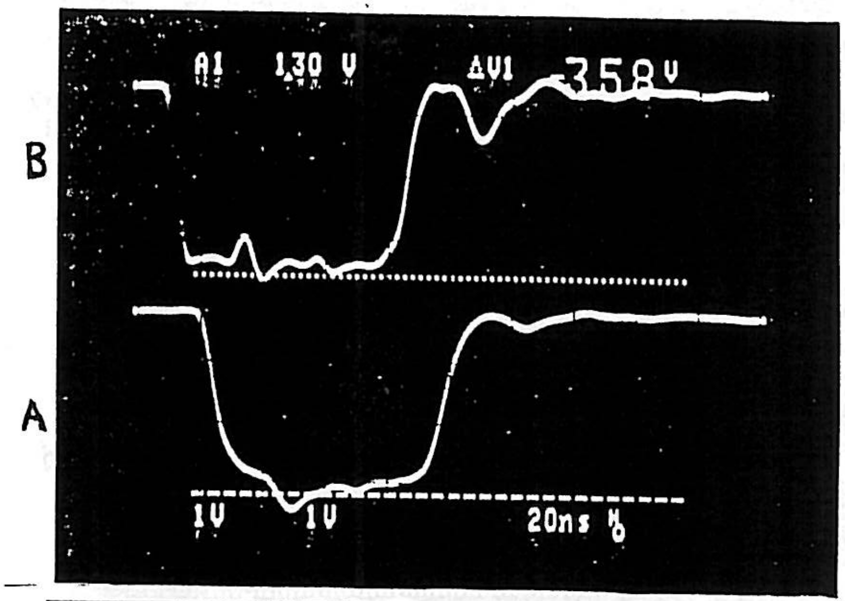


Fig. 1-4 100Ω Term







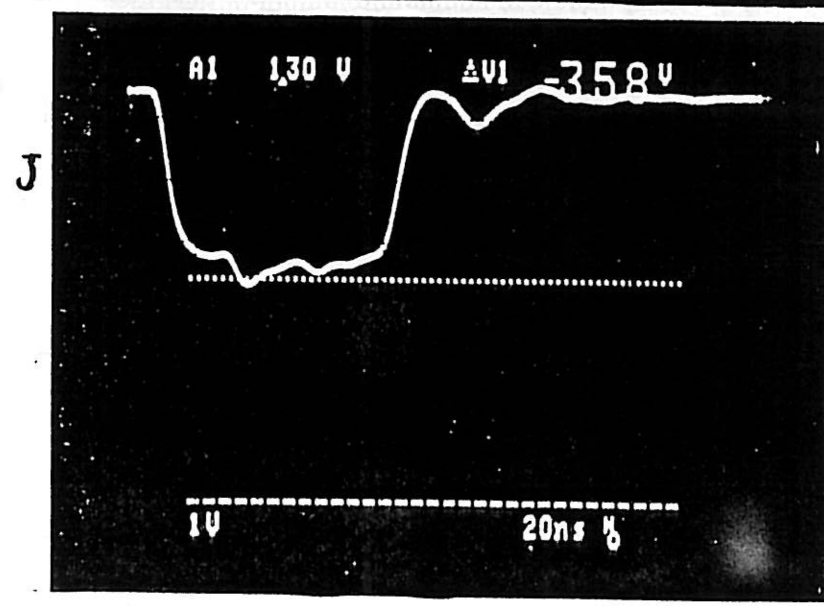
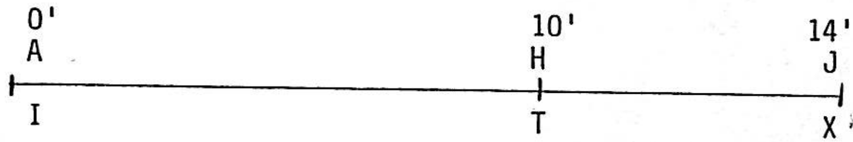
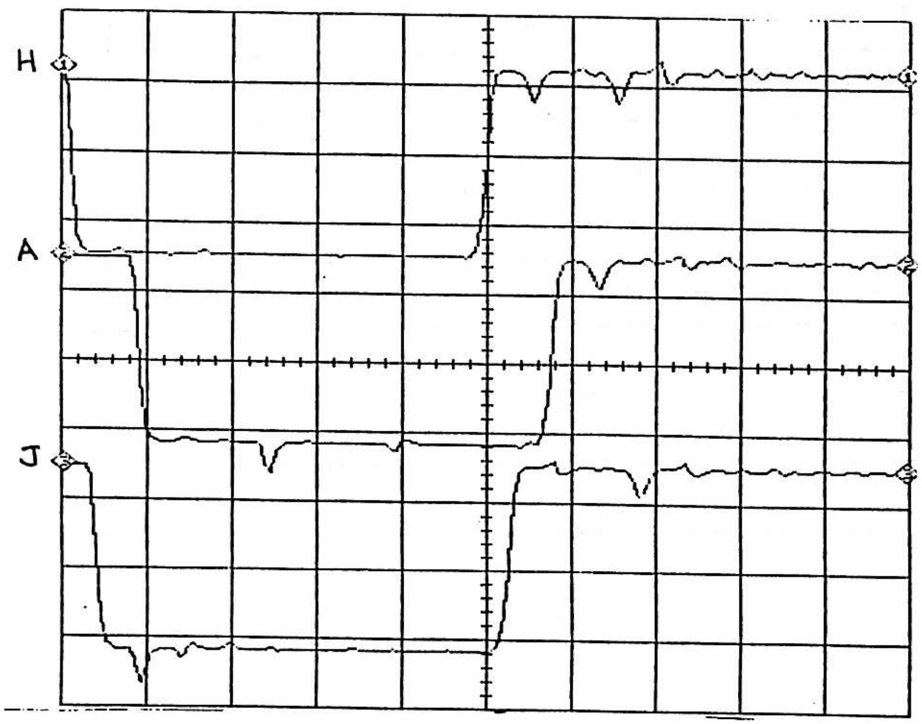
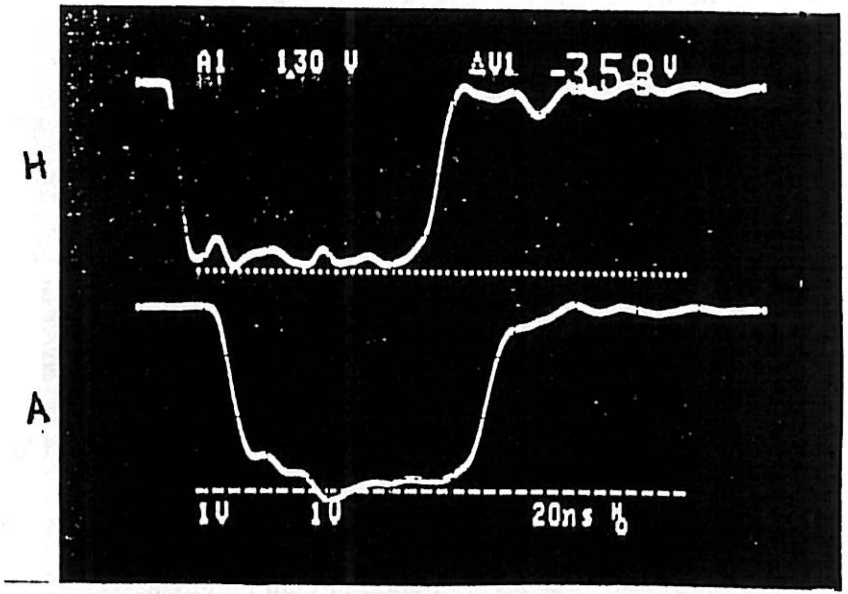


Fig. 1-5 100 Ω Term







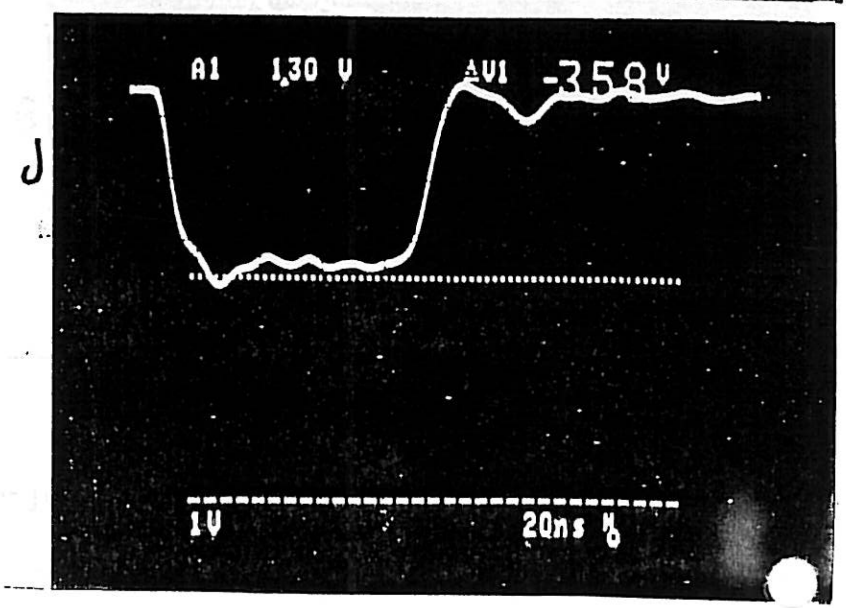
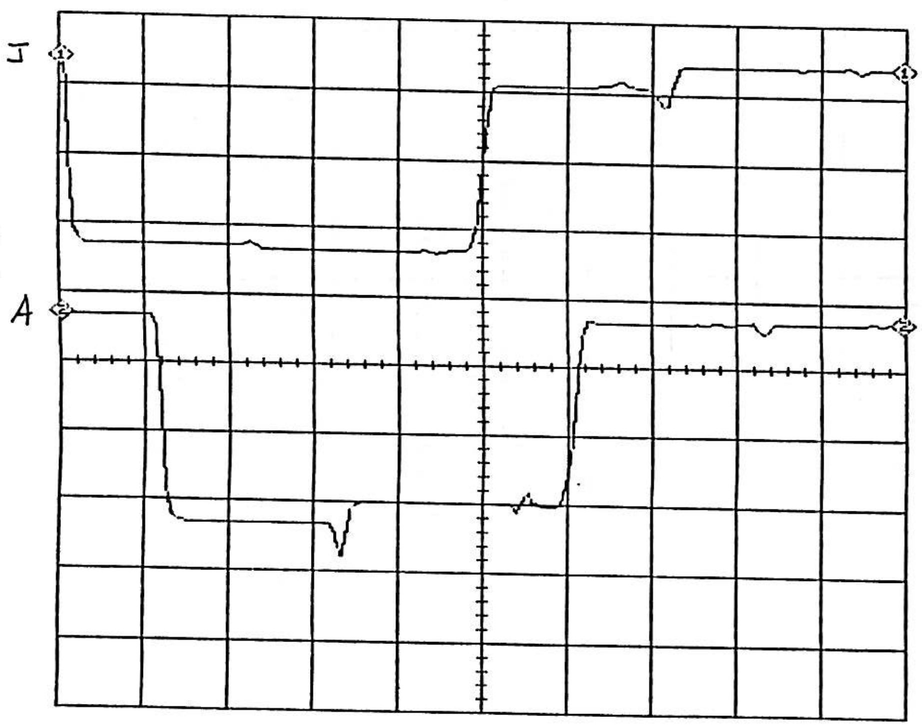


Fig. 2-1



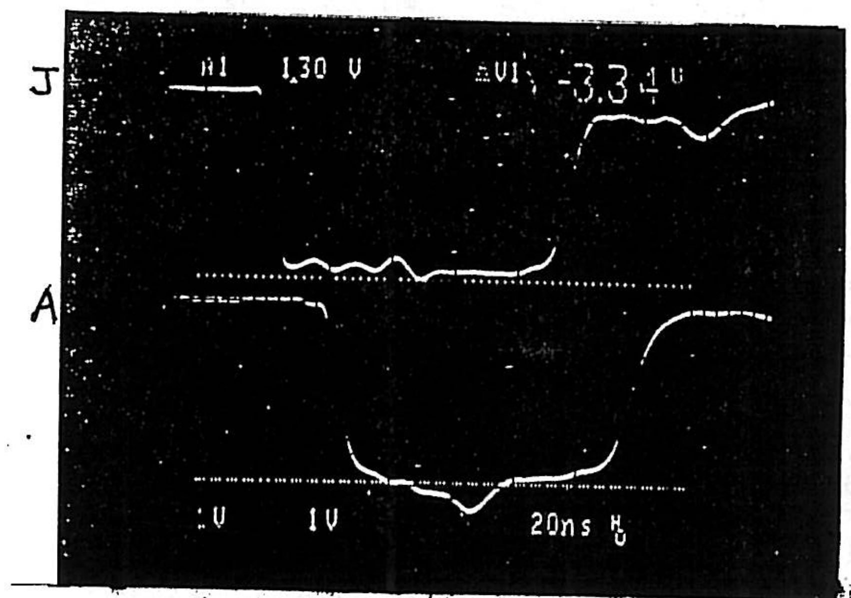


Fig. 2-2

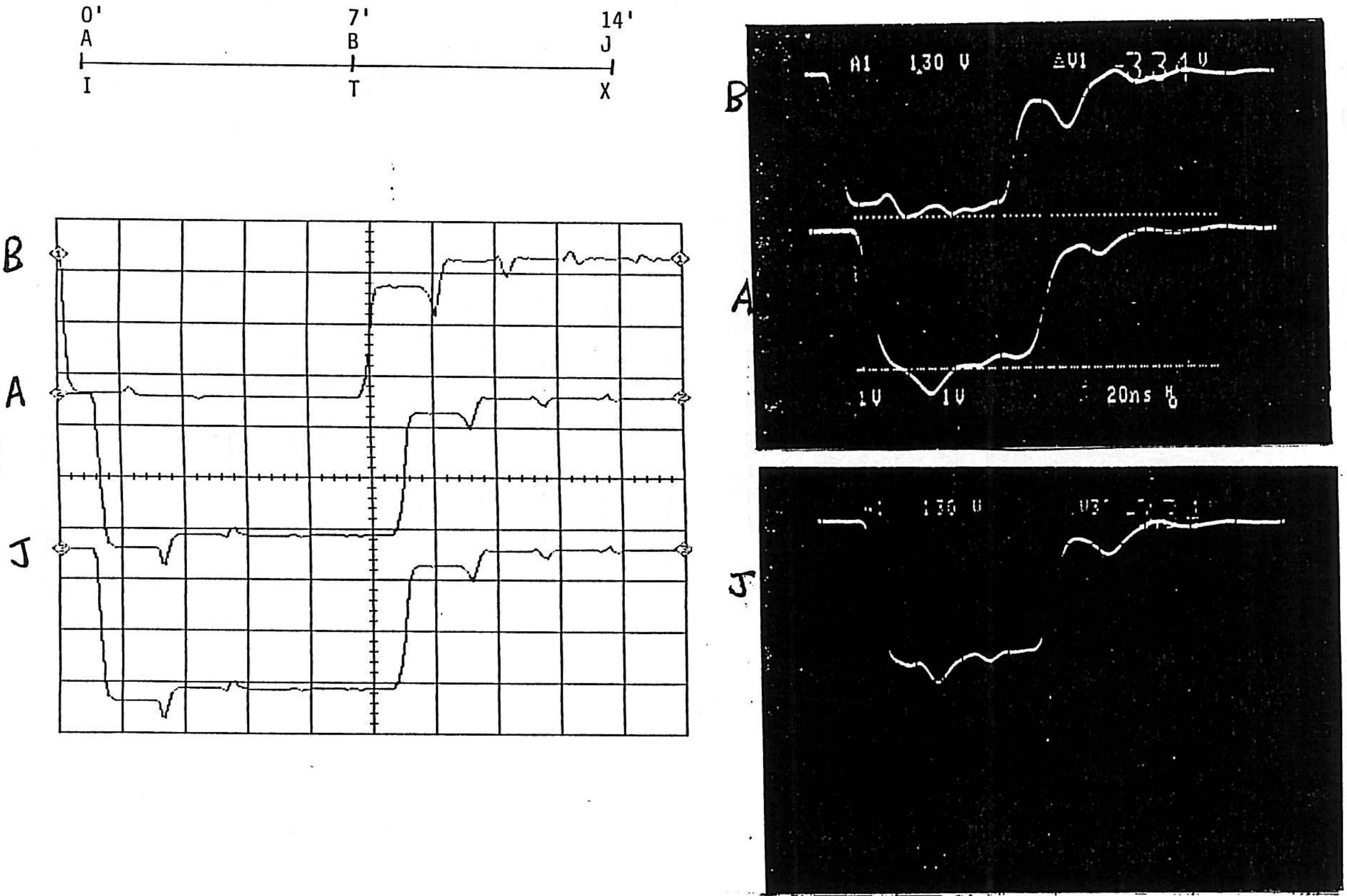
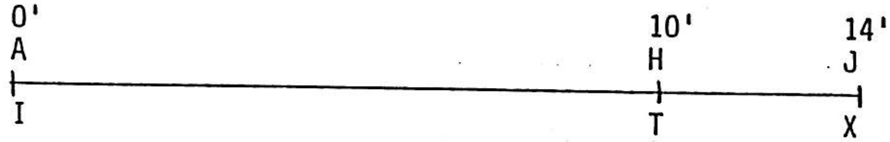
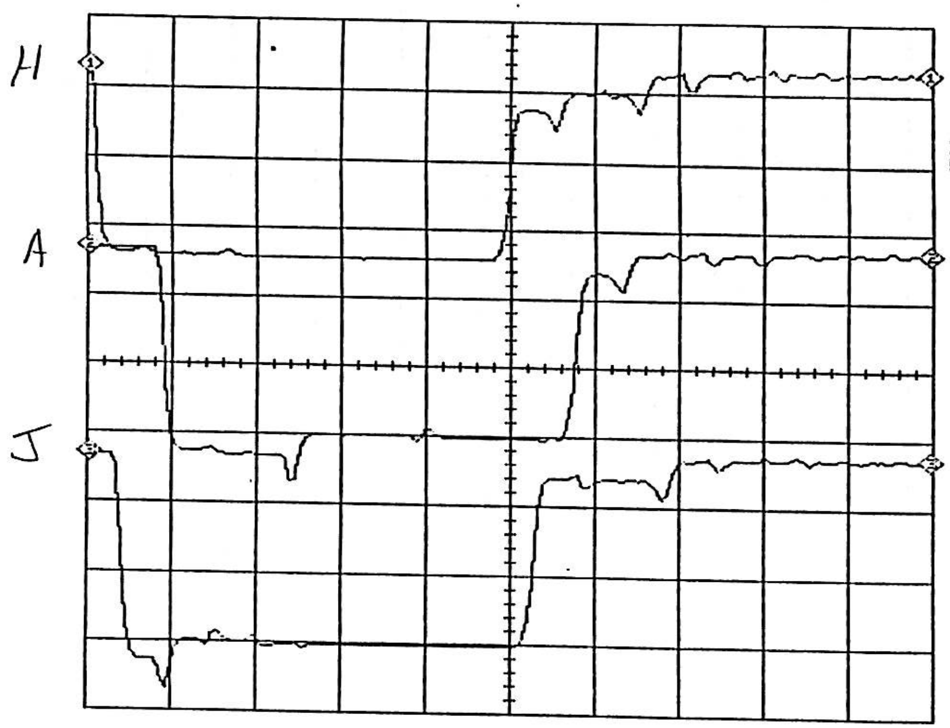
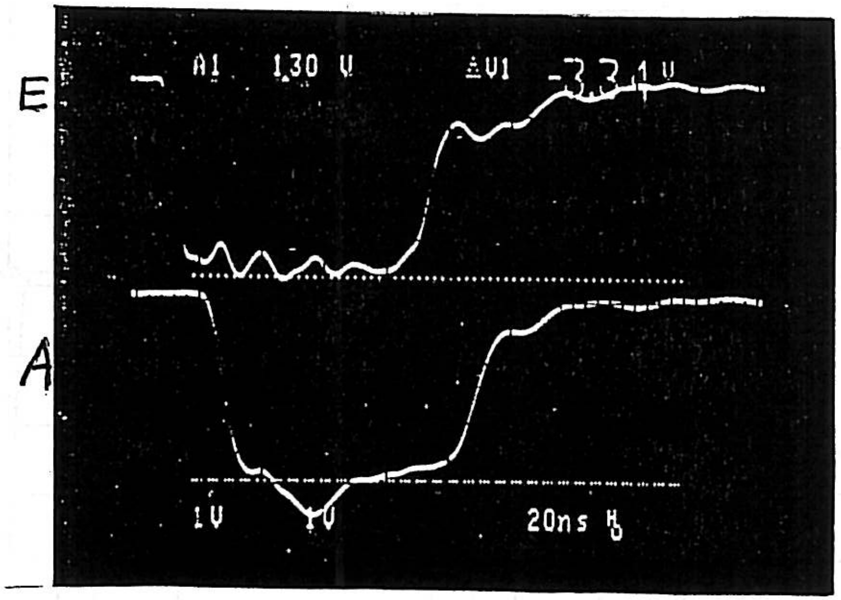


Fig. 2-3


0'
A
I
10'
H
T
14'
J
X


H
A
J


E
A
A1 1.30 V
ΔV1 -3.31 V
1V
1V
20ns

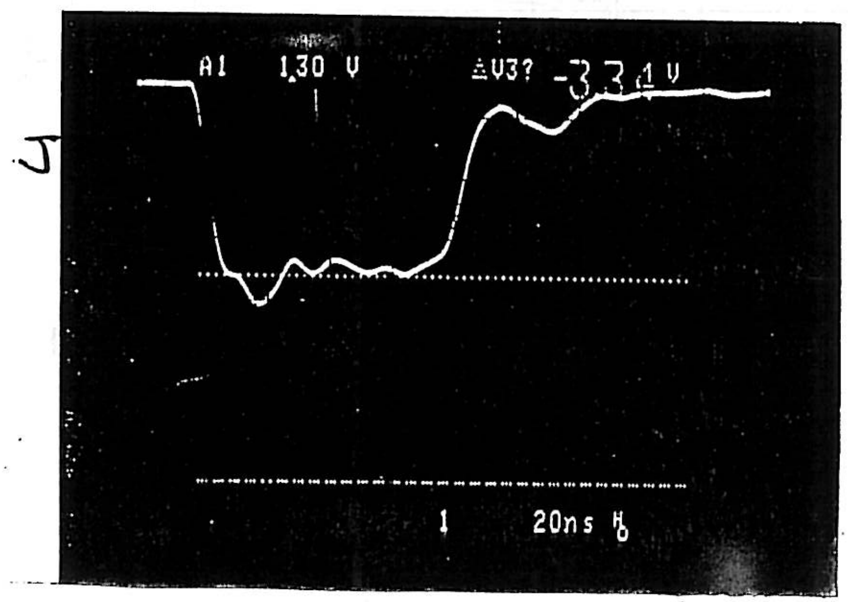

J
A1 1.30 V
ΔV3? -3.31 V
1
20ns

Fig. 2-4

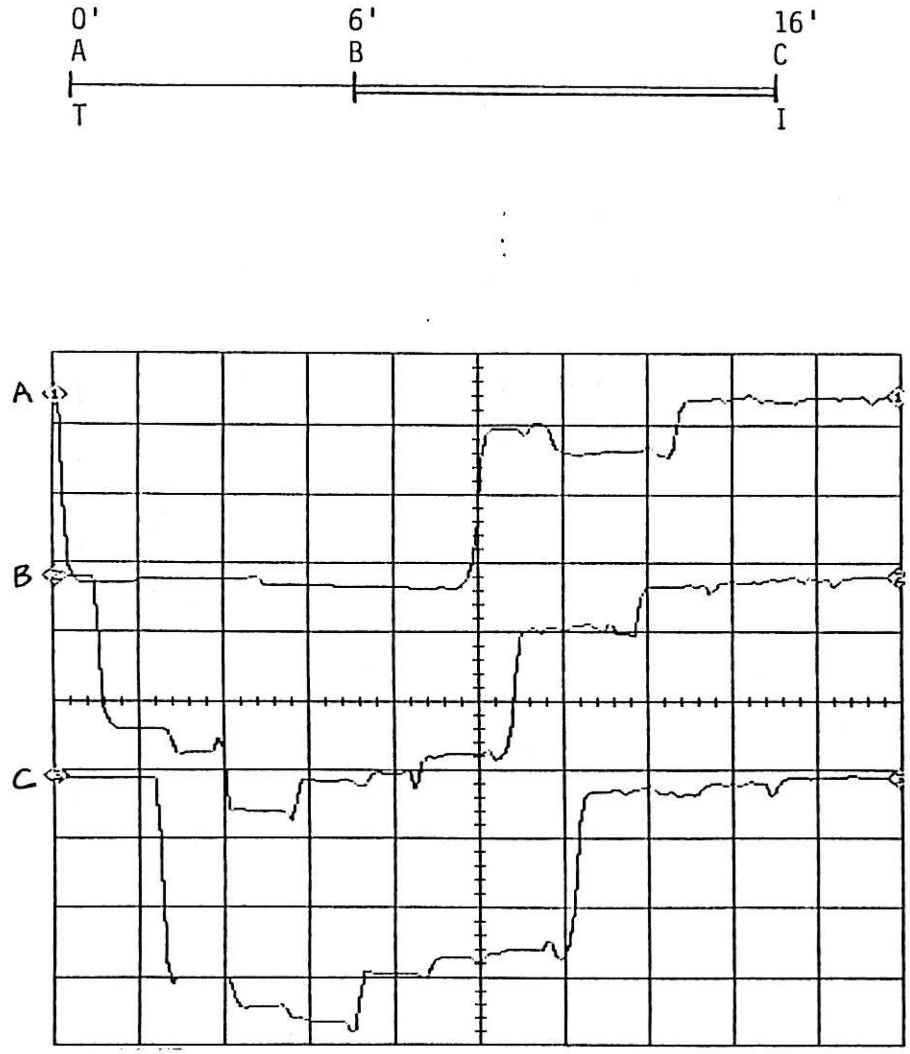


Fig. 2-5

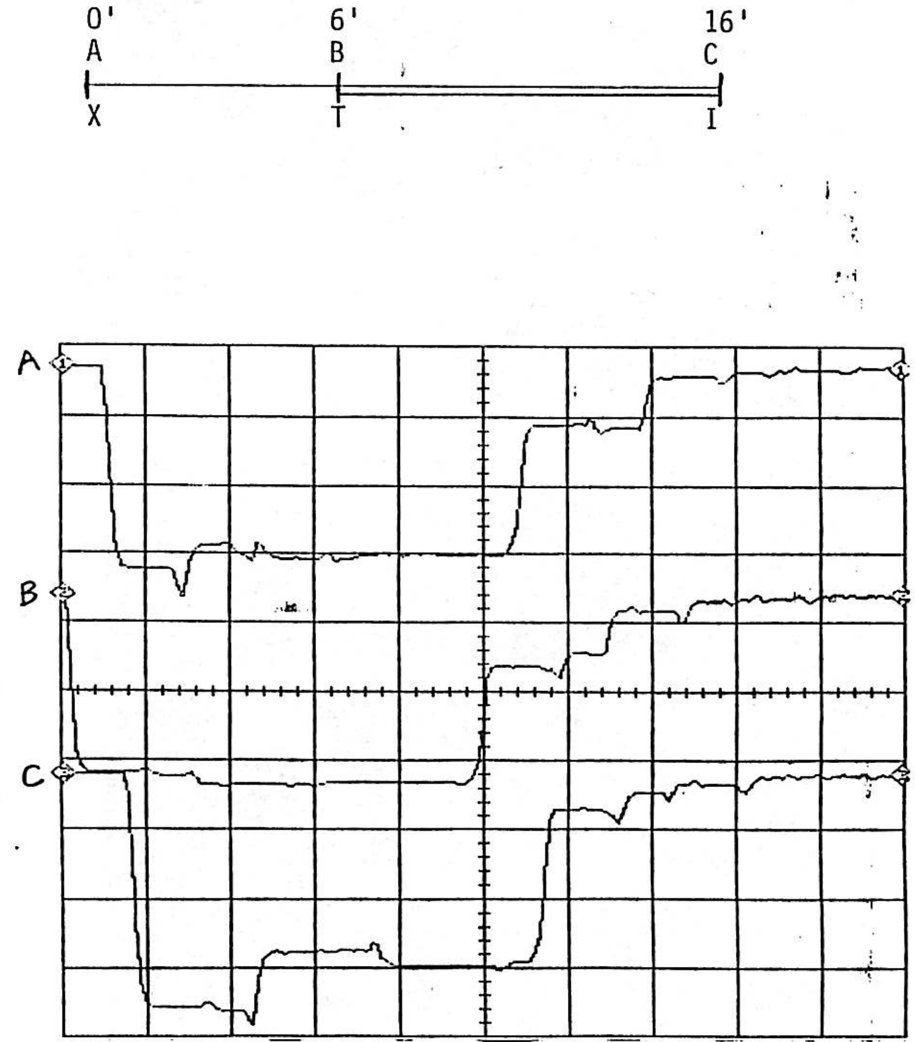
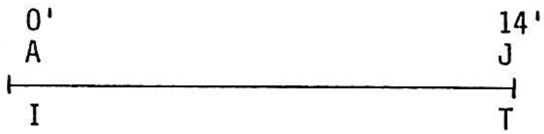
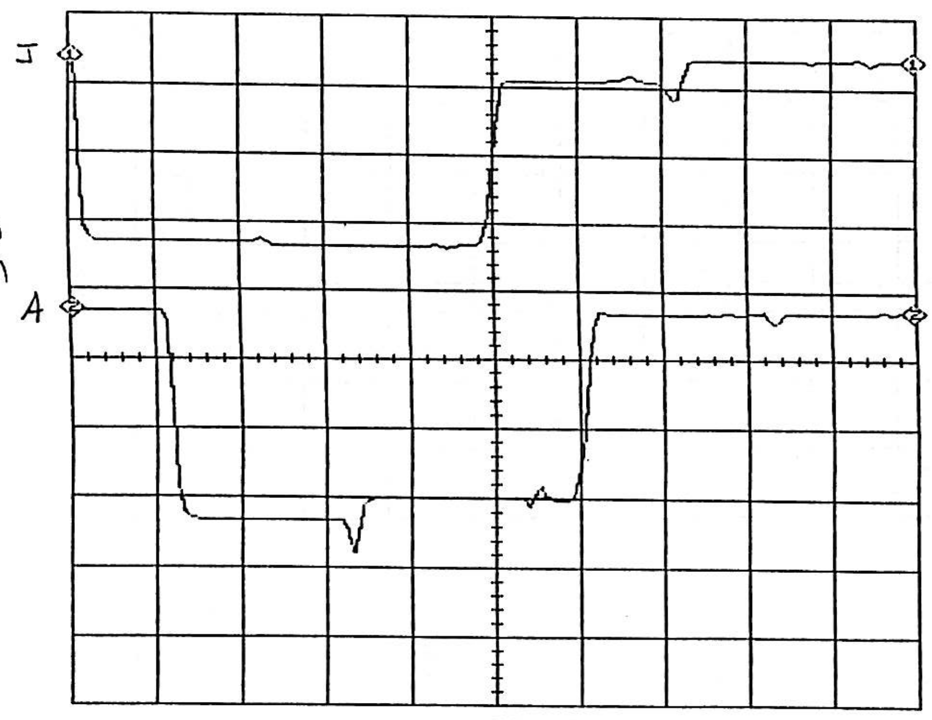


Fig. 3-1



35



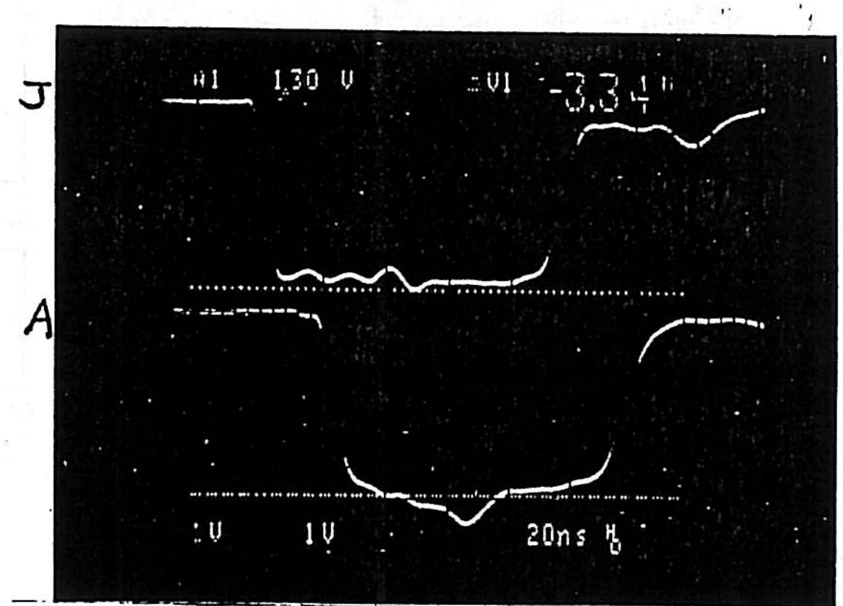
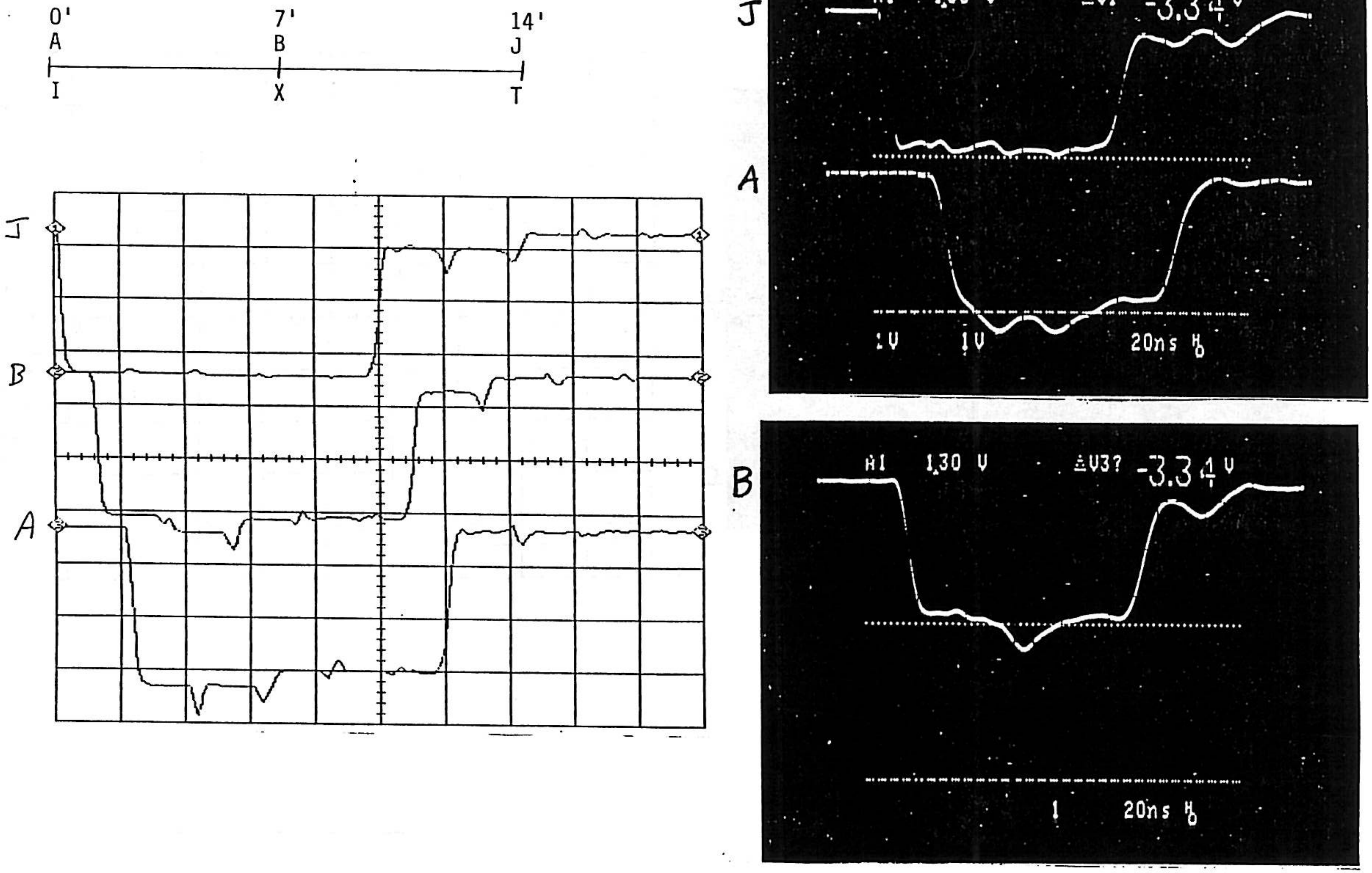
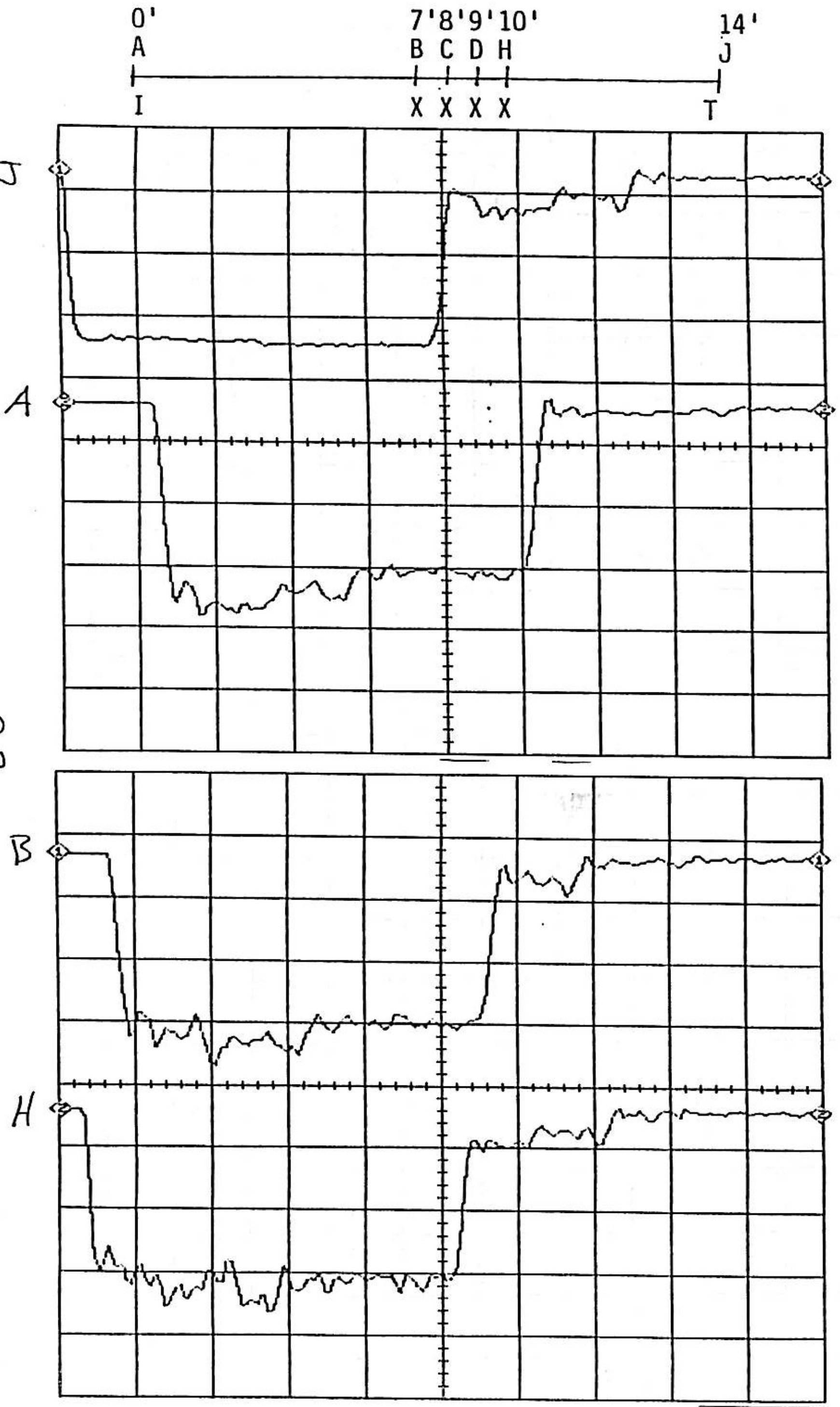


Fig. 3-2



36

Fig. 3-3



0'
A
7'8'9'10'
B C D H
14'
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X X X X
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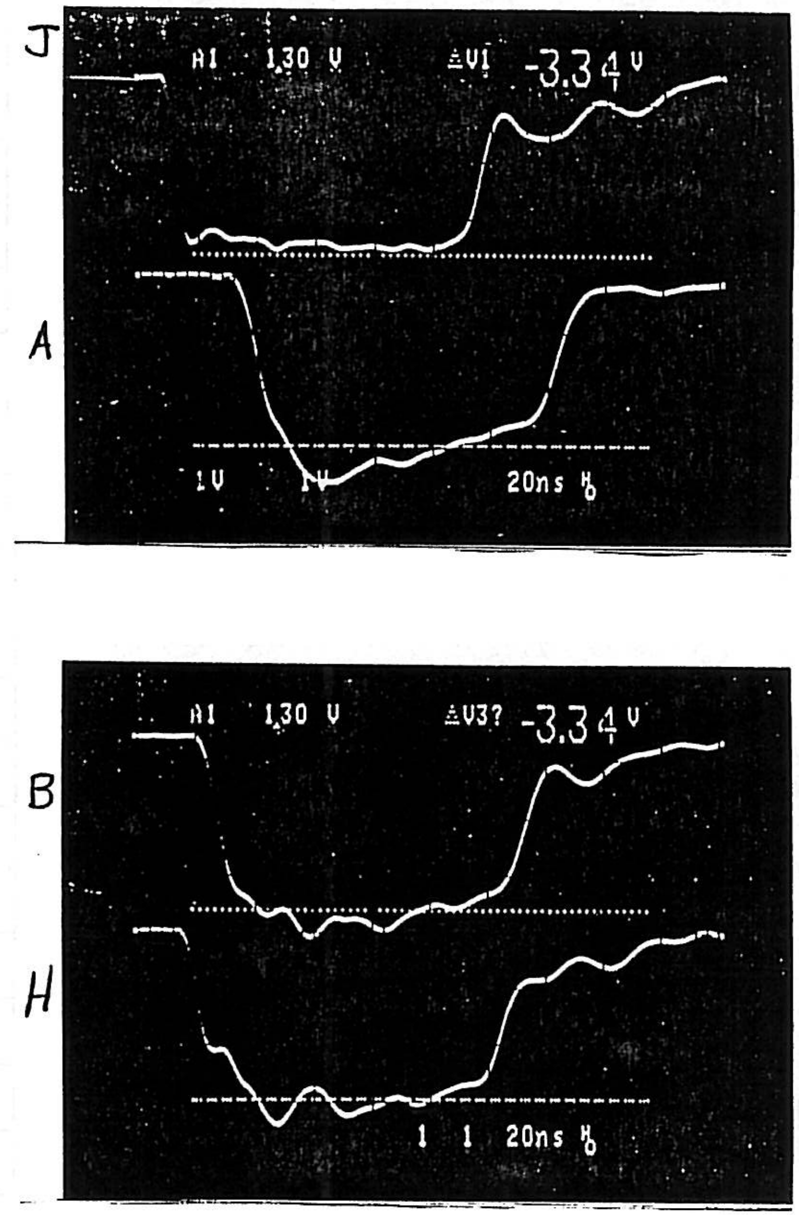
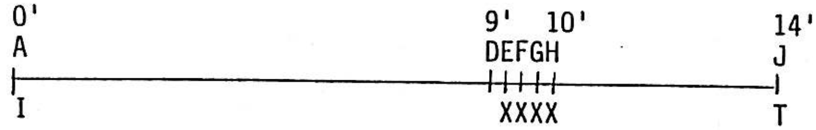


J
A1 1.30 V
ΔV1 -3.34 V
A
1V 1V 20ns
B
A1 1.30 V
ΔV3? -3.34 V
H
1 1 20ns


0'
A
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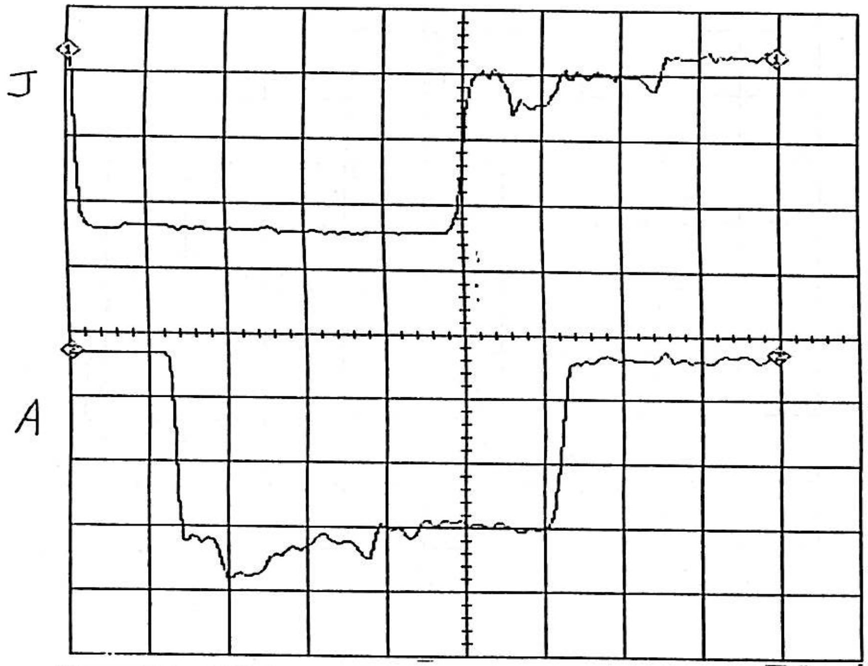
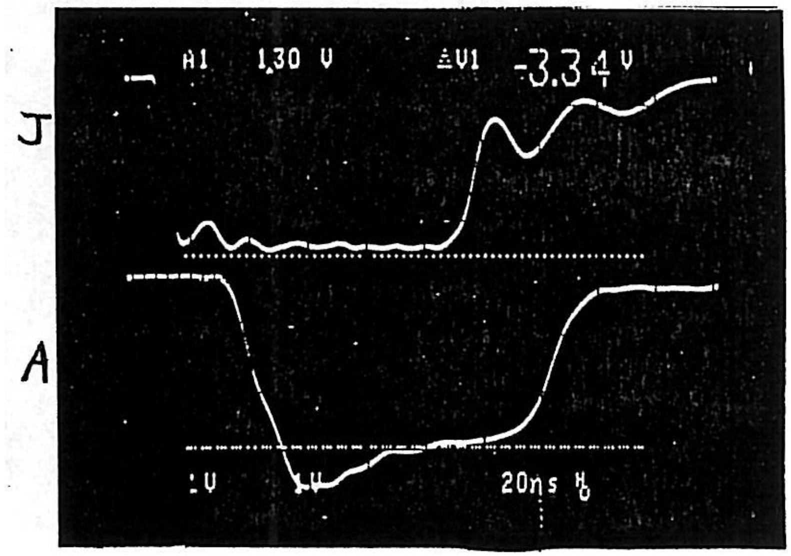
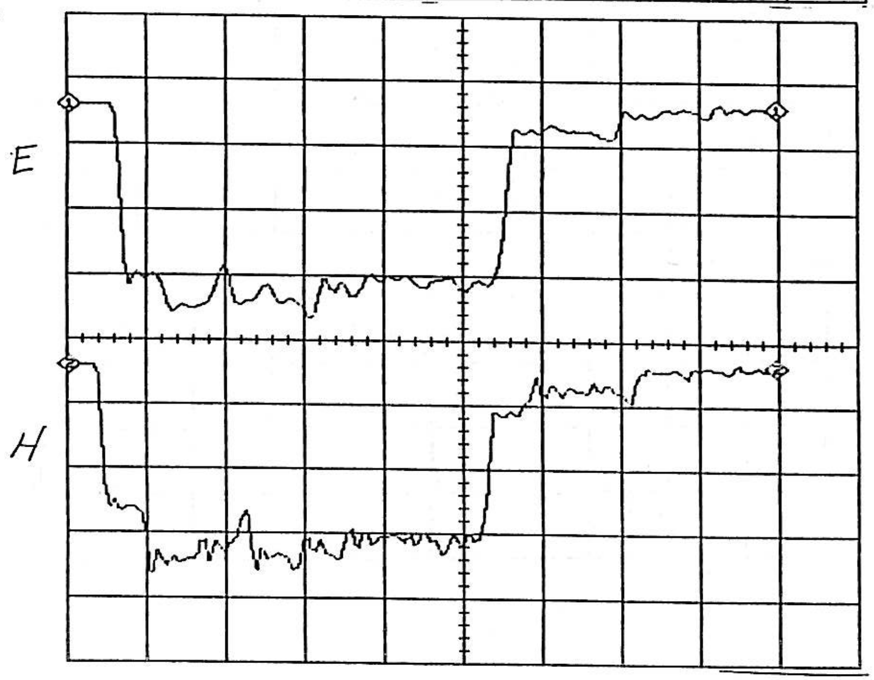
9' 10'
DEFGH
XXXX
14'
J
T

Fig. 3-4


J
A


J
A1 1.30 V
ΔV1 -3.34 V
A
1V 1V 20ns


E
H

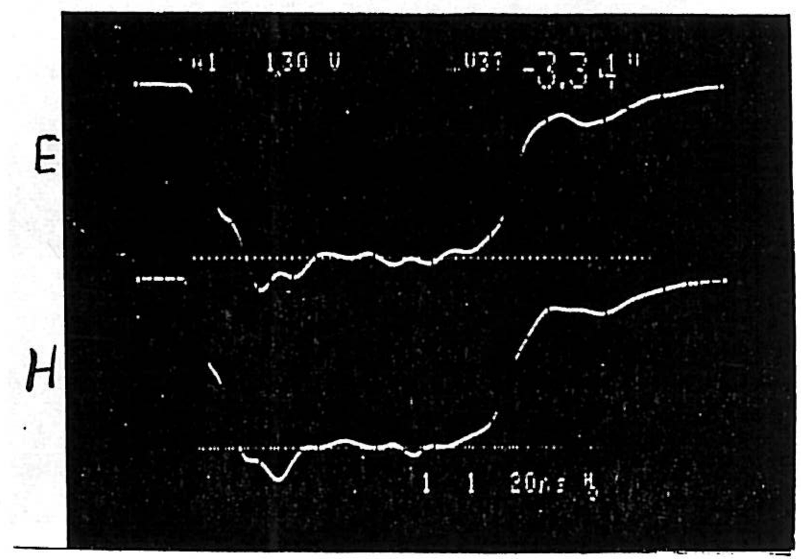

E
H
A1 1.30 V
-3.34 V

Fig. 3-5

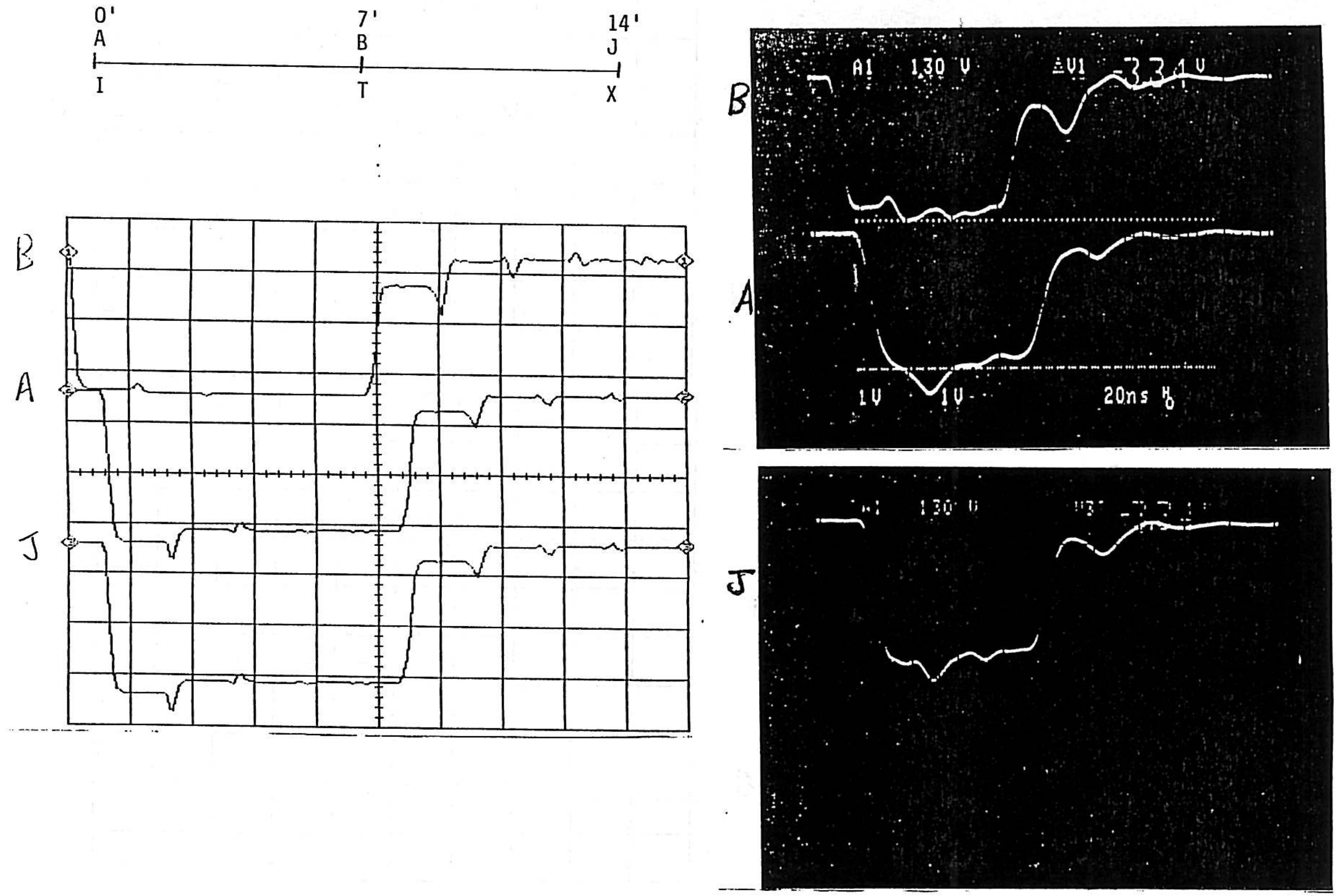
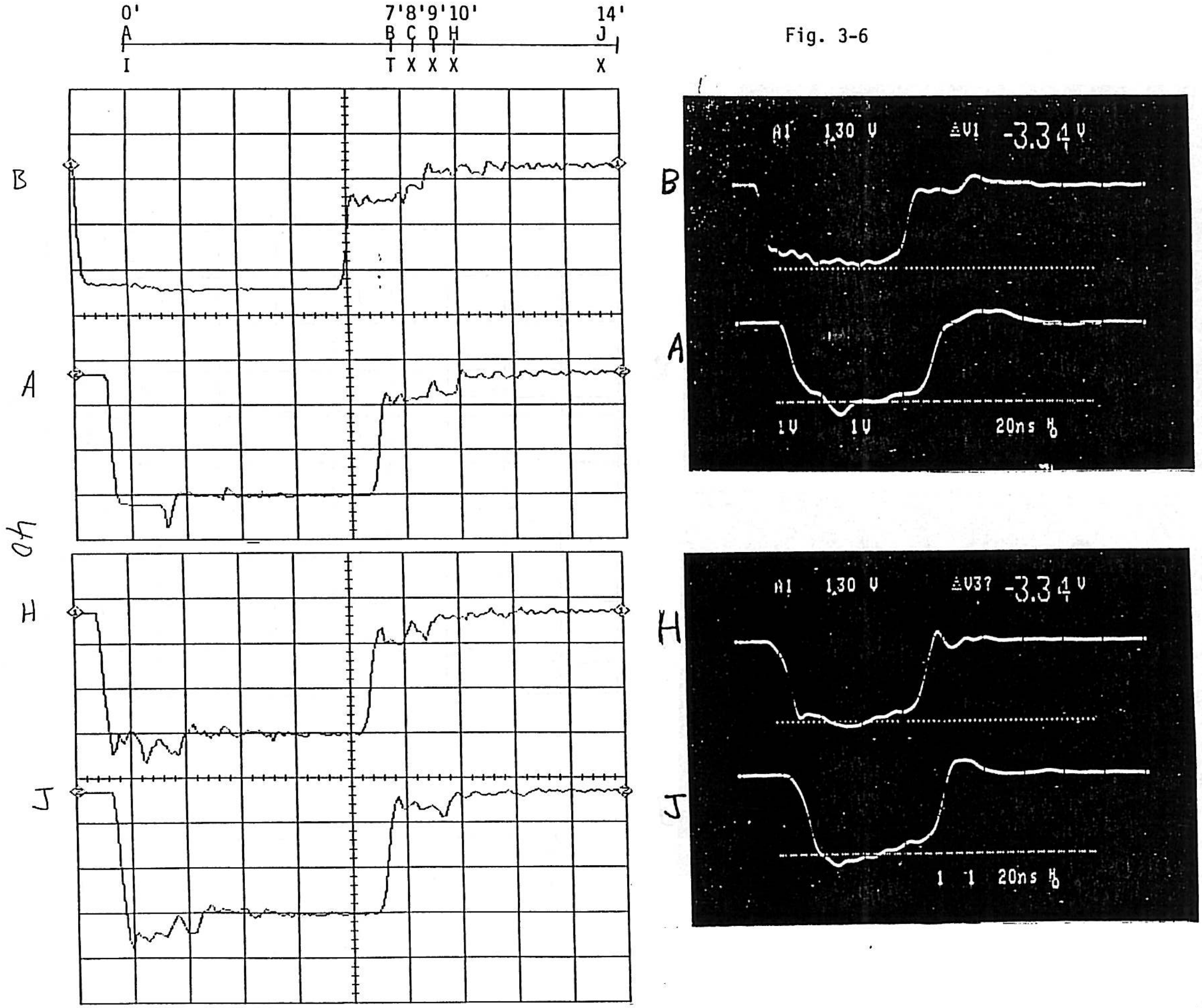


Fig. 3-6



0'
A
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7'8'9'10'
B C D H
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14'
J
X
B
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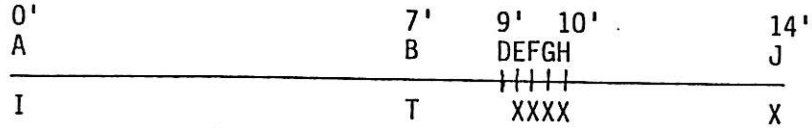
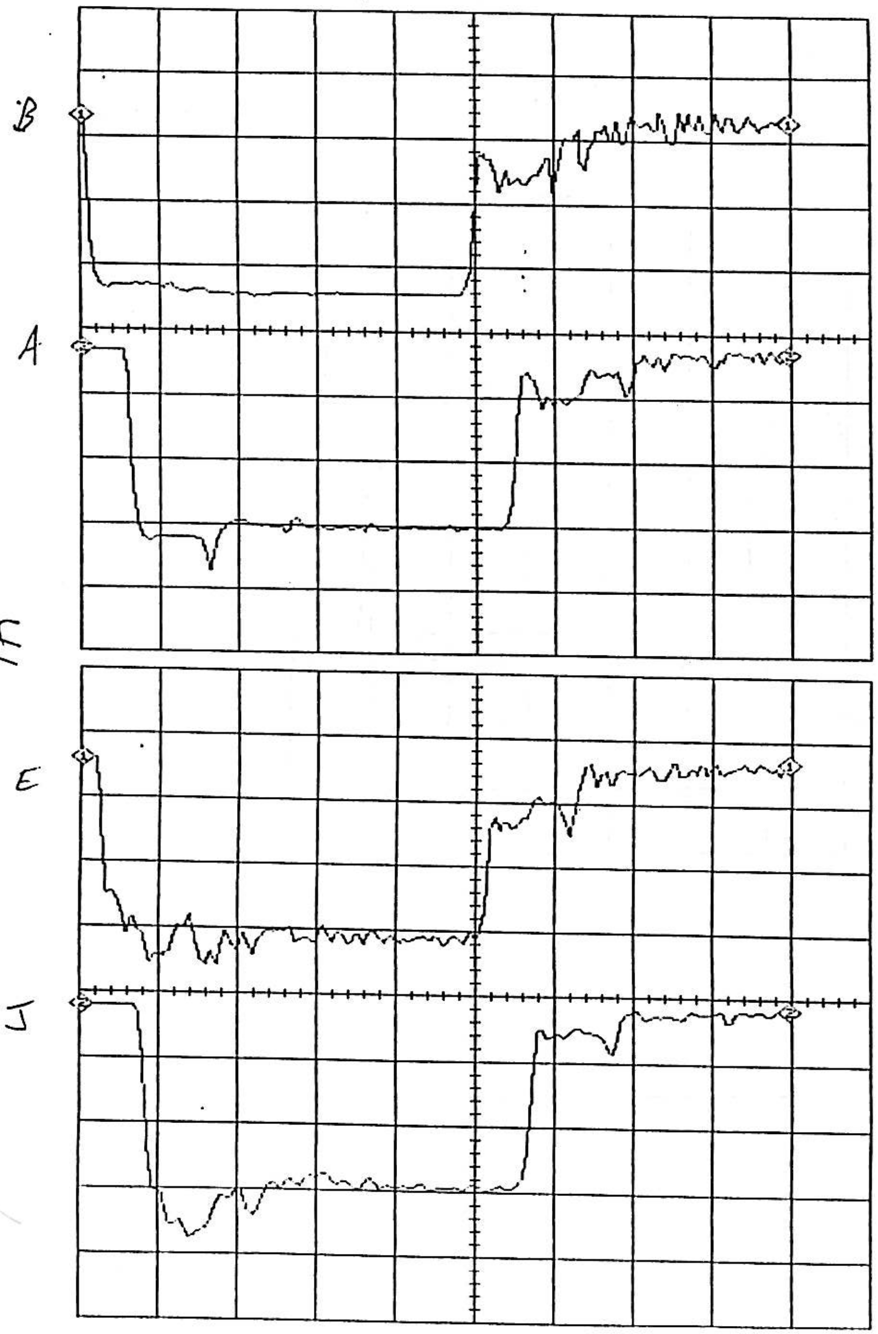
J
A1 1.30 V
ΔV1 -3.34 V
1V 1V 20ns
A1 1.30 V
ΔV3? -3.34 V
1 1 20ns

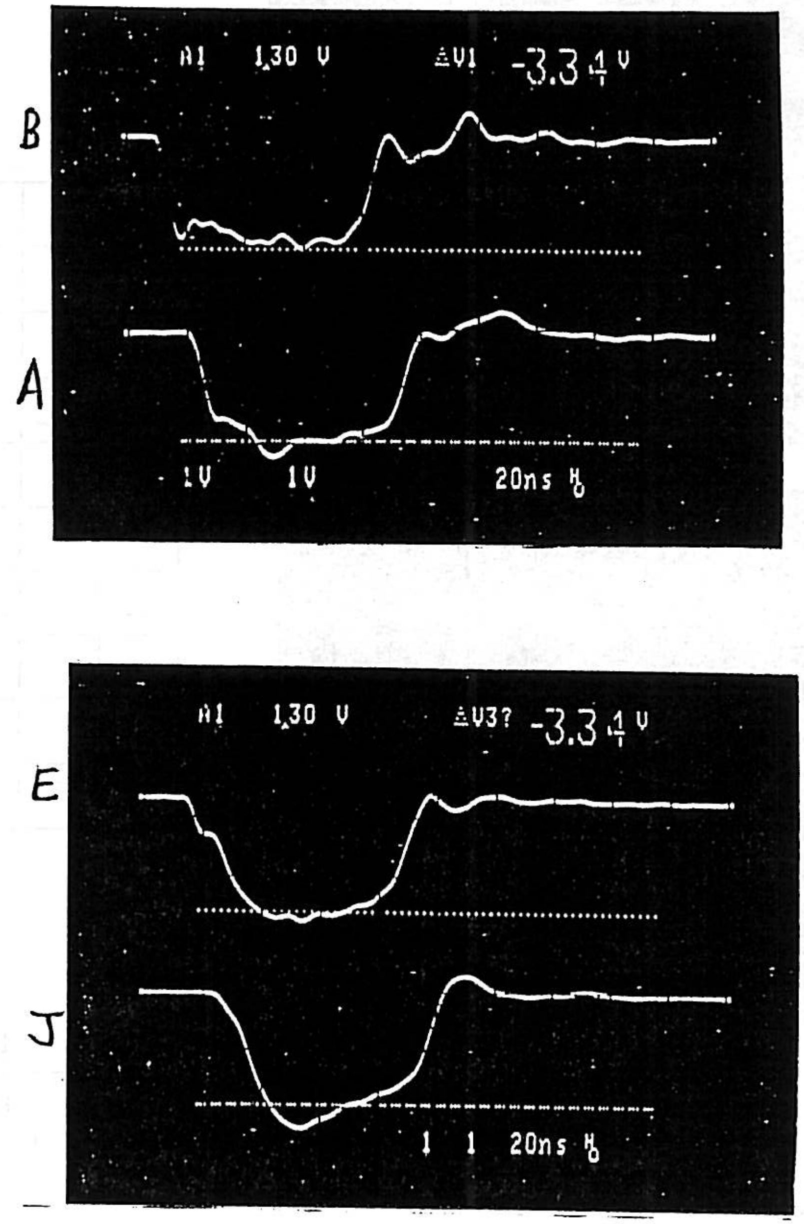


0' A I
7' B T
9' 10' DEFGH XXXX
14' J X

Fig. 3-7



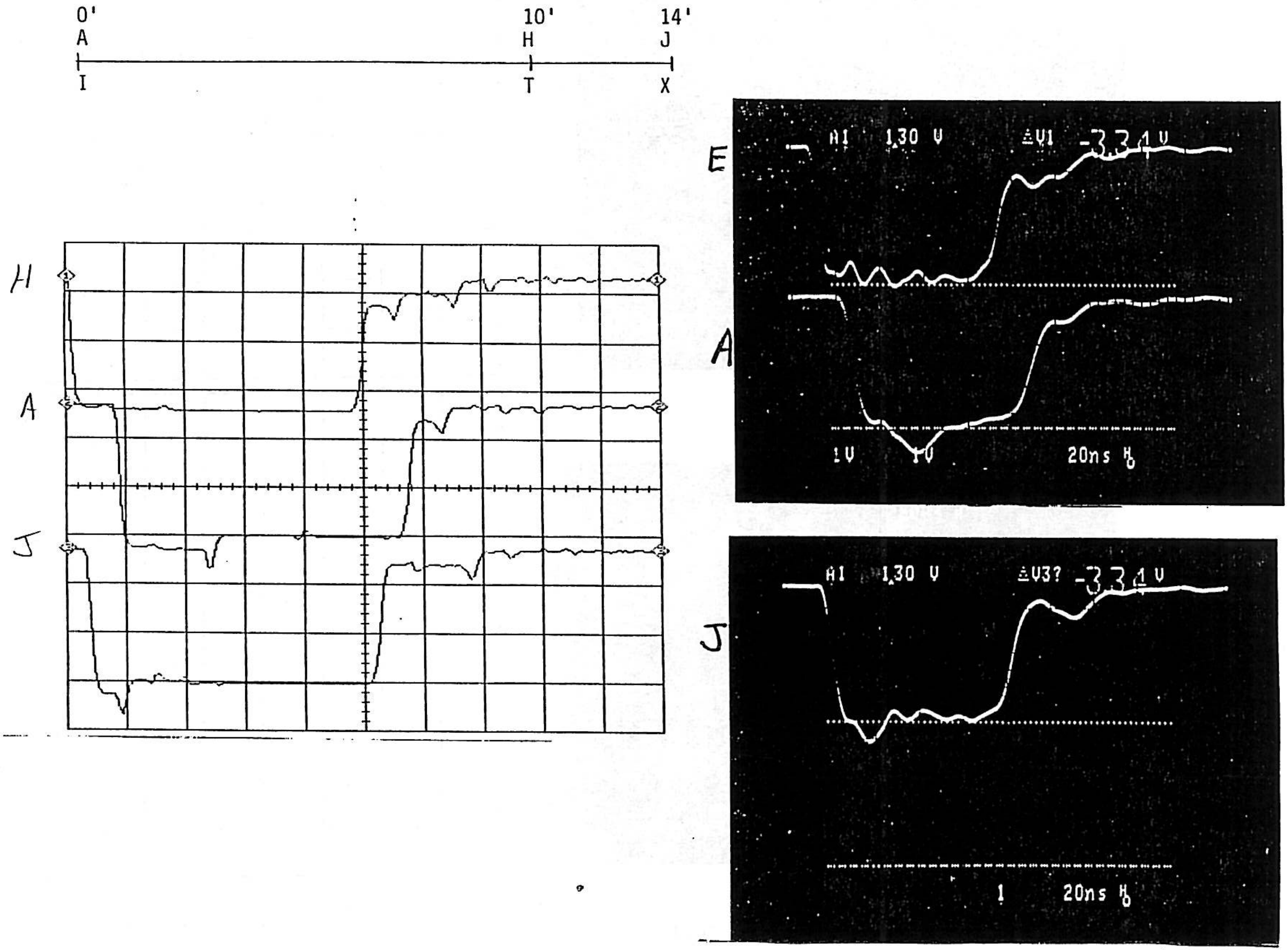
B
A
E
J



A1 1.30 V ΔV1 -3.34 V
B
A
1V 1V 20ns
A1 1.30 V ΔV3? -3.34 V
E
J
1 1 20ns

14

Fig. 3-8



0'
A
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14'
J
X
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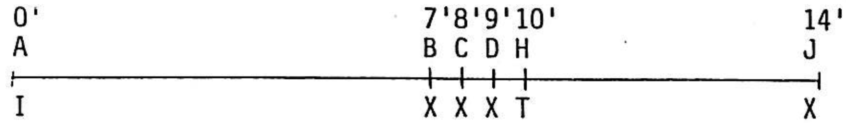
A
J
E
A1 1.30 V
ΔV1 -3.34 V
A
1V
1V
20ns
J
A1 1.30 V
ΔV3? -3.34 V
1
20ns

Fig. 3-9


0'
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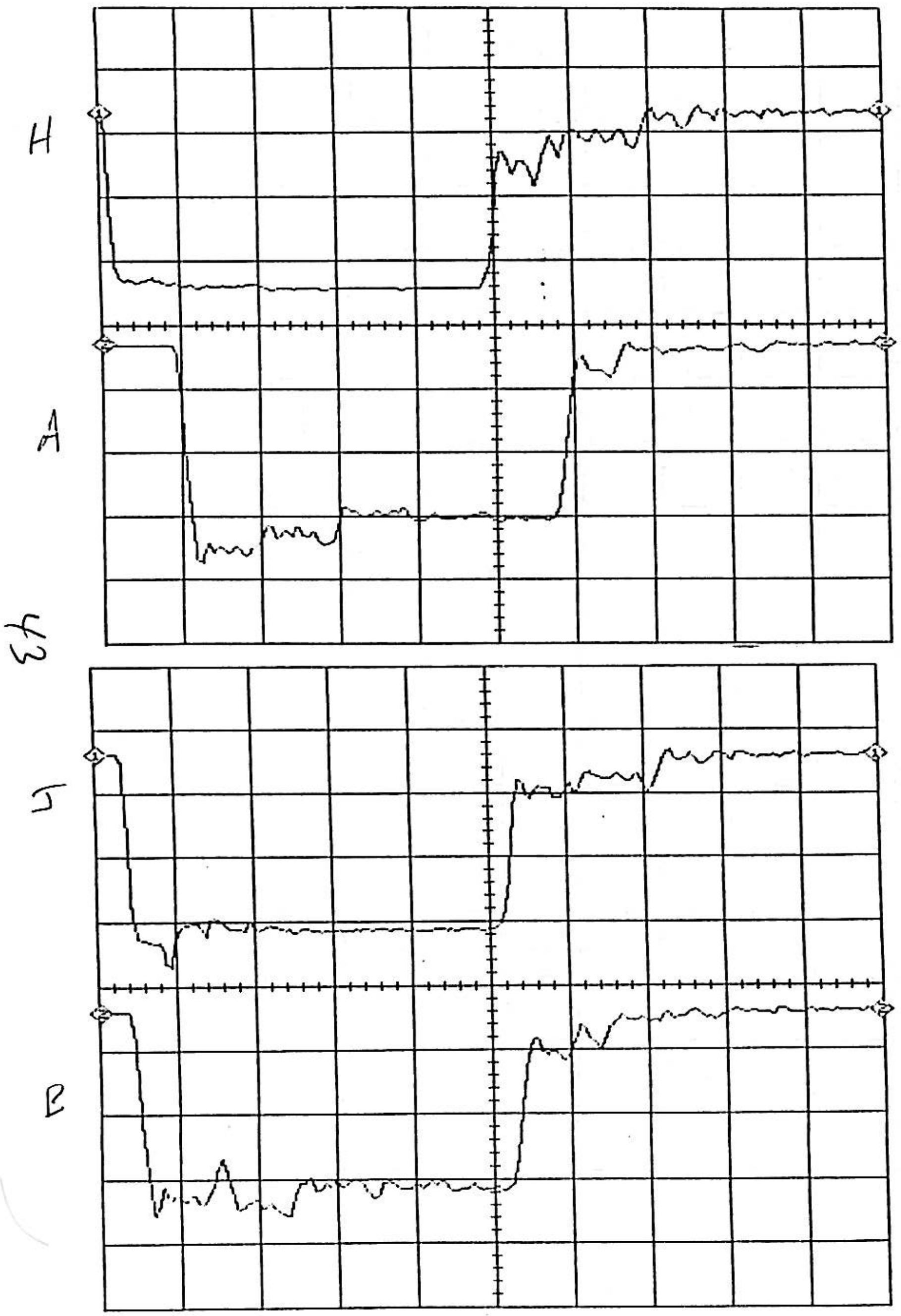
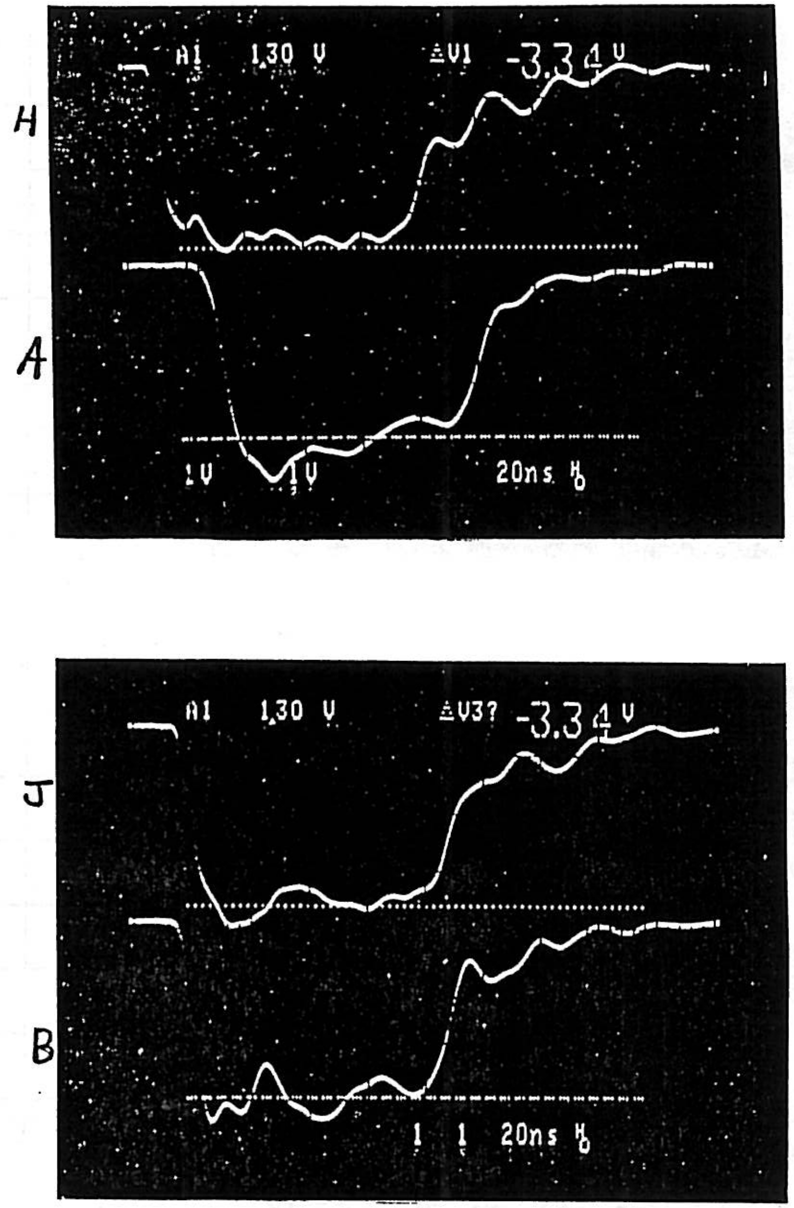
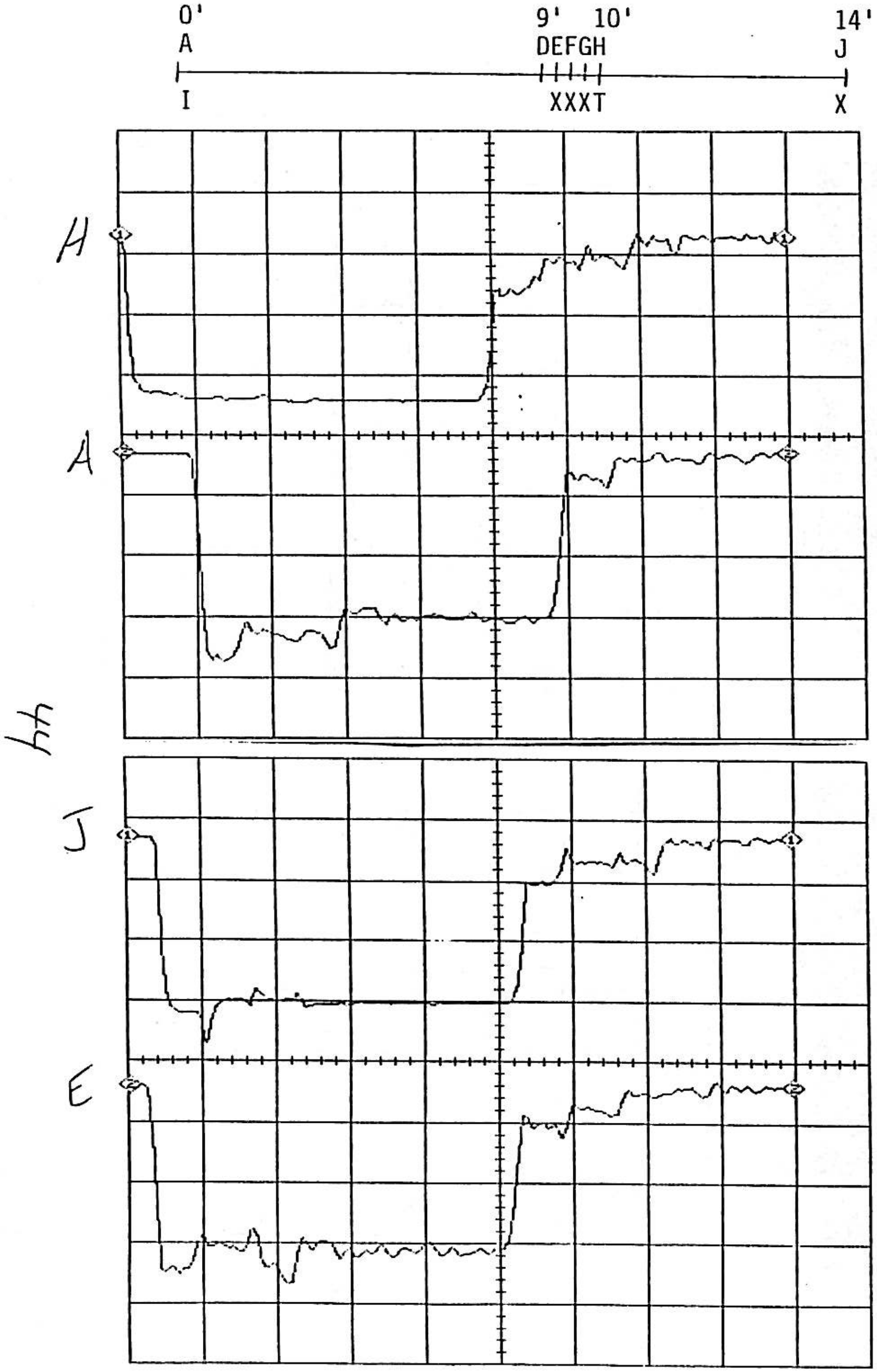
B C D H
X X X T
14'
J
X


H
A
J
B


A1 1.30 V ΔV1 -3.34 V
H
A
1V 1V 20ns
A1 1.30 V ΔV3? -3.34 V
J
B
1 1 20ns



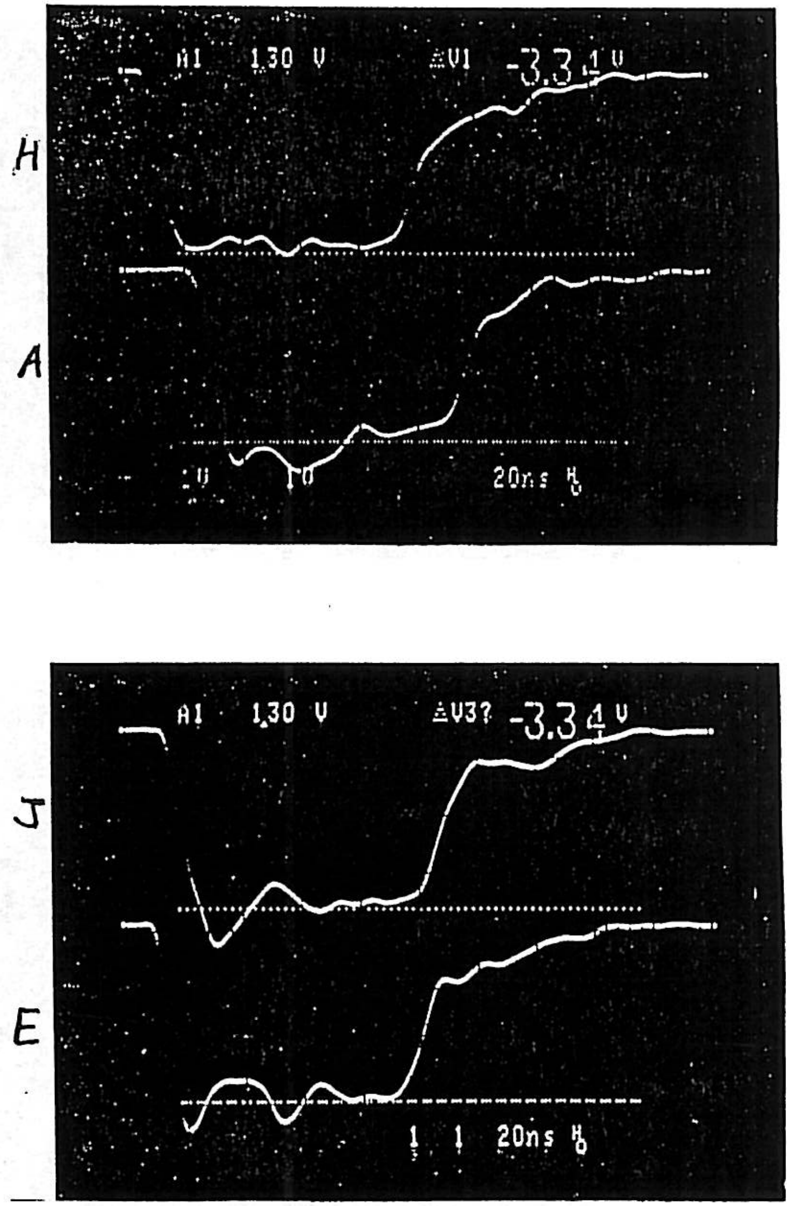
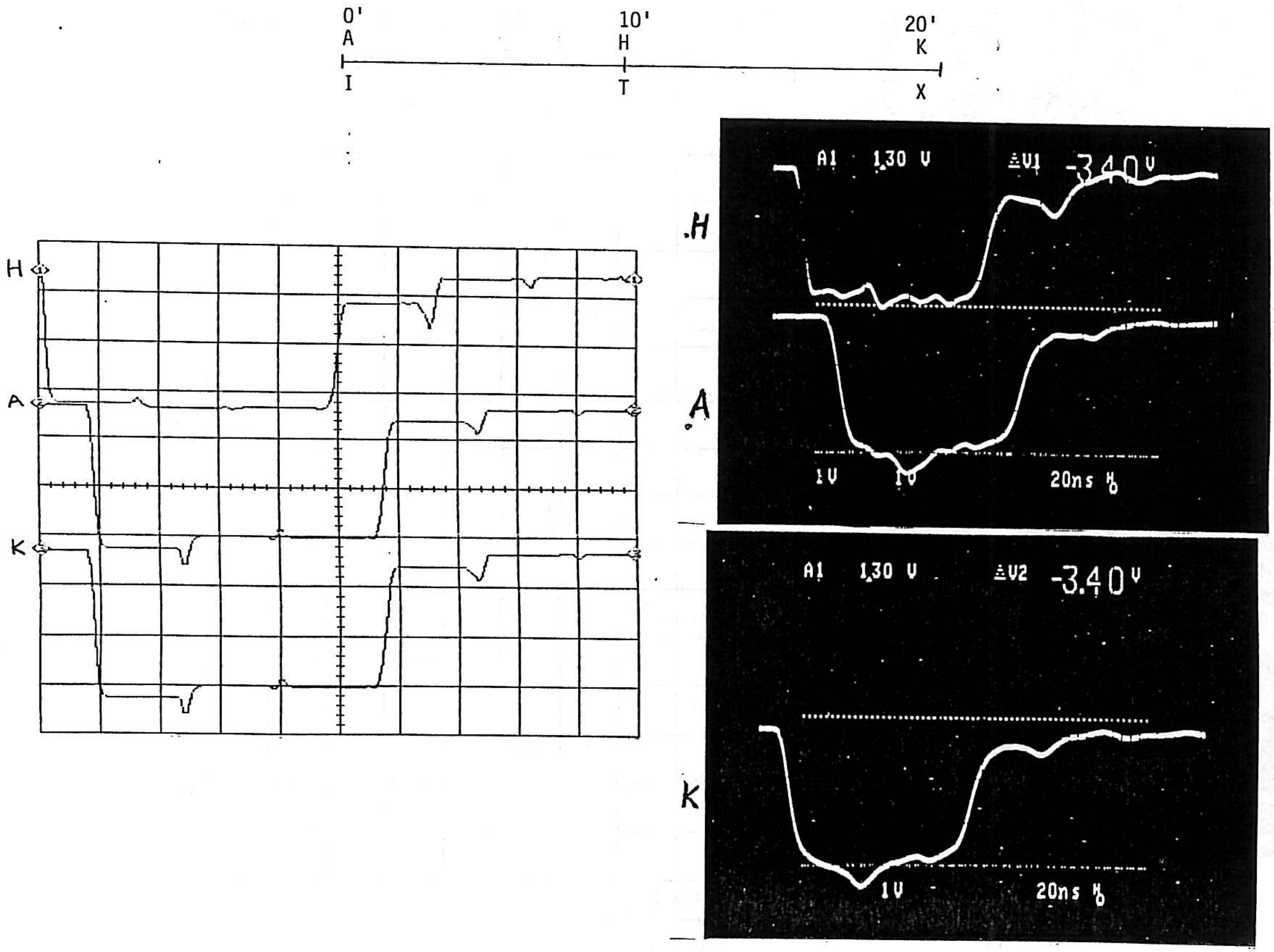


Fig. 3-10

Fig. 3-11



0'
A
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10'
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T
20'
K
X
H
A
K
A1 1.30 V
ΔV1 -3.40 V
1V
1V
20ns
A1 1.30 V
ΔV2 -3.40 V
1V
20ns

Fig. 3-12

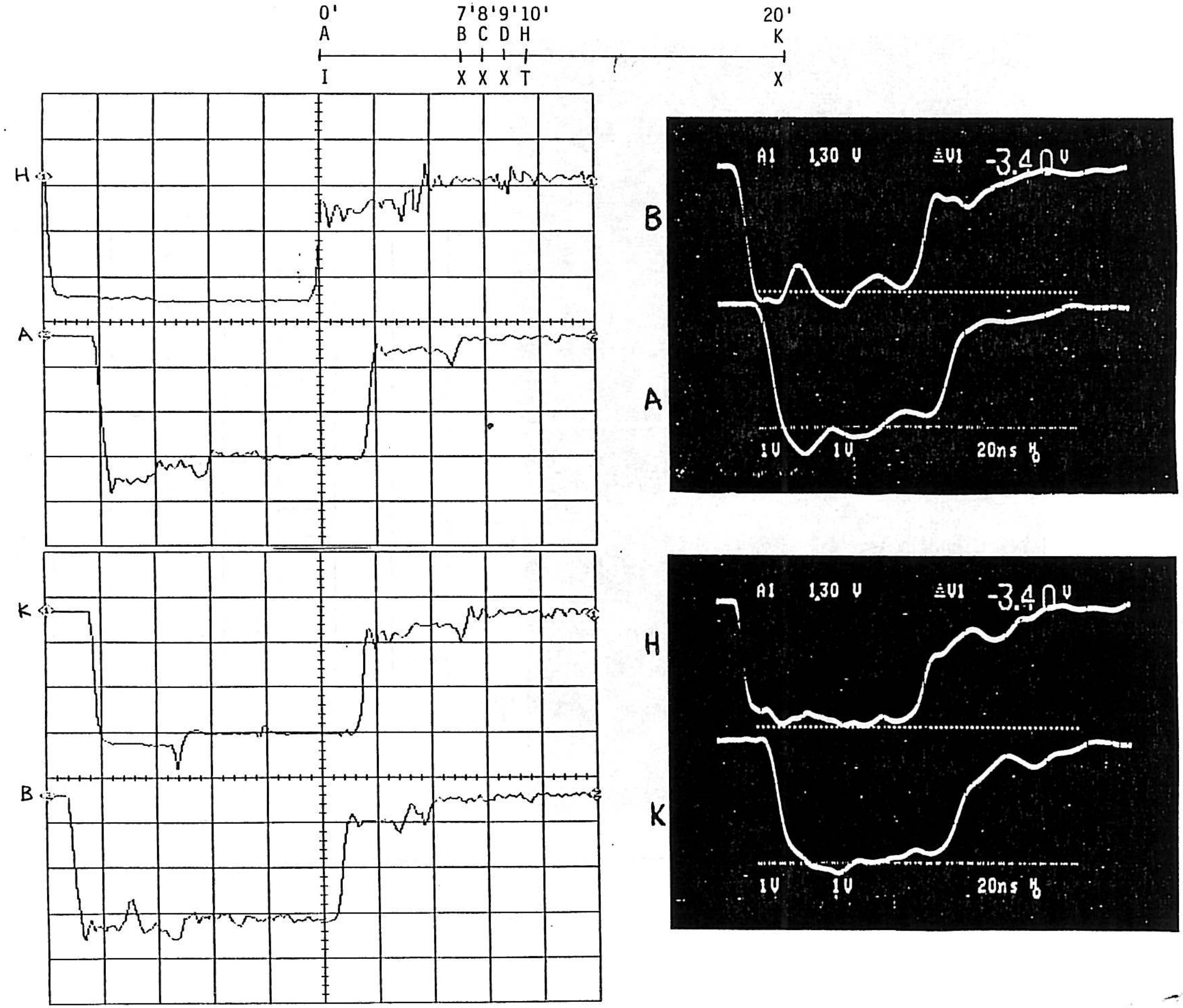


Fig. 3-13

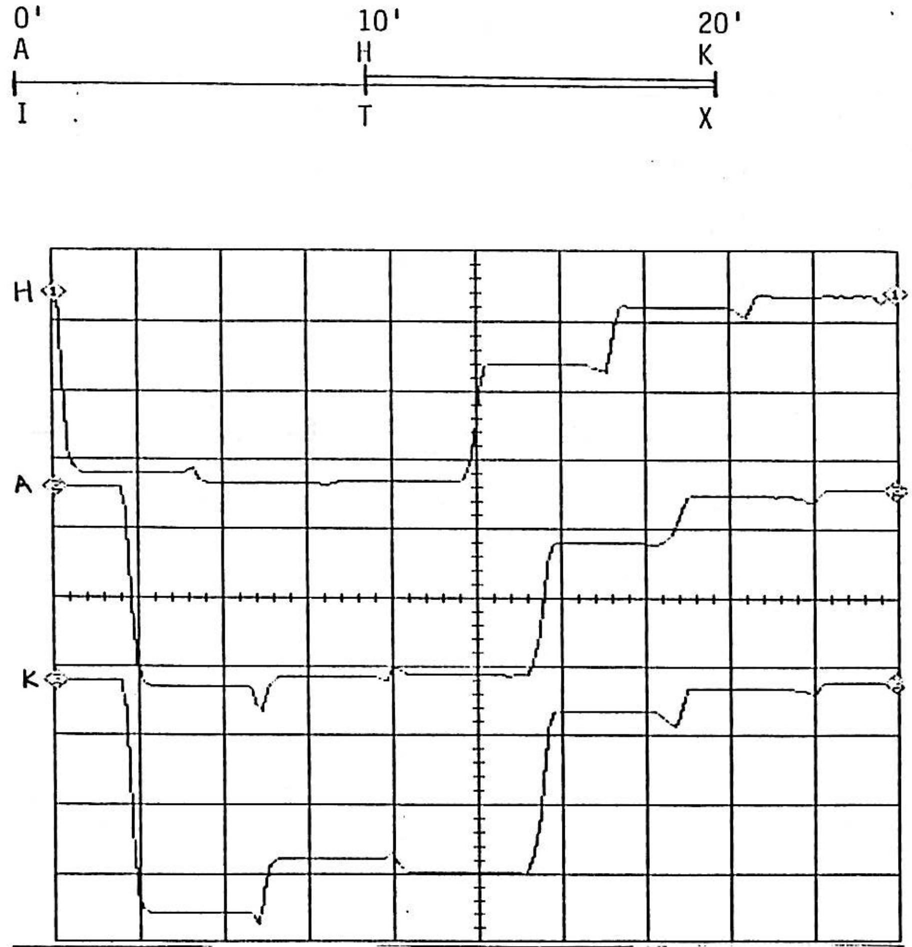


Fig. 3-14

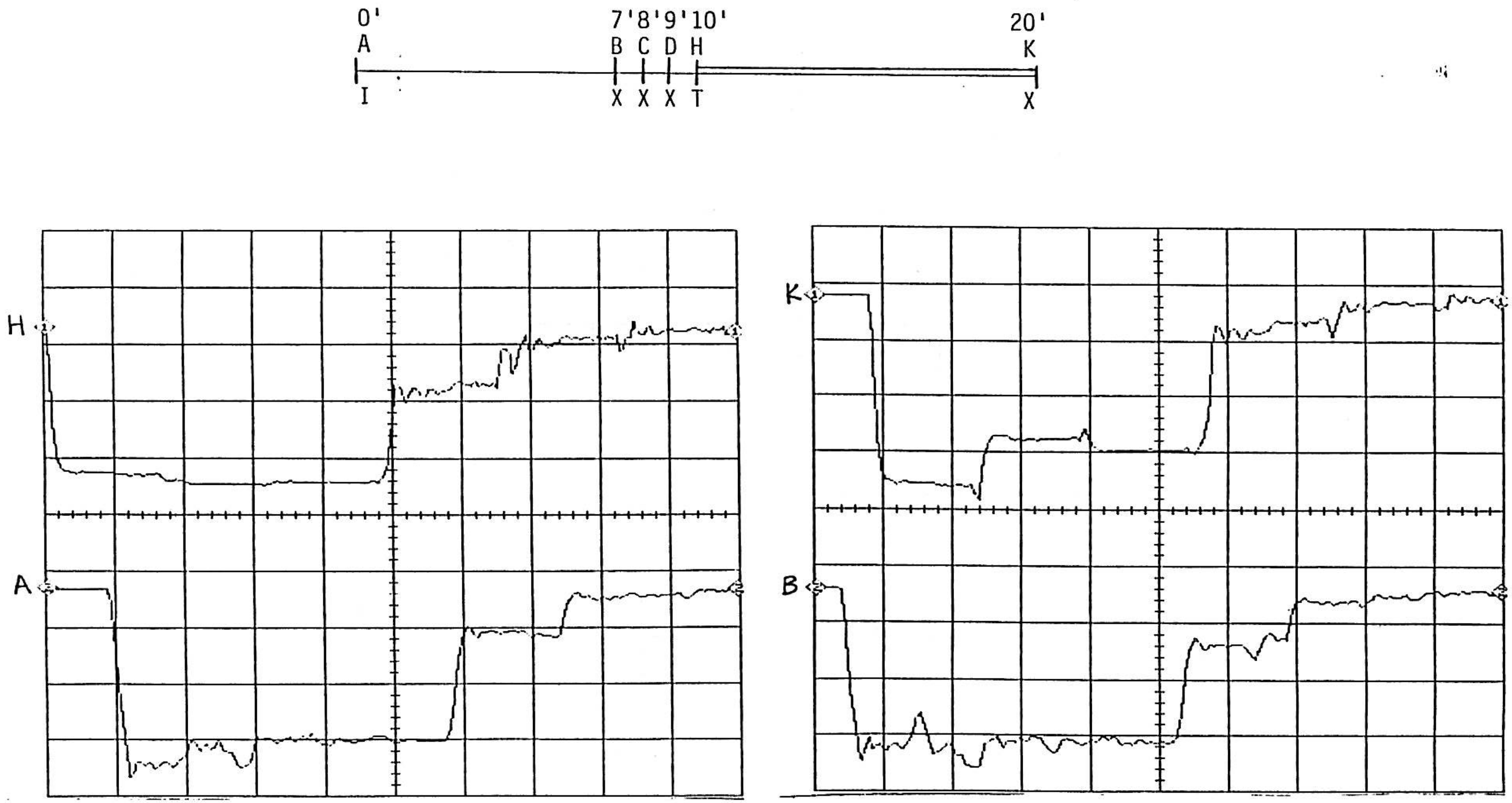


Fig. 4-1

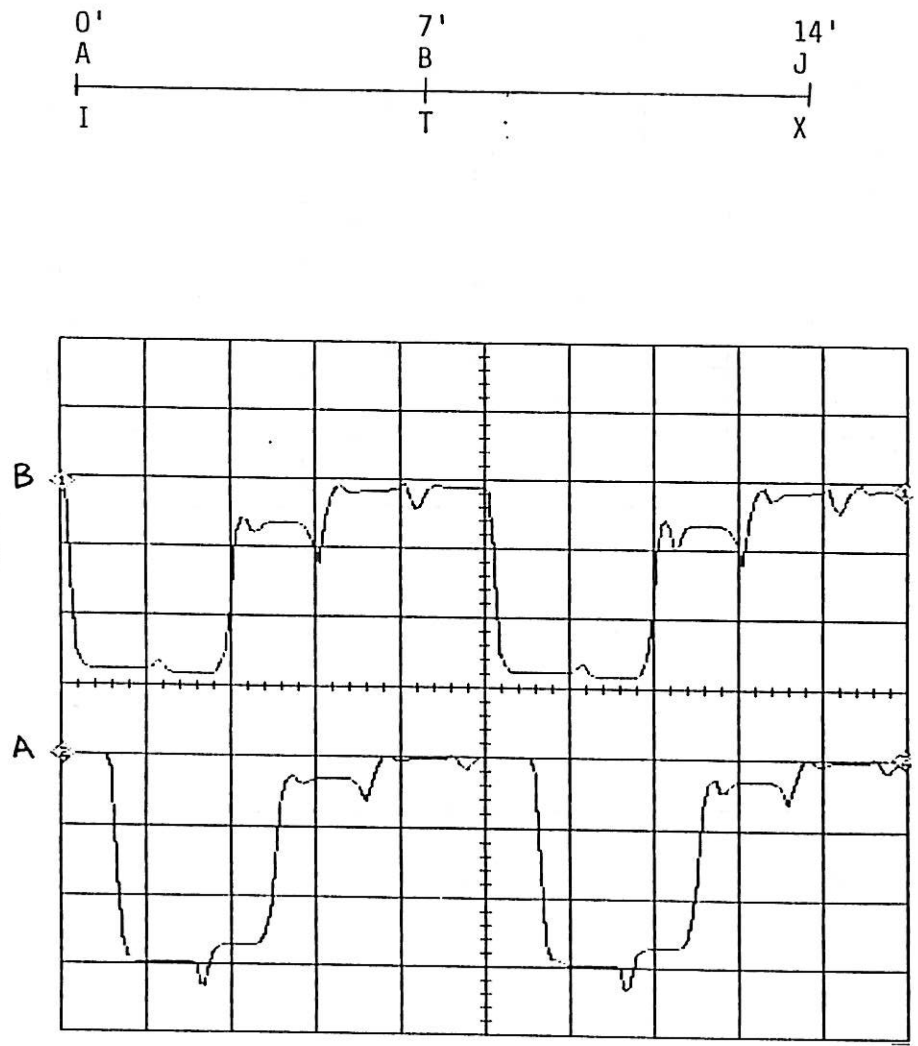


Fig. 4-2

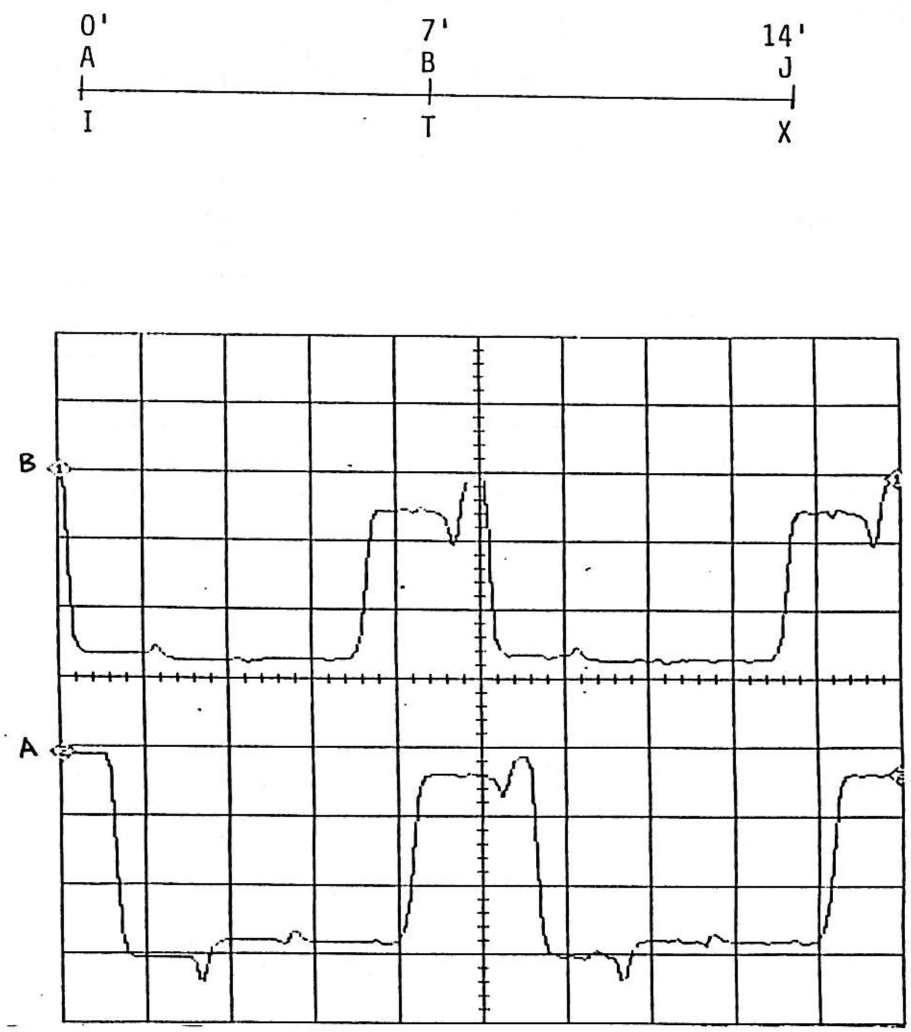


Fig. 4-3 4.25V Term

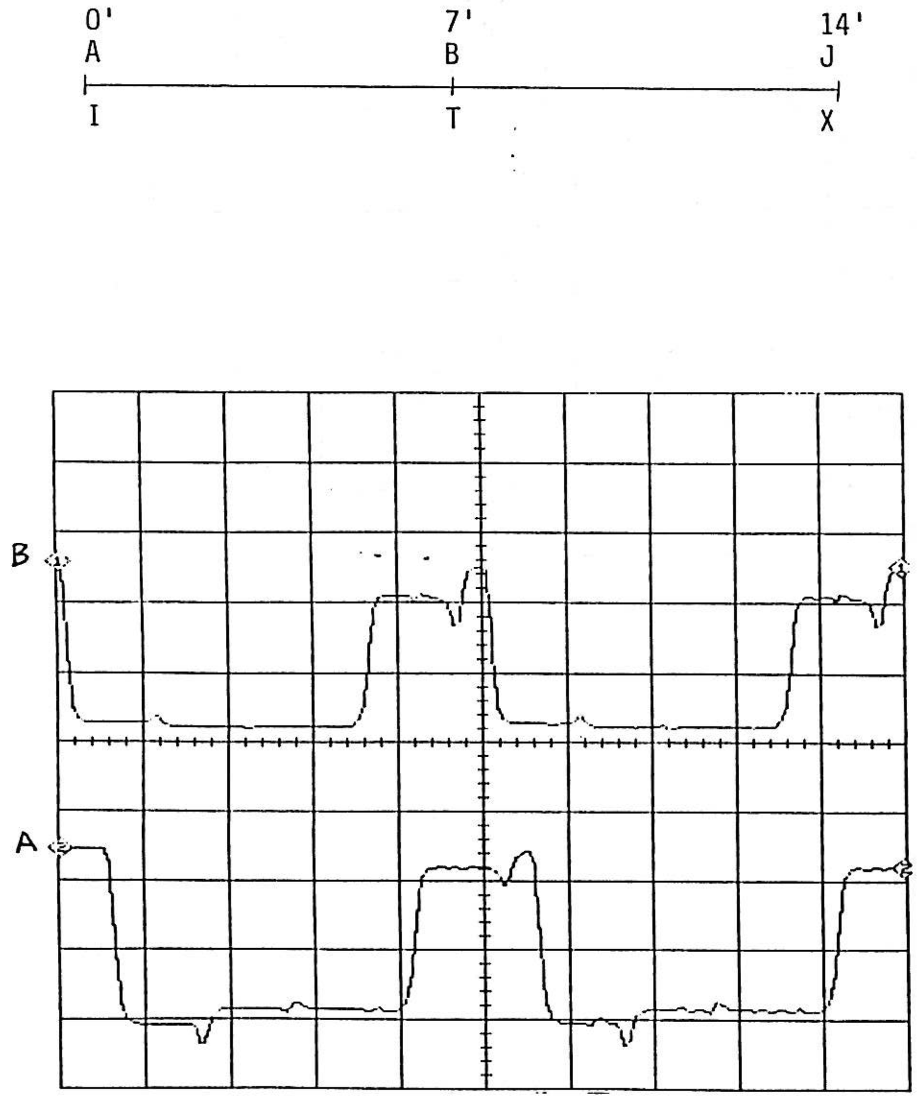


Fig. 4-4

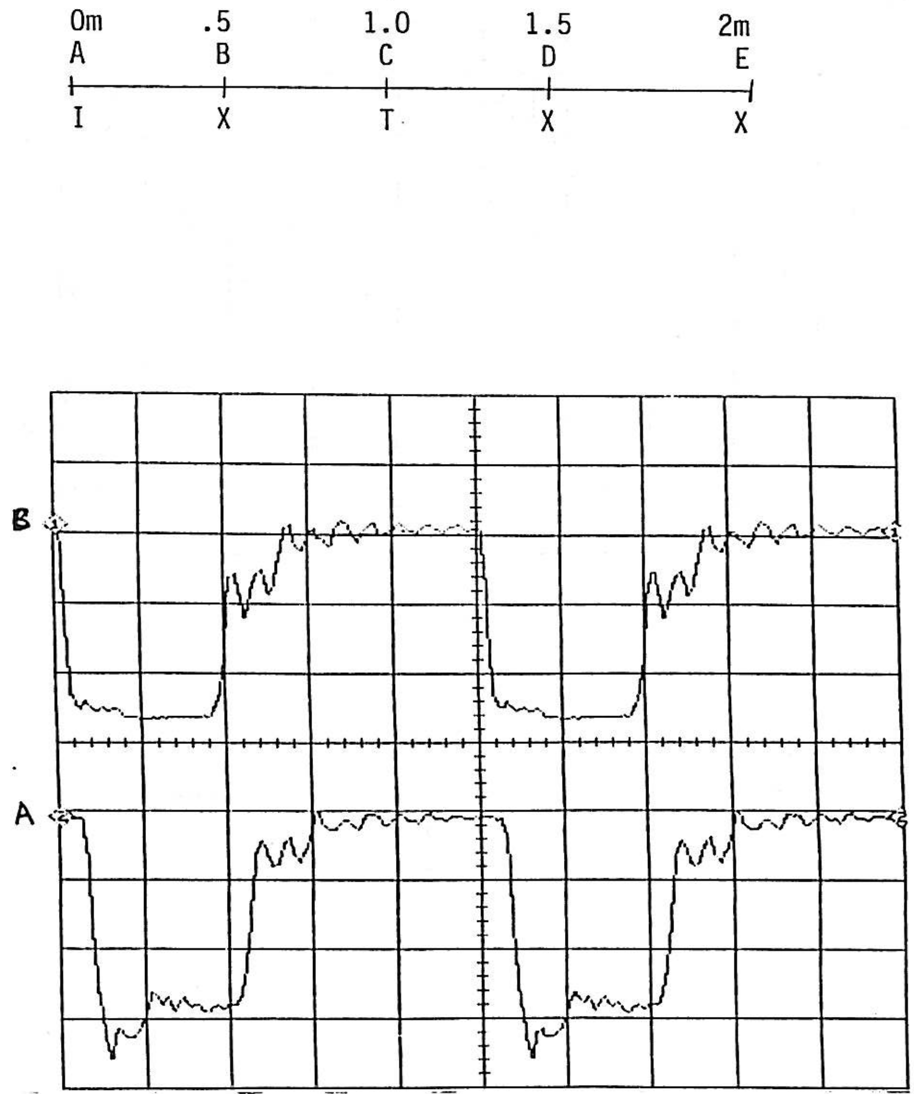


Fig. 4-5

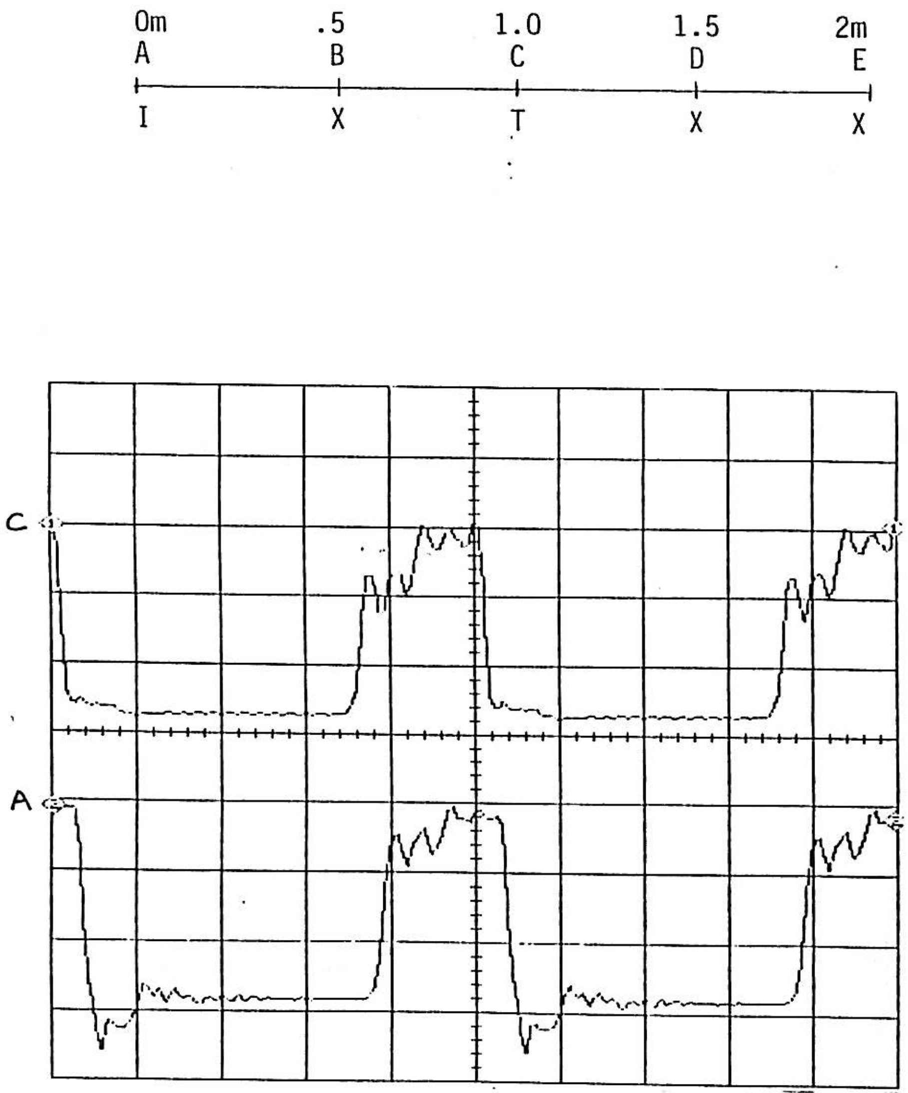
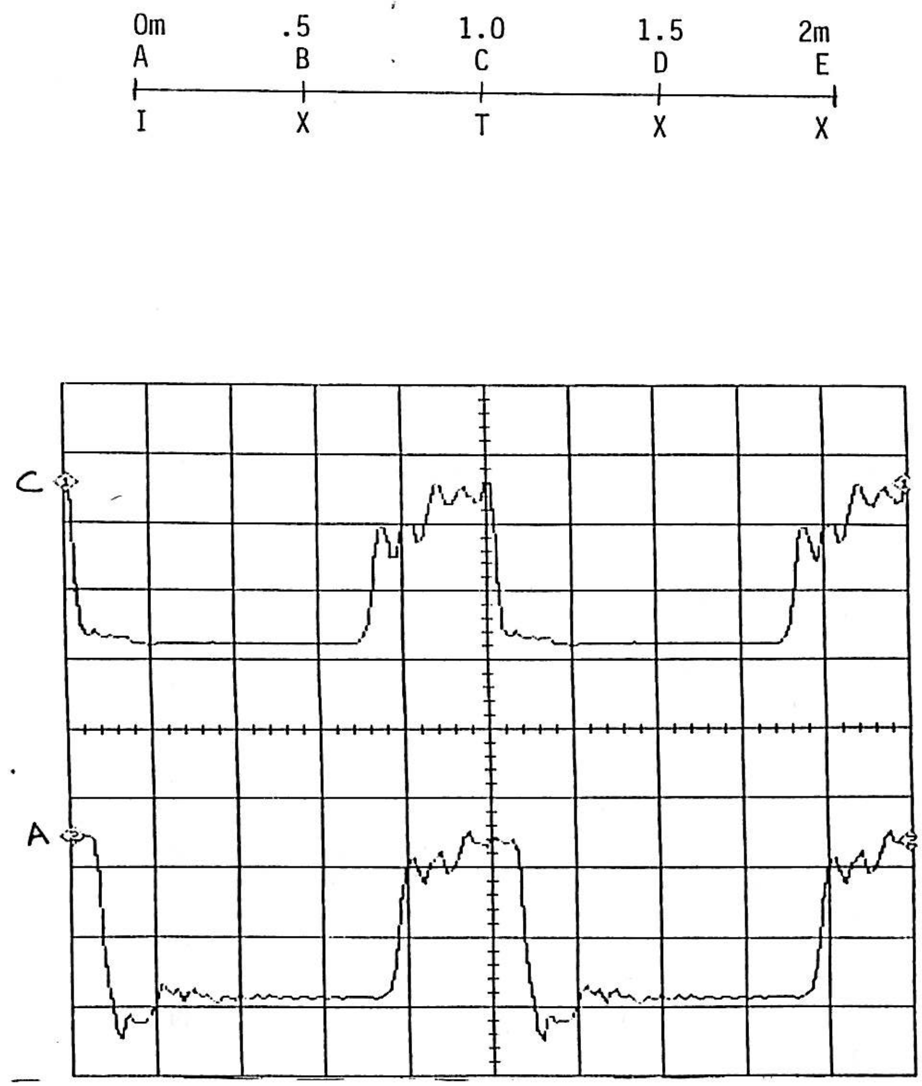


Fig. 4-6 4.25V Term



SCSI Bus Transmission Line Analysis

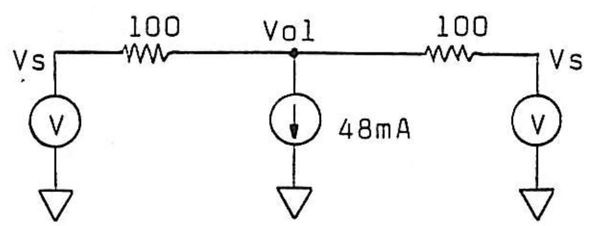
Terminator Resistance Calculation (for Figs. 1-3 through 1-5)

Constraints:

Cable impedance = 100 Ω

Driver output low voltage and current:
Vol = 0.5 V max at Iol = 48 mA

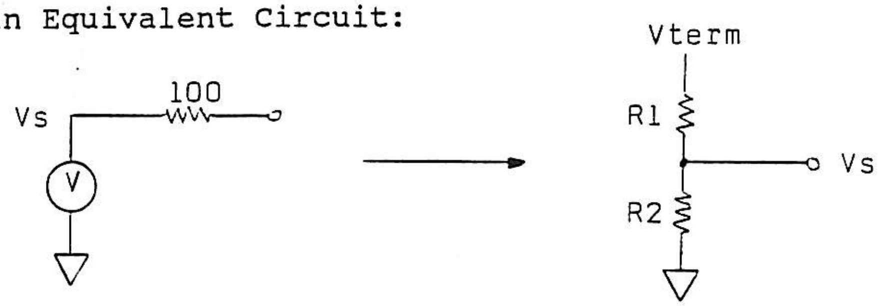
Circuit:



24 mA through each 100 Ω resistor

=> Vs = (24 mA)*(100 Ω) + Vol
= 2.4 V + 0.5 V
= 2.9 V

Thevenin Equivalent Circuit:



$$\frac{R1 \cdot R2}{R1+R2} = 100\ \Omega \qquad Vterm \cdot \frac{R2}{R1+R2} = Vs$$

For Vs = 2.9 V and Vterm = 5 V:

R1 = 172.41 Ω
R2 = 238.10 Ω

Note: With low Vterm the noise margin for signal negation is considerably reduced. If Vterm = 4.25 V:

R1 = 220 Ω, R2 = 330 Ω => Vs = 2.55 V

R1 = 172 Ω, R2 = 238 Ω => Vs = 2.47 V