X3T9.2/87-140

8/13/87

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Si: Review of ESDI X3T9.5/87-005 Revision 1.3

I have finally completed a review of the 18 May document. It is a document which exhibits the benefits of your dedicated efforts as technical editor. I am sorry that my heavy schedule has delayed my final review of this revision. However the delay has allowed me to factor in some inputs we have received from other controller designers contemplating ZBD (ZBR, Notched), ESDI controllers.

Since there is a desire to have all the comments concerning the ESDI available at the 17 August meeting, I have included all of my comments. You will find that some of the following comments could wait for the massaging of the ANSI editor. However, I think we both prefer that the final edit be limited to selecting type face and the appropriate roster of the parent committees. In order to minimize flipping back and forth through the document to find the areas being commented upon, I have attempted to keep the comments in the order they appear in the document, regardless of importance. Since there are quite a few comments, I am using the committee's latest mode of editing by striking out what was there and using italics for what is added in many cases. With this convention I am hoping the reasons will be self evident and an limiting explanation to only the more involved suggestions. However, this method of modifying in context tends to make this letter much more massive than the limited number of requested changes intended. Please do not infer that the size of this submittal indicates major problems with the document. To the contrary, it is a well done, highly useful document.

I am uploading this package to the committee BBS in two versions. One is this complete document under the file name ESDI[87.807. The other has only the changes and is in a series of files named CHG-XXX.087 where XXX corresponds to the same XXX as you have for your ANSI XXX files which comprise the ESDI document.

With the preliminaries out of the way, my comments are:

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The smaller size and low power requirements of small form factor drives led to the development of higher capacity (100 MB+), faster data rate (10 Mbit) and fast access time (sub -20 msecs+). To support these kinds of products it was felt that a new interface which was electrically compatible with that used on the lower end products would provide a simpler upgrade path than any other alternative.

Comment: The strike out is difficult to see except on a terminal. In this case it is nearly impossible. "(sub-20 msecs+) becomes "(sub 20 msecs)". It is also difficult to see the italics in some instances. If I'm able to get the time, I will try an underlined version.

An ad hoc industry group of controller and device manufacturers agreed to pursue this direction as a common effort and the first working document was introduced in May, 1985. This initial effort defined the Enhanced Small Disk Interface but after the definition of the Enhanced Small Tape Interface it was decided to merge the two into a single document in October, 1985 as the Enhanced Small Device Interface. In January, 1985 it was proposed that a version suitable for optical disk be incorporated and the first working draft was issued in March, 1985. NOTE: In May, 1987 It was agreed that *the Enhanced Small Device Interface on* tape did not have broad industry acceptance and would not be incorporated in the standard.

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This standard does not require that both of these be available on the drive; rather it is the choice of the manufacturer on which to implement. If desired, both may be offered with a selection method provided by the manufacturer. It is strongly recommended that controller implementations be designed to support both Fixed and Soft Sector drives.

Page 3 2

The raw error rate of recording at such high densities is high, and it is necessary to use extended and sophisticated error correction techniques so that the final error rate achieved is comparable to magnetic media. Provision has been made for implementation of an erasure pointer correction scheme.

Comment: This may be true. However someone that has not already implemented it will not be able to find it. Does this refer to the "Post Field" which "... may contain addressing information which can point to a replacement sector." or does it refer to the "Pre-Recorded Data Pointer"?

Page 4 2

Optional

This term describes features which are not required by the standard. However, if any feature defined by the standard is implemented, it shall be done in the same way as defined by *comply with* the standard.

Sector

This term refers to the address and data areas identified by the disk drive, relative to index, with zero as the first

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Track

That area of the disk accessible by a single head *without changing the head position*, within a single cylinder. A track may be read or written during one rotation of the disk.

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Write Splice

An area of the disk produced when writing begins or *ends*. Data in the write splice area on the disk is undefined and must not be read from the disk.

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In high speed applications, driver and receiver *delay variations* skew specifications are critical for timing calculations.

Page 6-1

	Disk Signals	Optical Signals	Signal Pin	Ground Pin
	Cable is Flat Ribbon (3 meters maximum)			
--->	HEAD SELECT 2(3)	Reserved	2	1
--->	HEAD SELECT 2(2)	Reserved	4	3
--->	WRITE GATE	=	6	5
<---	CONFIG/STATUS Data	=	8	7
<---	TRANSFER ACK	=	10	9
<---	ATTENTION	=	12	11
--->	HEAD SELECT 2(0)	SIDE SELECT	14	13
<---	SECTOR/AM FOUND	SECTOR	16	15
--->	HEAD SELECT 2(1)	Reserved	18	17
<---	INDEX	=	20	19
<---	READY	=	22	21
--->	TRANSFER REQ	=	24	23
--->	DRIVE SELECT 2(0)	=	26	25
--->	DRIVE SELECT 2(1)	=	28	27
--->	DRIVE SELECT 2(2)	=	30	29
--->	READ GATE	=	32	31
--->	COMMAND DATA	=	34	33

TABLE 6-1 CONTROL CABLE (J1/P1) PIN ASSIGNMENTS

	Disk Signals	Optical Signals	Signal Pin	Ground Pin
	Cable is Flat Ribbon (3 meters maximum)			
<---	DRIVE SELECTED	=	1	
<---	SECTOR/AM FOUND	SECTOR	2	
<---	COMMAND COMPLETE	=	3	
--->	ADDRESS MARK ENABLE	Reserved	4	
	GROUND	=	5	
--->	+/-WRITE CLOCK	=	7/8	6
	GROUND	=	9	
<---	+/-READ/REFERENCE CLOCK	=	10/11	12
--->	+/-NRZ WRITE DATA	=	13/14	15/16
<---	+/-NRZ READ DATA	=	17/18	19
<---	INDEX	=	20	

TABLE 6-2 DATA CABLE (J2/P2) PIN ASSIGNMENTS

Note: In tables 6-1 and 6-2 "=" indicates that the Optical signal has the same nomenclature as the Disk signal.

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6.2.2 HEAD SELECT 2(0), 2(1), 2(2), and 2(3) (D-O)

6.2.2.1 Disk

These four lines allow selection of each individual read/write

head in a binary coded sequence. HEAD SELECT 2(0) is the least significant line. Heads are numbered 0 through 15. When all HEAD SELECT lines are negated, head 0 shall be selected. Addressing more than 16 heads is allowed by use of the SELECT HEAD GROUP command.

A 150 OHM resistor pack allows for line termination.

Comment: The prior sentence is too much of an implementation statement and is not compatible with the optional termination. This objectionable sentence occurs many places and I believe is always redundant and/or at odds with the option.

If only one side is supported by a drive then this line may be ignored.

Comment: I will defer to optical implementors and integrators if they are unanimous in leaving in the struck sentence. However, it seems to me that it invites undetected errors.

Page 6-5

The parity utilized in all commands shall be odd. The parity bit shall be a "1" when the number of "1's" in a 16 bit command is an even number. The number of "1" bits in the command, plus parity, shall be an odd number.

No communications should be initiated attempted unless the COMMAND COMPLETE line is asserted. just prior to the start of the transfer. Note: This line shall be negated when not in use.

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6.3.2 READY (D-0)

6.3.2.1 Disk

This signal indicates only that the spindle is up to speed.

When this interface signal is asserted it indicates that the drive spindle is up to speed. When this signal is negated the drive spindle is not up to speed.

6.3.2.2 Optical

This signal indicates that the spindle is up to speed. This interface signal when asserted, together with COMMAND COMPLETE indicates that the drive is ready to read, write or, seek, *providing that Attention is not also asserted.* When the line is negated, all reading, writing and seeking is inhibited.

Comment: I don't see any distinction between optical and disk. Consequently I suggest one or the other paragraphs be used to cover both.

6.3.3 CONFIG/STATUS *DATA* (D-0)

The drive presents serial data on the Configuration/Status Data line upon request from the controller. See Figure 10-5 for typical operation. This config/-status serial data shall be presented to the interface and transferred using the handshake protocol with signals TRANSFER REQ and TRANSFER ACK. See Figure 10-2. Once initiated, 16 bits plus parity shall be transmitted MSB first. The parity utilized shall be odd.

Comment: The "-" does not show in the printed copy but is in the disk file. "config-status" changes to "config/status".

Page 6-7

6.3.5 ATTENTION (D-0)

ATTENTION is asserted when the drive wants the controller to request its standard status. Generally, this is a result of a fault condition or a change of status.

If a selected device encounters an unexpected condition which causes it to become busy and unable to respond to the controller it shall assert ATTENTION in conjunction with the negation of COMMAND COMPLETE.

Writing is inhibited when ATTENTION is asserted.

ATTENTION is negated by the Control Command with the Reset Interface Attention modifier set only if the condition which caused it to occur no longer exists.

Comment: As I recall the Boston working group meeting the function in the second paragraph was added for a mechanism to hold off the controller without regard to whether the reason was expected or not expected. In my mind, the condition would likely be expected by the drive and unexpected by the controller (granting to both the faculty to anticipate).

6.3.7 SECTOR/ADDRESS MARK FOUND (D-0)

These signals are available on the control cable (gated) and on the radial data cable (ungated). *One* Both of these signals shall be implemented *on both cables* by the drive manufacturer.
6.3.7.2 Disk Soft Sector (ADDRESS MARK FOUND)

Page 6-8

- o Whenever the drive is unable to respond to the interface e.g. during recovery from internally detected error conditions. If this should occur during the time that the device is selected, then ATTENTION shall be asserted to advise the controller that an unexpected event has occurred and that the device is busy

and unable to respond to the interface. *If COMMAND COMPLETE was negated due to an error condition, when the device is able to respond to the interface, it shall continue to assert ATTENTION and assert COMMAND COMPLETE. If COMMAND COMPLETE was negated due to a normal, non error condition, when the device is able to respond to the interface, it shall negate ATTENTION and then assert COMMAND COMPLETE.*

NOTE: NRZ READ DATA carries erasure pointer data during an erasure read in an optical disk drive.

Comment: Is this note of any value without any information on what an erasure read is?

Page 7-6

NOTE: The controller should respond with a Request Status command for any command transfer protocol timeout. Some drives have been built which implement Additional Vendor Unique Status in 8-15. The controller can manage this by requesting as many Vendor Unique status words as reported in *the device's* its Configuration response.

TABLE 7-5 REQUEST STATUS MODIFIER BITS

o Request Standard Status: When the command modifier bits 11-8 of the Request Status command *are is* 0000, the drive shall respond with 16 bits of Standard Status. Settings in this status may or may not be fault or change of status bits that cause ATTENTION to be asserted each time one is set.

Comment: The discrepancy between your assumption that the phrase's subject is "command modifier" and my assumption that it is "bits" occurs in quite a few places.

Page 7-7

o Request Device Type or Additional Vendor Unique Status or Reserved: When the command modifier bits 11-8 of the Request Status command is 1000-1111, the drive responds with all zeros if it is Reserved. The number of words available is specified by configuration data. If Device Type Status is defined in this specification it shall be reported, or additional vendor unique status may be provided. Each word of Additional Vendor Unique Status is requested using a different command modifier configuration. The command modifier for the first word is 1000 and subsequent words are requested by incrementing the command modifier by one.

Comment: To me, the description reads like ESDI has the capability to RESERVE a drive. Is the paragraph really referring to devices which report more words available than are implemented and/or to reserved configuration words? Assuming the latter, I suggest "or RESERVED" be struck from the command title and the description changed to "... all zeros if the response word is reserved . The number ...". In addition the whole paragraph appears to be in conflict with Table 7-5. After reflecting over the the table and this paragraph, the following replacement paragraphs come to mind to replace all of the material after Table 7-5 on pages 7-6 and 7-7:

o Request Standard Status: When the command modifier bits 11-8 of the Request Status command are 0000 and the Subscript is 0, the drive shall respond with 16 bits of Standard Status. Settings in this status may or may not be fault or change of status bits that cause ATTENTION to be asserted each time one is set.

o Request Extended Standard Status: When the command modifier bits 11-8 of the Request Status command are 0000 and the Subscript is 1, the drive shall respond with 16 bits of Extended Standard Status. Settings in this status may or may not be fault or change of status bits that cause ATTENTION to be asserted each time one is set.

o Request Vendor Unique Status: When the command modifier bits 11-8 of the Request Status command are 0001-0111, the drive responds with Vendor Unique Status (undefined in this specification). The number of words available is specified by configuration data. Each word of Vendor Unique Status is requested using a different command modifier configuration. The command modifier for the first word is 0001 and subsequent words are requested by incrementing the command modifier.

o Request Optical Device Status : When the command modifier bits 11-8 of the Request Status command are 1001, the drive responds in accordance with Table 7-8.

o Request Current Track Position : When the command modifier bits 11-8 of the Request Status command are 1010, the optical drive responds in accordance with Table 7-9.

Note: If the controller requests a *reserved* status *word* by incrementing through the various Command Modifier Bits, or if a reserved function is randomly requested, the device shall respond with all zeros. The number of Vendor Unique Status words available is specified by configuration data. Each word of Additional Vendor Unique Status is requested using a different command modifier configuration.

Page 7-8

Comment: I suggest that Table 7-7 bits 13 and 12 be modified. Please note that my comments are based upon the disk file which is different than the printed document.

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14	1	= ...able Media Not Present	0
	0	= Removable Media Present *or not Removable*	0
13	1	= Write Protected - Removable Media	0
	0	= *Not Write Protected or not Removable Media*	0
12	1	= Write Protected - Fixed Media	0
	0	= *Not Write Protected or not Fixed Media*	0
3	1	= Write Gate with Track Offset Fault #3	1
2	1	= Vendor Unique Status Not Associated with Error Condition	0
	1	= Vendor Unique Status Available for Error Condition	1
1	1	= Write Fault #2	1

* *If bit 3 is set, bit 1 shall also be set.*

Comment: I suggest moving the Synchronized Spindle response from Extended Status to Standard Status using bit 10 (or 11 if Optical wants the same status). I would architecturally maintain Extended Status but, for this publication, have it all reserved. If a controller is not the master, what should the Master drive report? Is it always synchronized from a status viewpoint? I'm interested in inputs of the host variety.

Page 7-10

A Status Response complying with Table 7-7 is returned when the Command Modifier bits are 0000 *and the Subscript is 0*, and lists the conditions under which the Status Response bits shall be set and if ATTENTION is asserted.

3	Reserved	0

#3 Conditions that can cause Write Fault are:

a) Excessive write current.
b) Multiple heads selected, no head selected, or improperly selected with WRITE GATE asserted.
c) DC voltages grossly out of tolerance.
d) WRITE GATE asserted to a previously recorded or flagged defective sector
e) Simultaneous assertion of READ GATE and WRITE GATE if DRDW not implemented.

Comment: Since optical can implement track offset, I wonder why bit 3 should be different than disk. Since the early part of the document commented that optical disks typically have only one head, I wonder why multiple heads are included in an example of conditions which can cause a write fault. Is DRDW needed in the optical?

Page 7-11/12

7.6.3.2 Optical Device Status/Current Track Position

There are two additional status response words (Optical Device Status and Current Track Position) returned to the controller in response to the Request Device Status command.

A Status Response complying with Table 7-8 is returned when the Command Modifier bits are 1001. *Table 7-8* and lists the conditions under which the Status Response bits shall be set and if ATTENTION is asserted.

Bit	Status Response	ATTI
15	Drive Initialization Failure	1
14	Sensor Failure	1
13	Cartridge Load/Unload Failure	1
12	Spindle Not at Speed Failure	1
11	Focus Failure	1
10	Phase Lock/Tracking Failure	1
9	Tracking Failure	1
8	PLO Failure due to Laser Dying	1
7	Not Track Following	1
6	Not on Correct Track	1
5	Coarse Seek Failure	1
4	Write was Terminated	1
3	Eject Request	1
2	MO (MagnetoOptic) - Erase Encoded:10=Erase 11=Transition	x
1	- Write 01=Write 00=Off	x
0	Reserved	0

Note: The encoded responses are shown with Bit 2 first and Bit 1 second.

TABLE 7-8 OPTICAL DISK DEVICE STATUS RESPONSE BITS

A Status Response complying with Table 7-9 is returned when the Command Modifier bits are 1010. Bits 15-8 define the current Track High order byte and bits 7-0 define the current Track Low order byte. NOTE: A drive which implements the Distance/Direction type of Seek only shall respond to this status request with an Invalid Command Fault.

Bit	Status Response	ATT
15	Current Track High Order Byte - MSB	0
14		0
13		0
12		0
11		0
10		0
9		0
8	Current Track High Order Byte - LSB	0
7	Current Track Low Order Byte - MSB	0
6		0
5		0
4		0
3		0
2		0
1		0
0	Current Track Low Order Byte - LSB	0

TABLE 7-9 OPTICAL DISK CURRENT TRACK STATUS RESPONSE

General Configuration response flags shall be used to verify the validity of the responses. Actually I thought configuration flags were specified in the tape section which has been removed.

Comment: Does everyone except myself know what General Configuration response flags are?

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Command Modifier Bits 11-8	Subscript 7-0	Configuration Response	Bit
0 0 0 0	1	Bit Significant Configuration of Drive and Format	Bit
		1 = Synchronized Spindles supported	15
		1 = High Speed Data Port (See 7.7.1.3)	14
		1 = Notched Drive with Equal Zones exc first/last	13
		1 = Notched Drive with Unequal Zone Sizes	12
		1 = Soft Sectored Notched Drive	11
		1 = Notched Drive Capable of Non-notched Operation	10
		Reserved	9 to 1
0 0 0 0	x	Values for Configuration of Drive and Format	
	8	Maximum Transfer Rate in Kilohertz (rounded)	
	9	Rotational Speed	
	10	Head Group Skew	
		Bits 15-8 Reserved	
		Bits 7-0 Head Group Skew	
	11	Drive Delays	
		Bits 15-8 Read Data Propagation Delay in bits	
		Bits 7-0 Write Data Delay in bits	
	12	Drive Delays	
		Bits 15-8 Reserved	
		Bits 7-0 Mark Detection Skew	
	13	Write Splice Information	
		Bits 15-8 READ GATE Window Size in bits (maximum)	
		Bits 7-0 Size of Write Splice in bits (maximum)	
	14	Notched Drive Zones Supported (See 7.18)	
		Bits 15-80 Reserved	
		Bits 7-0 Number of Zones (FF=Controller Definable)	
	15	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Tracks per Zone	
	16	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Address of First Track in Zone	
	17	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Format Information	
		If Subscript 1 Bit 11=1 Then bits 15-0 are Bytes/Track	
		If Subscript 1 Bit 11=0 Then bits 15-0 are Sectors/Track	

TABLE 7-11B MAGNETIC DISK GENERAL CONFIGURATION RESPONSE BITS

Comment: If the notched drive happened to have all equal zones, should bit 13 = 1? Several changes are suggested above. The reasons for the changes follow. It seems preferable to lump the values common to both notched and non-notched drives ahead of the notched values. Thus the movement to subscripts 11-13. There has been at least one presentation of the concept of having

different recording algorithms in the zones. Such a technique might use few zones of large size. Consequently it seems desirable to allow a larger number of tracks per zone (16 Bits). Since the most straightforward technique for notched drives uses soft sectoring, to me, it seems misleading to leave soft sectoring requirements out of the notched drive characteristics. I recognize that the soft sectoring information could be obtained from the 0100 command, but by the same token fixed sector information could be obtained by the 0110 command. Consequently, I suspect that having only the one method highlighted in the notched drive characteristics will send some implementations down a path which makes maintaining all of the performance advantages of notched drives more complex. An additional factor favoring the foregoing change is that some drives may very well support fixed sectoring in a non notched mode while only supporting soft sectoring in the notched mode.

Additional comment: As I have suggested before, it may be better to provide the capability to sequence directly through all zone characteristics without cycling through the Set Configuration Command. One method would be to use a different subscript for each zone. Perhaps there would be some objection to this as presently structured, since it would reduce the possible zones from 256 to 80 (or 82 if the missing subscripts 2 / were found). However the full number of zones could be recaptured, if that is desired, by devoting at least one full command modifier to notched drives. Maintaining the present structure, the full number of zones can be reported by repetitive Request Configuration commands with the 0000 modifier and the following slightly modified response:

Command Modifier Bits 11-8	Subscript 7-0	Configuration Response	Bit
0 0 0 0 0	1	Bit Significant Configuration of Drive and Format	
		1 = Synchronized Spindles supported	15
		1 = High Speed Data Port (See 7.7.1.3)	14
		1 = Notched Drive with Equal Zones exc first/last	13
		1 = Notched Drive with Unequal Zone Sizes	12
		1 = Soft Sectored Notched Drive	11
		1 = Notched Drive Capable of Non-notched operation	10
		Reserved	9 to 1
0 0 0 0 0	x	Values for Configuration of Drive and Format	
	8	Maximum Transfer Rate in Kilohertz (rounded)	
	9	Rotational Speed	
	10	Head Group Skew	
		Bits 15-8 Reserved	
		Bits 7-0 Head Group Skew	
	11	Drive Delays	
		Bits 15-8 Read Data Propagation Delay in bits	
		Bits 7-0 Write Data Delay in bits	
	12	Drive Delays	
		Bits 15-8 Reserved	
		Bits 7-0 Mark Detection Skew	
	13	Write Splice Information	
		Bits 15-8 READ GATE Window Size in bits (maximum)	
		Bits 7-0 Size of Write Splice in bits (maximum)	
	14	Notched Drive Zones Supported (See 7.18)	
		Bits 15-100 Reserved	
		If Bit 8=0 Then report is for first zone *	
		Bits 7-0 Number of Zones (FF=Controller Definable)	
		If Bit 8=1 Then report is for next zone	
		Bits 7-0 Number of Zone being reported	
		If Bit 9=0 Then report is for first or intermediate zone	
		If Bit 8=1 & Bit 9=1 Then report is for last zone	
		If Bit 8=0 & Bit 9=1 Then report is a sequence error	
	15	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Tracks per Zone	
	16	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Address of First Track in Zone	
	17	Notched Drive Characteristics (See 7.18)	
		Bits 15-0 Format Information	
		If Subscript 1 Bit 11=1 Then bits 15-0 are Bytes/Track	
		If Subscript 1 Bit 11=0 Then bits 15-0 are Sectors/Track	

* Note: It is the responsibility of the controller to sequence through groups of Subscript 14-17 until all zone characteristics are reported.

TABLE 7-11B MAGNETIC DISK GENERAL CONFIGURATION RESPONSE BITS

The time is measured from the end of the write splice to the end of the last bit where the controller may assert READ GATE and successfully achieve PLO Sync lock on the drive to assure a successful read operation. If no window is required by the drive, it shall set this value to zero, indicating to the controller that *the default value applies.* there is no window requirement.

IMPLEMENTOR'S NOTE: This value is intended to *achieve more accurate control of Read Gate to facilitate special clock acquisition techniques (i.e.* support drives which use PLO Sync fields that are split into a 'high frequency' section followed by a 'low frequency' section to speed PLO lock). Drives which do not require *the more accurate Read Gate* this feature shall set this value to zero to allow the controller to increase the PLO Sync size to meet its own needs. The only restriction which then applies is that READ GATE shall be asserted by the controller in sufficient time to guarantee the minimum number of PLO Sync bytes.

If this value is not returned by the drive, then the controller shall assume that the maximum write splice size is 3-7 bits. See also 8.2.3.

IMPLEMENTOR'S NOTE: This value measures the time from WRITE GATE assertion to when the drive's write channel is able to write valid data. It should not include any delays associated with getting WRITE DATA bits to the media.

If this value is not returned by the drive, the controller shall assume that the Write Data Delay is 0 bits. *See also 8.2.7.*

7.7.1.5.3 Mark Detection Skew

This value measures the time, in bits, that INDEX, SECTOR, or ADDRESS MARK FOUND may vary relative to data recorded on the media i.e. the maximum distance in bits between the earliest possible and the latest possible, detection of INDEX, SECTOR, or ADDRESS MARK FOUND.

This value is a measure of the distance that *one of these marks a* mark may move relative to a write splice between the write function and a subsequent read.

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7.7.1.6 Specific Configuration Response

If command modifier bits 0001-1111 are used, the specific configuration information shown in Table 7-12 is returned for each Request Configuration command with those modifiers.

Command Modifier Bits 11-8	Configuration Response	
0 0 0 1	Number of Cylinders - Fixed	(FIXCYL)
0 0 1 0	Number of Cylinders - Removable Media (0 if not)	(REMCYL)
0 0 1 1	Number of Heads	
	Bits 15-8 Removable Drive Heads	(REMHDS)
	Bits 7-0 Fixed Heads	(FIXHDS)
0 1 0 0	Minimum Unformatted Bytes per Track	
0 1 0 1	Minimum Unformatted Bytes per Sector (Hard Sector only)	
0 1 1 0	Number of Sectors per Track	
	Bits 15-8 Reserved	
	Bits 7-0 Sectors per Track	
0 1 1 1	Minimum Bytes in ISG Field (not inc InterSector Speed Tol)	
	Bits 15-8 ISG Bytes after Index/Sector Pulse to WSplice	
	Bits 7-0 Bytes per ISG	
1 0 0 0	Minimum Bytes per PLO Sync Field	
	Bits 15-8 Reserved	
	Bits 7-0 Bytes per PLO Sync Field required *after* when READ GATE is asserted	
1 0 0 1	Number of Words of Vendor Unique Status Available	
	Bits 15-8 *Number of Extended Status Words* Reserved	
	Bits 7-0 Number of Vendor Unique Status Words	
1 0 1 0 to 1 1 0 1	Reserved	
1 1 1 0	Seek Overhead Skew	
	Bits 15-8 Cylinder Switch Skew	
	Bits 7-0 Head Switch Skew	
1 1 1 1	Vendor Identification (Optional - See Table 7-17)	
	Vendor Id - Extended Information (See 7.7.4.2)	

Note: Removable heads map from 00 to (REMHDS-1)
Fixed heads map from REMHDS to (REMHDS+FIXHDS-1)
Removable cylinders map from 0000 to (REMCYL-1)
Fixed cylinders map from 0000 to (FIXCYL-1)

TABLE 7-12 MAGNETIC DISK SPECIFIC CONFIGURATION RESPONSE BITS

Example: A drive with 32 sectors/track spinning at 3,600 rpm with a 5 msec cylinder switch seek time, no overhead on head switch, and a skew value of 77 reported in bits 15-8 (60/3600*256=65.1 usecs per unit of skew and 5 msec/65.1 usecs =76.8). The controller uses this to allow an actual skew of 10 (77*32/256=9.6) sectors between cylinders excluding any

controller overhead.

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Command Modifier Bits 11-8	Configuration Response
0 0 0 1	Number of Tracks on Fixed Media (Erasable only)

Page 7-21

NOTE: Any manufacturer of ESDI products which are not listed above should contact the editor to have an Identification Code assigned.

Comment: The chair should work with the X3T9 chair to confirm a more lasting registration identity for this note.

Page 7-24

Disks which can modify gain and use other techniques to recover data shall interpret the modifiers in a drive specific manner. Disks which cannot provide such functions shall ignore this command.

Page 7-26

Soft Switch modifiers are also used to configure disk drives capable of handling variable frequency recording, sometimes referred to as MCAV (Modified Constant Angular Velocity) or as Notched drives. The disk may be divided into zones of recording frequency that support a different number of sectors per track. If a disk can adapt itself to any frequency it shall do so by reporting x'FF' in response to Request Configuration with Subscript 7414.

Comment: I still prefer a more directly visualized term such as one of the following: Zoned Bit Density (ZBD); Zoned Bit Recording (ZBR); Zone(d) Bit Density,Recording; or Zone(d) Sectoring.

Page 7-27

The controller may use Set Configuration with synchronized drives to set this(the selected) drive to act as master (7-0 = x'01') or as slave to another drive (7-0 = x'00').

Comment: Although I requested this function and understand how it would work, I am confused. Is x'01' an example of the switch settings that may be used or the required settings. Probably the wording for setting sector mode on page 7-28 is the reason I raise the question. This question would be eliminated by changing Table 7-29 to that shown below.

The controller may use Set Configuration to identify the zone to be worked with (the first zone is numbered as 1 and begins at cylinder 0).

Comment: Pages 7-27 and 7-28 will require some changes if the method for handling notched drives I suggested in prior sections is accepted. If the present method is maintained or is one of two alternate methods, some additional changes are required. Since the zone selection is a method of setting the drive/controller up, the fact that the drive responded as a non-notched drive when set to Zone 0 does not indicate what will happen if a subsequent non zero Zone is set. I recommend that a notched drive have a switch setting to set it to notched mode. When in notched mode, it should respond to a Zone 0 setting with a normal zoned response. When in a non-notched mode it should respond to a Zone 0 setting as a non-notched drive. However, it is conceivable that the total cylinders for the non-notched mode could be lower than in the notched mode. Since Zone 0 is preferable for the non-notched bit rate, it would be less disruptive to designate the first Zone as Zone 0 beginning at the Maximum cylinder. As pointed out in my letter of 5/10/87, a statement is needed that a format operation is required after zone conditions are altered in order for the change to be effective.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	P	CMD Function	Switch No	Switch Parameter
1	1	1	0	0	0	0	0											0000 to 0FFF	Vendor Unique
				0	x	x	x											1000 to 1FFF	Reserved
				1	0	0	0												
						to													
				1	0	1	0												
				1			1											1411	Set Drive Synchronized Mode
																			x'00'= Slave x'01' = Master
				1	1	0	0											1412	Set Notched Mode
																			x'01'= Notched x'00' = Not Notched
				1	1	0	1											1413	Notched Drive Zone Number
				1	1	1	0											1414	Notched Drive Tracks/Zone
				1	1	1	1											1415	Notched Drive Sectors/Track

Example: If a magnetic disk drive is capable of supporting soft or hard sector operation according to the setting of Dipswitch 1 then the configuration would be described as follows:

1	1	1	0	0	0	0	1	1411	xxxx xx01 = Set Soft Sector
									xxxx xx10 = Set Hard Sector

TABLE 7-29 SET CONFIGURATION SOFT SWITCH PARAMETER BITS

Page 8-1

o trailing edge of ADDRESS MARK ENABLE during hard sector format (as defined in Figure 8-14) or soft sector format.

Comment: Isn't Figure 10-8 a better reference? In addition the document, as did the defacto version, uses both "hard sector" and "fixed sector" as the term to describe the opposite of "soft sector". I suggest only one be used. Although dealer's choice is acceptable, there is logic to "hard sector" as the antithesis and to avoid any "fixed disk" connotation.

Page 8-2

Assuming head selection is stabilized, the time lapse from negating READ GATE to asserting WRITE GATE shall be five REFERENCE CLOCK periods minimum.

Comment: It seems safer to plan for 24 MBits/sec operation by maintaining the time called out by SMDE ANSI standard which is the same as this requirement at 10 MBits/sec. This could either be done by changing to a minimum of 500 nanoseconds or by adding a high speed port requirement. "Assuming head selection is stabilized, the time lapse from negating READ GATE to asserting WRITE GATE shall be five REFERENCE CLOCK periods minimum for drives with a Subscript 0 Configuration Response of bits 8 or 9 (=10 MHz) =, shall be twelve REFERENCE CLOCK periods minimum for drives with a Subscript 0 Configuration Response of Bit 10 = 1 (=10 MHz). If the controller requests maximum transfer rate, this value may be adjusted to any number of bits with a minimum time of 500 nanoseconds."

WRITE GATE shall not be asserted until 15 usec after a head change *and* or COMMAND COMPLETE is asserted.

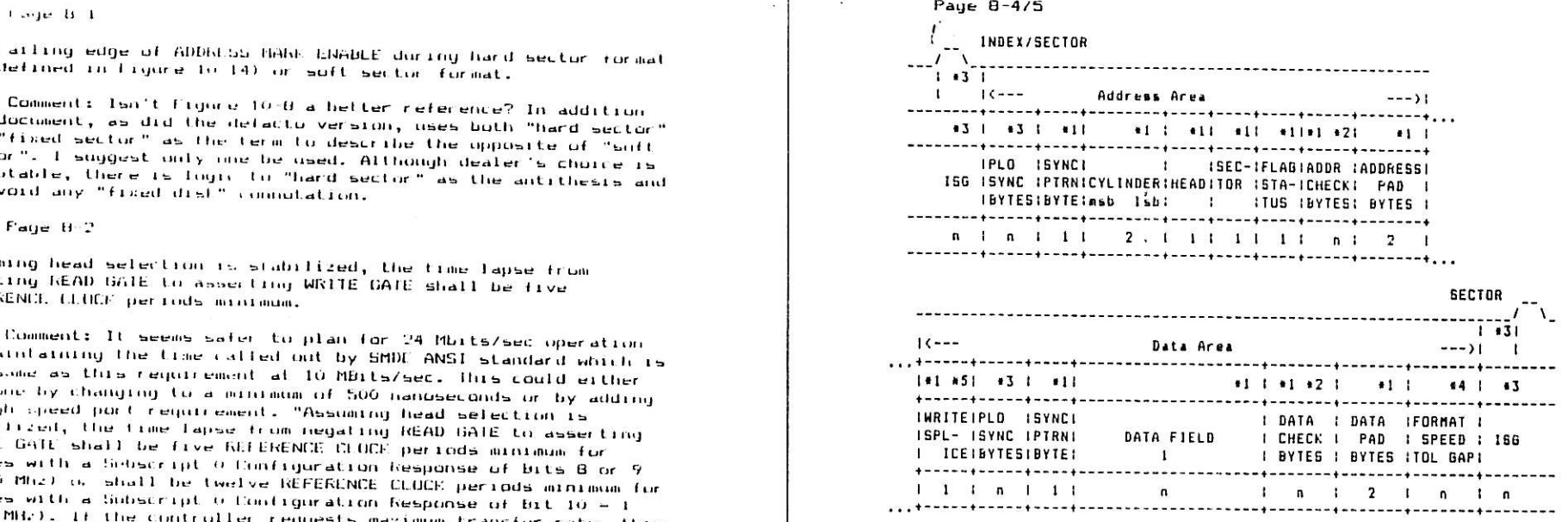
Write data received at the I/O connector ~~may shall~~ be delayed by the write data encoder by up to 8 bit times maximum *or as reported in Subscript 11 of the Values for Configuration of Drive and Format Response* prior to being recorded on the media.

Comment: The subscript was 15 prior to my suggested change.

Page 8-3

The recorded format on the disk is under control of the controller. The INDEX and SECTOR pulses are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed data records is shown in Figure 8-1.

Page 8-4/5



#1 These areas are examples only, and may be structured to suit individual customer requirements
#2 The number of check bytes is controller-defined.
#3 Established by device and reported in response to Request Configuration Commands.
#4 Format Speed tolerance gap is required if REFERENCE CLOCK is not tied to rotational speed. The applicability of this gap is defined in the Configuration data.
#5 *Values for areas may be altered by Configuration Response data.*

NOTE: All byte numbers indicated are minimums.

FIGURE 8-1 FIXED SECTOR FORMAT

a) Drive required write-to-read recovery time (the minimum time between negation of WRITE GATE and assertion of READ GATE or ADDRESS MARK ENABLE which is specified in the "ISG Bytes after Index/Sector" in Configuration Data Response.

b) Other drive required ISG times.

c) Variations in detecting INDEX and SECTOR.

d) Controller decision time between sectors.

all but the last are used by the *drive* manufacturer as the basis of determining the "Bytes per ISG" specified in the Configuration Data Response.

An appropriate error-detection mechanism is generated by the controller and applied to the address for data integrity purposes. These codes are written on the media during formatting. Data integrity is maintained by the controller recalculating and verifying the address field check codes when the ID is read. ADR check bytes are *controller* user defined.

8.3.4.1 Write Splice

This area is required by the drive to allow time for the write drivers to turn on and reach recording amplitude sufficient to ensure data recovery. This area shall be allowed for in the format and the controller shall send zeros during this time. The resulting splice *is a maximum of one byte or as reported by Subscript 13 of the Values for Configuration of Drive and Format Response.* from a minimum 2 bit pulse shall be at most one byte long.

8.3.4.5 Data Check Bytes

The Data Check bytes, commonly referred to as ECC (Error Check Code or Error Correction Code), are generated by the controller and written on the media at the end of the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Check Bytes or applying error correction algorithms if applicable after the Data Field is read. The Data Check Field is *controller* user defined.

8.3.4.6 Data Field Pad

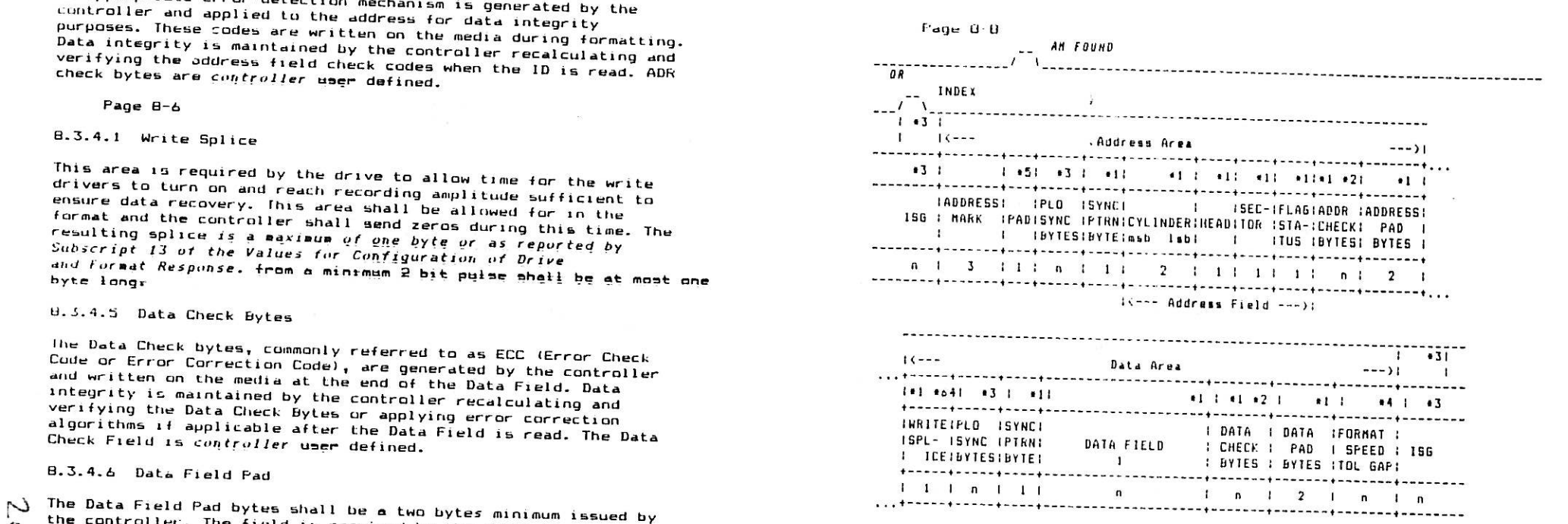
The Data Field Pad bytes shall be a two bytes minimum issued by the controller. The field is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes. The controller shall send zeros during these byte times.

This gap, if required, shall be between each sector. The byte pattern in this gap shall be zeros.

Note: The controller must account for this gap, if required, in sector format calculations. However, with worse case conditions the actual recorded gap may be truncated to zero bytes by the next SECTOR or INDEX pulse.

8.3.6 Fixed Sector PLO Sync Format Timing

The purpose of the format is to organize a data track into smaller sequentially numbered blocks of data called sectors.



#1 These areas are examples only, and may be structured to suit individual customer requirements
#2 The number of check bytes is user-defined.
#3 Established by device and reported in response to Request Configuration Commands.
#4 Format Speed tolerance gap is required if REFERENCE CLOCK is not tied to rotational speed. The applicability of this gap is defined in the Configuration data.
#5 This is part of the PLO Sync Field to allow for READ GATE assertion delays. The controller should treat this as an additional byte in the PLO SYNC field.
#6 *Values for areas may be altered by Configuration Response data.*

NOTE: All byte numbers indicated are minimums.

FIGURE 8-2 SOFT SECTORED FORMAT

Page 8-9

8.4. Address Mark Pad

The Address Mark Pad byte follows the Address Mark field and is to be considered as an additional byte in the FLO Sync field. It's purpose is to allow for READ GATE assertion delays after detecting the ADDRESS MARK FOUND signal. *When writing, the controller shall send zeros during this byte.*

Page 8-11

8.6.6 Head Switching Time

WRITE GATE shall be negated at least 1 us before a head change to switch to the other surface. WRITE GATE may not be asserted until 15 us after a head change *and until* or COMMAND COMPLETE is asserted.

8.7.1 Format Rules

The recorded format on the disk is not always *entirely* necessarily under control of the controller. *In some cases it* may *be* but is either pre-formatted by the media supplier or under control of the drive. There is more than one method for manufacturers to pre-format disks. The INDEX and SECTOR pulses are available for use by the controller to indicate the beginning of a track and sector zero, and the beginning of sectors other than zero respectively.

Page 8-12

8.7.3.2 Sync Pattern Byte(s)

This field establishes byte Synchronization (i.e. the ability to partition the is ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the controller the beginning of the address field information. It is recommended that the Sync Pattern Byte(s) contain more than a single one bit for a greater confidence level of detection.

The drive may synthesize a Sync Pattern. and If *the Sync Pattern is not detected* it fails to be presented on the first attempt to read a sector, the drive is responsible to recover *with a synthesized Sync Pattern* on the next revolution. *On the failing revolution, the SECTOR pulse may also be missing preceding the missing Sync Pattern.* The sector pulse preceding a Sync Pattern may or may not have been presented under the circumstances when a drive fails to present Sync Pattern.

8.7.3.3 Address Field

These bytes are *controller* user- defined and interpreted. by the user's controller.

Page 8-13

8.7.3.5 Sector Write Status

If the media has been certified by the manufacturer this field contains zeros to indicate the sector has been certified as usable by the manufacturer. If this byte contains any ones, then the sector cannot be recorded because it has been flagged as defective by the manufacturer.

The controller may choose to ignore this field, and consider it part of the gap but it it possible that the drive will abort any attempted write operations if the byte contains any ones.

Comment: That doesn't sound like a good choice! Is it intended to not offer any hint where some of these fields are located?

Page 8-14

8.7.4.4 Data Field

The data field contains *information for the host system's* data files. A data field may be constructed from segments which contain data (in multiples of 128 bytes) and its associated Error Correction Code (in multiples of 8 bytes). NOTE: The multiples need not be the same value. By using segments to construct large data fields, a simple and straightforward encoder/syndrome calculator can be used instead of having to use the type of more complex ECC needed to handle large fields of contiguous data.

Comment: Is it intended that ROM not be allowed to use ESDI?

Page 8-15

8.7.6.5 Post Field Check Codes

The Post Field Check Code bytes are generated by the controller and written on the media at the end of the Post Field. Data integrity is maintained by the controller recalculating and verifying the Post Field Check codes or applying Error Correction algorithms, if applicable when the Post Field is read. The Post Check field is *controller* user defined.

Page 9-1

For normal command operation, none of the status or configuration data responses need be transferred *again*. This simple interface operation should be easily implemented by both drive and controller manufacturers. The recommended "Fault/Abnormal" condition handling procedure is provided to increase the compatibility between drive and controller manufacturers. None of the recommended procedures violate or take exception to *other parts of* this standard.

9.2 HANDLING COMMAND TRANSFER ERRORS

The intent of this section is to define orderly detection, termination and resynchronization techniques for errors (or faults) which occur as a result of communication of Command and Configuration/Status data. Both the drive actions and the controller actions are defined.

The orderly detection, termination and resynchronization techniques for these faults are covered in Section 9.2.2.

9.2.1.2 Parity Error

This occurs when either the drive or the controller detects a parity error on appropriate Command or Configuration/Status data. This fault is detected after the a complete 17 bits of Command or Configuration/ Status data has been transferred. This type of fault may occur with or without ATTENTION previously asserted.

Figure 10-24 and Figure 10-25 define the interface protocol for either a Parity Error, Invalid Command or Unimplemented Command fault with ATTENTION previously negated and ATTENTION previously asserted *respectively*. In Figure 10-24 and Figure 10-25, the error occurred on a command sent by the controller which would result in status or configuration data being sent back by the drive. Thus, the controller is expecting to assert TRANSFER REQ for the first bit of Configuration/Status data after sending the parity bit of the command data.

In Figure 10-25, ATTENTION was previously asserted and cannot be used to inhibit the TRANSFER REQ for the first bit of Configuration/Status data (or terminate this TRANSFER REQ). For the case shown in Figure 10-25, the key assumption made by the drive is that the controller will assert TRANSFER REQ for the first bit of Configuration/Status data within 10 msec after the trailing edge of the TRANSFER ACK for the parity bit of the Command.

If the Controller has not requested the first bit of Configuration/Status data within this 10 msec time out, the drive shall assert COMMAND COMPLETE. If the controller asserts TRANSFER REQ for the first bit of Configuration/Status data within this 10 msec, the drive shall create an Interface Fault to the Controller which will then signify that resynchronization is to occur. (The drive should also not respond to any subsequent TRANSFER REQS which occur within 10 msec of the last TRANSFER REQ for this sequence due to the 10 msec timeout denoted by note #4 in Figure 10-25).

If a communication fault, as defined by Figure 10-24 or 10-25, occurred on a command which did not expect status or configuration data to be transferred back to the controller, the controller should not issue a TRANSFER REQ for the first bit of Configuration/Status data. For these Communication fault conditions, the notes and timing of Figure 10-24 and Figure 10-25 are applicable except that TRANSFER REQ shall not be asserted by the controller for the first bit of Configuration/Status data as defined *by note* at #3 in Figure 10-24 and 10-25.

e) *The controller and drive should assume that* all combinations *depicted in* of Figure 10-26 *can occur and should be accounted for.*

9.3.1.6 Bit 10: Transfer Rate > 10 MHz

If Bit 10 is a 1, the *clock rate for the* disk drive NRZ Data Transfer Rate is greater than 10 MHz. Per *this current standard* **the current specification**, the rate is > 10 MHz and <15 MHz. Otherwise, Bit 10 is a zero. If this bit is a 1, the controller should be capable of operating with up to at least a 15 MHz Data Rate.

Comment: Some portions of the standard have the upper limit at 24 Mhz. If possible, it would be preferable to use 24.

9.3.1.7 Bit 9: Transfer Rate >5 MHz, <=10 MHz

If Bit 9 is a 1, *clock rate for the* disk drive NRZ Data Transfer Rate is greater than 5 MHz but less than or equal to 10 MHz. Otherwise, Bit 9 is a zero. If this bit is a 1, the controller should be capable of operating with up to at least a 10 MHz Data Transfer Rate.

9.3.1.8 Bit 8: Transfer rate <5 MHz

If Bit 8 is a 1, the *clock rate for the* disk drive NRZ Data Transfer Rate is equal to or less than 5 MHz. Otherwise, Bit 8 is a zero. If this bit is a one, the controller should be capable of operating with up to at least a 5 MHz data transfer rate.

9.3.1.13 Bit 3: Not MFM

If Bit 3 is a 1, then the drive does not employ an MFM encoding method to write data on the media. If Bit 3 is a 0, an MFM encoding method is used. This bit state may be used by controllers to *help* select Disk Data Error correction methods (The utilization of encoding other than MFM may result in larger

data error burst lengths). If this bit is a 1 the controller shall ensure that the start of a PLO sync field is defined.

9.5.1.16 Bit 0: Reserved

This bit shall always be set to zero.

Comment: This one reserved bit should not be singled out. If the requirements of Section 7.2 (0) do not apply to responses (and literally they probably do not), the first paragraph of 7.2 should be expanded to cover responses and moved to 7. (0). As you will note, I have not systematically dealt with this issue. However the document should be revised to state each and every reserved case or rely entirely on a blanket statement.

Page 9-10

9.4.1 General Error Recovery Philosophy

As indicated in Figure 10-18, Figure 10-19 and Figure 10-26, the normal procedure to recover from a fault condition detected by the drive (indicated by ATTENTION being asserted), is for the controller to first issue a Request Status Command, read the Standard Status response, *and in some cases the Extended Standard Status*, and then issue a Reset Attention Command to reset the fault condition in the drive.

The general philosophy is that a drive should recover from a fault state by attempting recovery techniques when the Reset Attention Command is received (i.e. the drive shall attempt to become operational if possible). In some cases, depending on the status bits which were set, additional recovery commands may be required *from* by the controller (e.g. a command to eliminate a track offset condition, turn on the spindle motor). In addition, the drive should utilize an asserted ATTENTION line to inhibit reads or writes if an internal fault condition exists.

Once the controller has determined that a fault condition exists (i.e. ATTENTION *and COMMAND COMPLETE* asserted) the controller should terminate the current operation and properly read and reset the Standard Status. After receiving a valid Standard Status response the controller may then proceed to decode the status bits and perform error recovery based on *the* status bits set.

If the controller cannot recover from the fault detected after three retries, the controller should proceed by reading *Standard Status, Extended Standard Status, and* Vendor Unique Status (if available) and reporting this status to the system. When reading Vendor Unique Status, the controller should read all available responses, as specified in configuration data, in sequence starting with the first location.

Table 9-2 *shows* reveals that no command transfer may be initiated by the controller if either TRANSFER REQ or TRANSFER ACK is asserted, or if COMMAND COMPLETE is negated.

Page 9-11

Table 9-2 also *shows* reveals that the READY line is utilized to indicate that the spindle motor is up to speed. The READY line being negated does not necessarily indicate a fault condition in the drive. For example, the spindle may have been stopped by a previous command.

Page 9-12

9.5 STANDARD STATUS

Standard Status bits 15-12 are status bits which do not cause ATTENTION to be asserted when set. The controller should check these bits as a potential reason for a fault being set by the drive in response to a controller attempted operation or invalid read data.

Standard status bits 11-0 *if* are set to 1 and cause ATTENTION to be asserted to advise when a fault condition or change of status occurs that the controller may not be aware of.

Comment: It is not clear what portions of Section 9 apply to optical. Certainly this section does not.

Page 9-14

9.5.1.12 Bit 4: Seek Fault

This bit should be set for any reason the drive suspects that a seek function has not been executed properly. If this bit is set, the controller should reset Standard Status, perform a *Recalibrate* and reissue the Seek command a minimum of three times prior to defining that the drive may require operator intervention. This bit is intended to indicate that a transient (or potentially solid) problem exists with the drive positioning system. This bit should not be set for an invalid seek address received from the controller.

9.5.1.14 Bit 2: Vendor Unique Status Available

This bit should be set by the drive to indicate that vendor unique status is now valid. The controller is not required to read this vendor unique status. Vendor Unique Status is only intended to be utilized by trained field maintenance personnel and is not intended to be interpreted by disk controllers or operating systems. The Vendor Unique Status responses should be read by the Controller and sent back to the system for *maintenance purposes as appropriate in the specific application.* a print out of these codes which may then be utilized by the field maintenance personnel.

In Table 9-3, numbers enclosed in circles denote the order in

which the indicated recovery command should be issued. In Table [illegible] numbers identified by asterisks are notes and not associated with the order in which recovery commands are issued. The Standard Status Bits 12, 13 and 14 indicate conditions in the drive that are probably not changeable via the command interface to the drive and manual intervention likely to be is required. The order in which the recovery commands are issued is straight forward. The Initiate Diagnostics Command should not be utilized until the controller has attempted the indicated recovery command sequences at least three times and has failed to correct the fault indicated.

Comment: With the addition of the Set Configuration command, there could be implementations that could recover from Bits 12 and 13 over the interface. Whether they should is another question.

Page 9-16/17/18

Comment: The condition designators I, II, and III need to be added back into Tables 9-3A&B and 9-4.

The drive need not implement special logic to detect the deselection of a drive prior to completion of a Command or Configuration/Status transfer. The defined communication fault protocol resynchronization features should detect this condition if the drive is adversely affected.

Page 10-1

tBT - Bit Time

10.3 TERMS

The interface uses a mixture of open collector TTL signals for control and differential signals for data. The terms asserted and negated are used for consistency and to be independent of electrical characteristics.

Asserted - the negative logic signal is true (=0)
- the differential signal is positive (=1)

Negated - the negative logic signal is false (=1)
- the differential signal is negative (=0)

All signals are shown with the Asserted condition towards the top of the page. The Negated condition is shown towards the bottom of the page relative to the Asserted condition.

Page 10-4

Comment: Based upon the ANSI SMDE standard I assume 42 nanoseconds is not long enough for the leading edge of write gate to address Mark Enable. Therefore I request that at least 100 nanoseconds be reinstated as the minimum tA in Figure 10-3. It may be that a larger value such as the Write Splice width should be used. I am assuming these small values have never been used reliably. The artwork in the recommended soft sector format of the defacto standard implies Write Gate is raised at the leading edge of Index and Address Mark Enable at the trailing edge. If someone implemented this way they could have had a 500 nanoseconds minimum time. However the standard calls out that the write delay to recording can be up to 7 bits and the write splice width of up to a byte(and now as subscripted values) for a total of 15 bits which is greater than 500 nanoseconds for Reference Clock Rates under 30 MHz. A extenuating factor is that some popular controller chips, for a format operation turn on Write Gate with the leading edge of INDEX with considerable delay and then turn it off at the next leading edge of INDEX with even more delay. The net effect of this, with the present minimum would be for write turn on to reduce the detection margin of the Address Mark and then for the controller turn off of Write gate to further erode it with the turn off splice. For reliable Address Marks, my judgment is that the minimum tA should be at least 2 Byte times.

Comment: In Figure 10-4 Drive Select 2(0-3) should be shown valid before the second asserted Drive Selected.

Page 10-5

Comment: I think the second group of 16 bits should be changed to "Response Bits". Wouldn't it be less misleading to show some asymmetry in the timing especially between the transition from controller output to drive output? Given the space available, Figure 10-5 may need to be split into two figures. For *5, wouldn't it be more typical to show the command error occurring after the command and before the status? (I recognize that the defacto version also showed it after status.) This seems to be a figure that would benefit from a hand drawing or perhaps a CAD package. We need to sort out the timing tradeoffs between flagging a command error and the requirements for Section 6.3.5 paragraph 2.

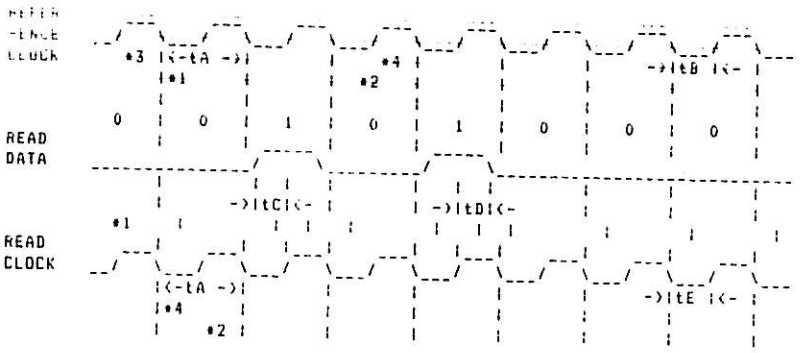
Page 10-6

Comment: With sector slewing, a controller should be free to have the first sector be other than 0. Therefore "sector 0" should be changed to "first sector".

Page 10-6

Comment: The value for tC is missing. It should be 16 bits minus tZ maximum *2. Add a note "* 2 If a subscripted value is used, that value minus tZ is the maximum for tC." The intention of the media content at the controller end of the cable is not clear. I think it should be deleted. The relation between the unnumbered note and tZ is not clear. What is the reason for this latter note?

(drive connector)



Label	Min.	Max.	Units	Label		Min.	Max.	Units
tA	0.900	1.100	T	tC	(Set Up Time)	14	-	nsec
tB	0.425	0.575	T	tD	(Hold Time)	14	-	nsec
				tE		0.425	0.575	T

*1 All times are measured in fractions of the clock period. T is the nominal period of the clock signals and is the inverse of the REFERENCE or READ CLOCK frequency.

*2 Phase relationship between REFERENCE CLOCK and NRZ WRITE DATA or WRITE CLOCK is not defined.

*3 REFERENCE CLOCK is valid when READ GATE is inactive; READ CLOCK is valid when READY is asserted.

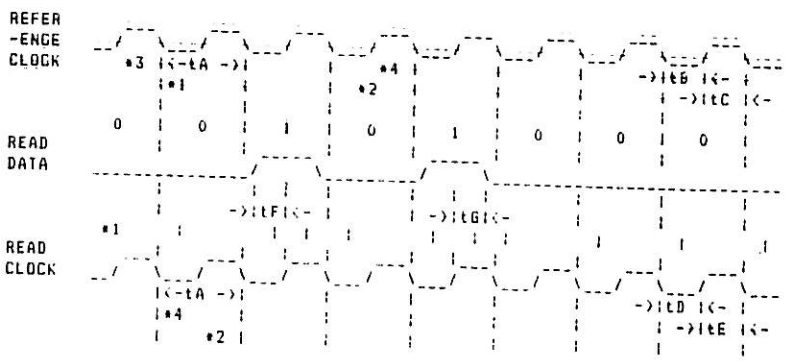
*4 Similar period symmetry shall be +/- 4 nsecs between any two adjacent cycles during reading or writing.

NOTE: When operating at 10 MHz the following values shall be used:
tE = 50 +/- 7.5 nsec
When operating at 15 MHz the following values shall be used:
tE = 33.3 +/- 5 nsec
The leading edge of the clock pulses is the controlled edge and should be used for data latching.

FIGURE 10-9 LOW SPEED PORT (0-15Mhz) DISK NRZ READ DATA TIMINGS

Comment: The text breaks at 10 Mhz and the timing diagrams break at 15 Mhz. Looks like we need to re-group or add an explanation.

(All signals are measured at the drive connector)



Label	Min.	Max.	Units	Label		Min.	Max.	Units
tA	0.950	1.050	T	tD		0.408	0.592	T
tB	0.408	-	T	tE		0.450	0.550	T
tC	0.592	-	T	tF	(Set Up Time)	5	-	nsec
				tG	(Hold Time)	5	-	nsec

*1 Some times are measured in fractions of the clock period. T is the nominal period of the clock signals and is the inverse of the REFERENCE or READ CLOCK frequency.

*2 Phase relationship between REFERENCE CLOCK and NRZ WRITE DATA or WRITE CLOCK is not defined.

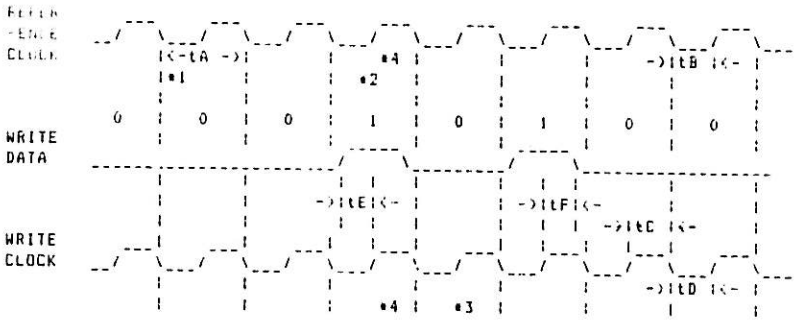
*3 REFERENCE CLOCK is valid when READ GATE is inactive. READ CLOCK is valid when READY is asserted.

*4 Similar period symmetry shall be +/- 2 nsecs between any two adjacent cycles during reading or writing.

NOTE: When operating at 15 MHz the following values shall be used:
tD = 33.3 +/- 6.1 nsec
When operating at 24 MHz the following values shall be used:
tD = 20.8 +/- 3.8 nsec
The leading edge of the clock pulses is the controlled edge and should be used for data latching.

FIGURE 10-10 HIGH SPEED PORT (10-24Mhz) DISK NRZ READ DATA TIMINGS

(Drive connector)



Label	Min.	Max.	Units	Label		Min.	Max.	Units
tA	0.900	1.100	T	tD		0.210	0.790	T
tB	0.425	0.575	T	tE	(Set Up Time)	*4*	-	nsec
tC	0.210	0.790	T	tF	(Hold Time)	*4*	-	nsec

*1 All times are measured in fractions of the clock period. T is the nominal period of the clock signals and is the inverse of the REFERENCE or READ CLOCK frequency.

*2 Phase relationship between REFERENCE CLOCK and NRZ WRITE DATA or WRITE CLOCK is not defined.

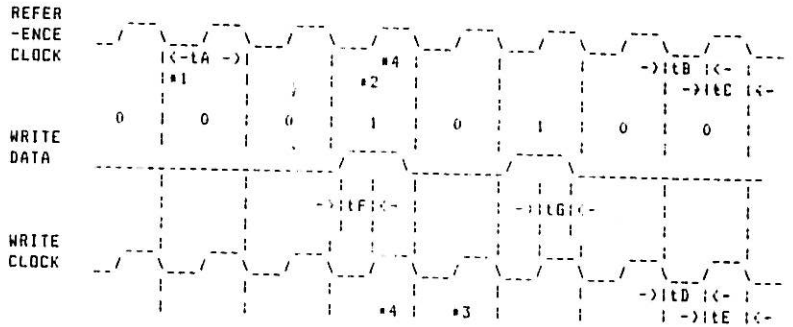
*3 The WRITE CLOCK shall be the same frequency as the drive supplied REFERENCE CLOCK (i.e. the WRITE CLOCK is the controller received and retransmitted DRIVE REFERENCE CLOCK).

*4 Similar period symmetry shall be +/- 4 nsecs between any two adjacent cycles during reading or writing.

NOTE: When operating at 10 MHz the following values shall be used:
tB = 50 +/- 7.5 nsec tD = 50 +/- 29 nsec
When operating at 15 MHz the following values shall be used:
tB = 33.3 +/- 5 nsec tD = 33.3 +/- 19 nsec
The leading edge of the clock pulses is the controlled edge and should be used for data latching.

FIGURE 10-11 LOW SPEED PORT (0-15MHZ) DISK NRZ WRITE DATA TIMINGS

(REFERENCE CLOCK is measured at the drive connector;
WRITE DATA and WRITE CLOCK are measured at the controller connector)



Label	Min.	Max.	Units	Label		Min.	Max.	Units
tA	0.950	1.050	T	tD		0.312	0.688	T
tB	0.408	0.592	T	tE		0.688	-	T
tC	0.692	-	T	tF	(Set Up Time)	5.0	-	nsec
				tG	(Hold Time)	5.0	-	nsec

*1 Some times are measured in fractions of the clock period. T is the nominal period of the clock signals and is the inverse of the REFERENCE or READ CLOCK frequency.

*2 Phase relationship between REFERENCE CLOCK and NRZ WRITE DATA or WRITE CLOCK is not defined.

*3 The WRITE CLOCK shall be the same frequency as the drive supplied REFERENCE CLOCK (i.e. the WRITE CLOCK is the controller received and retransmitted DRIVE REFERENCE CLOCK.)

*4 Similar period symmetry shall be +/- 2 nsecs between any two adjacent cycles during reading or writing.

NOTE: When operating at 15 MHz the following values shall be used:
tB = 33.3 +/- 6.1 nsec tD = 33.3 +/- 12.5 nsec
When operating at 24 MHz the following values shall be used:
tB = 20.8 +/- 3.8 nsec tD = 20.8 +/- 7.8 nsec
The leading edge of the clock pulses is the controlled edge and should be used for data latching.

FIGURE 10-12 HIGH SPEED PORT (10-24MHZ) DISK NRZ WRITE DATA TIMINGS

Page 10-12

Comment: Isn't Figure 10-12 too generic for Optical? If the reference to High Speed Port makes this figure applicable to disk, the 15 periods without a clock pulse violates the ESDI requirements for disk and I think for optical.

Page 10-14

Comment: Why is alternative 2 required for the high speed port?

Page 10-15

Comment: In Figure 10-16 there should be no implied coincidence between the trailing edge of INDEX and the leading edge of ADDRESS MARK ENABLE. What is not required on disks implemented with a high speed port?

Page 10-16

Comment: The timing relationship of ATTENTION and COMMAND COMPLETE needs to be further addressed. Figure 10-18 may be impacted. Figure 10-19 needs the RA definition included.

Page 10-23

Comment: It appears that ATTENTION is drawn in the wrong state in Figure 10-23. Note 2 should be "TRANSFER ACK is negated."

Page 10-20

Comment: Change note 4 to read "With TRANSFER ACK negated and ATTENTION asserted, Drive asserts COMMAND COMPLETE after TRANSFER REQ has been negated continuously for 10 msecs."

Page 10-21

Comment: The sub note to note 2 should be expanded as follows "Controller should issue a Request Status Command following the protocol outlined in 9.2.3. This will result in Request Status at least three times." Why and what procedure should the controller perform 3 times? The sub note to note 7 should be modified as follows "If ATTENTION is not negated, the Controller should ...".

Page 10-22

Comment: I don't see the usefulness of Figure 10-27. If it is needed, note 2 should be changed to "Request Status and Reset Attention".

Page App-1

The defect list shall resides on Sector 0 of the maximum cylinder and is be repeated on two other cylinders; maximum cylinder minus 8 and cylinder 4095 (x'FFF'). This allows for redundancy should an error occur on the maximum cylinder.

Comment: Why so many? The likelihood of having a broke I/O accessing either x'000' or x'FFF' seems higher to me than other addresses. In my view it should be the responsibility of the controller to subtract 3 cylinders from the user address space for defect logs and other housekeeping information. Therefore all cylinders which are used to store data for access by the controller should be accessible to the controller by normal means. (I thought I knew what triggered the request for a third flaw map. If it did, the message got garbled because this implementation in no way matches what they wanted.)

Some All ESDI disks shall ship with copies of the defect list on three cylinders. The cylinder at the address of 4095 is a drive-unique location. It may be located anywhere on the drive that the manufacturer chooses.

Comment: Even in a data area?

The manufacturer *should* shall guarantee that *at least one defect list* either maximum cylinder or the cylinder at 4095 is error free.

Page App-2

Only one size of Defect List shall be recorded per drive and must be the minimum sector size which will contain the locations of the maximum number of defects allowed per surface track.

	←---			Data Area			---→	
	WRITE SPL-ICE	PLO SYNC BYTES	SYNC PTRN BYTE	DEFECT LIST	DATA CHECK BYTES	DATA PAD BYTES		ISG
Hex	00	00	FE	*5	*4	00		00
Size	1	*2	1	256	2	2		n

*1 Drives with a High Speed Port require that a write splice be formatted at the start of the PLO Sync field.
*2 PLO Sync Field and ISG are as reported in response to Request Configuration commands.
*3 Cylinder = Maximum Cylinder or (Maximum Cylinder minus 8) or 4095
Head = 0, 1, etc. Sector = 0 Flag = x'00' or x'01'
*4 X(16) + X(12) + X(5) + 1
*5

	Date	Defect Location	Defect Location	Defect Location	//	Defect Location	Defect Location
Field	MDYHPP	CCBBL	CCBBL	CCBBL	//	CCBBL	CCBBL
Size	6	5	5	5	//	5	5

The Date consists of six one-byte fields:
M=Month: x'01-0C' D=Day: x'01-1F' Y=Year: x'52-xx'
H=Head: x'00-xx' P=Pad: x'00' P=Pad: x'00'
The Defect Location consists of three fields:
CC = MSB and LSB of cylinder address.
BB = MSB and LSB of byte count from index.
L = Length of error in bits (NOTE: resolution is within 7 bit cells of start of the flaw)
NOTE: The manufacturer may choose to pad the PLO Sync area by up to four bytes beyond those reported in Configuration Data.

FIGURE A-1 DEFECT LIST FORMAT

Page App-5

If the Header Address identifies that the sector is defective then its address *is* shall be listed in the Flaw Map and an alternate sector allocated. It is recommended that the alternate sector area be allocated in close proximity to the Flaw Map so that seeking to the Flaw Map will place the controller only a short seek away from the requested sector.

Page App-6

The controller shall begins reading at the first sector in the Flaw Map following the entries for factory identified defects. When the first non-recorded sector is read, then the address of the defective sector and its assigned alternate is used by the controller to write the data in the alternate sector.

Page App-7

Magnetic disks have a much lower defect rate, and it is practical to retire all sectors which contain a defect. The ECC is used *for error detection and* as an error recovery method for occasional errors and *error correction* is not *the primary* a strategy for data integrity.

Page App-8

For magnetic media, *at current bit densities*, the ECC is typically used to handle errors that result from "grown defects" (i.e. latent defects not identified in the factory scan or field certification). Automatic reallocation of affected sectors is one strategy that a controller may adopt.

It is *sometimes* possible to monitor the error correction thresholds and pass flags to the user on marginal sectors before data becomes uncorrectable. One flag would request that a particular sector be retired, while another would request that the entire piece of media be retired. Obviously, this type of defect prognosis is effective only if the media is read periodically.

Page App-9

Another approach would be to put the controller in a special diagnostic mode where write is inhibited. The controller is in a write mode for accepting data, but is in a read mode for ECC processing, thus supplying to the ECC circuits a data record plus redundancy bytes which contains known error conditions. Correct syndrome generation can then be verified.

Comment: Will IPI and SCSI support this approach?

Page App-10

Correction times must be considered when selecting a processor and buffer strategy. *For* In many *some* cases, three or more buffer *would* will be required.

C.4.1 SINGLE BUFFER STRATEGY WITH SECTOR INTERLEAVING

Upon processing a sector in the buffer and finding it bad despite retry procedures, the processor can reread the sector using the erasure read command. This will place the erasure pointer information into the buffer for use in the EDAC algorithm.

Comment: This command does not seem to exist.

* Write splice to be a minimum of 8 bits
** Controller shall reinitializes timing with each sector pulse

FIGURE D-2 FIXED SECTOR OPTICAL DISK TIMING

D.2 OPTIMEM FORMAT

Comment: The format is missing. If it is included do we need to indemnify ourselves for legal action resulting from favoritism? Will there be a method provided for various marketeers to add an appendix for their favorite companies format? Or when it shows up will we think it is widely applicable and give it a generic title?

When the transmission line attenuates the high frequency signal, the rise and fall rate of the signal at the receiving end are reduced. This increase in rise and fall time at the input of the receiver will result in placing the input in an undetermined state for an extended period. Since noise from other sources can cause perturbations on the input signals, jitter at the output of the receiver can result. The signals will appear as variable width pulses at the output of the receiver.

Comment: There is some very useful material in the transmission line appendices. Perhaps an observation should be added that the signal rise time can impact the shielding and grounding requirements to comply with certain EMI standards.

It is essential that the driver and receiver *as well as any board mounted terminators* be located close to the edge of the PCB (printed circuit board) to reduce the mismatch between the board and the transmission line, and to minimize reflections and hence distortion, if as the board is not matched to the line. Variations in the length of the board metallization can affect delays, and efforts should be made to maintain equal lengths. This delay introduced by the PCB is approximately 0.15 nsec/inch of metallization.

The 41LG Line Driver and 41LF Line Receiver are high speed parts suitable for use in the high speed data port. Optimum operation of these circuits requires proper termination of the transmission line or twisted pair. The 41LG is typically a 25 ohm line driver and is specified at 50 ohms.

Comment: The last sentence is not clear, at least in the [illegible] context.

The skew of the 41LG line driver is typically less than 0.5 nsec and *should* guaranteed to be less than 1 nsec. The variation in skew between two identical paths in the same package is typically less than 0.2 nsec. The 41LG line driver and 41LF line receiver in combination have been shown to have less than 20% distortion of the output wave shape of the 41LF line receiver when operating with transmission lines up to 12 meters at 25 MHz as shown in Figure E-1.

Comment: 20% of what?

o With a test load of 2 resistors, 50 Ohms each, connected in series between the driver output terminals, the magnitude of the differential voltage (VI) measured between the two output terminals *should* shall be equal to or greater than 2V, or 50% of the magnitude of VO, whichever is greater. For the opposite binary state the polarity of VI is reversed (VI).

o During transitions of the driver output between alternating binary states, the differential voltage measured across 100 Ohm load *should* shall monotonically change between 0.1 and 0.9 of VSS less than 0.1 of the unit interval or 20ns, whichever is greater. Thereafter, the signal voltage *should* shall not change more than 10% of VSS from the steady state values until the binary state occurs.

G.1.2 Receiver

The electrical characteristics of the receiver specified in RS-422 are:

o The receiver *should* shall not require differential input voltage more than 200mV to correctly assume the intended binary state, over an entire common-mode voltage range of -7 to +7V. The common-mode voltage (VCM) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to +/- 7V.

o The receiver *should* shall maintain correct operation for a differential input signal ranging between 200mV and 6V in magnitude.

o The maximum voltage between either receiver input terminal and receiver circuit ground *should* shall not exceed 10V (3V signal + 7V common-mode) in magnitude. Also, the receiver *should* shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.

o The total load (up to 10 receivers) *should* shall not have a

resistance more than 90 ohms at its input points.

Any Line Driver/Receiver meeting RS-422 should meet the requirements or the ESDI specification permits any Line Driver/Receiver meeting RS-422 to meet the requirements except for the timing specifications. Selecting from available devices requires knowledge of the interface connection followed by a comparison between the data treansfer timing specifications and manufacturers published data.

REFERENCE CLOCK is accepted by the controller and is used to generate WRITE CLOCK and to synchronize WRITE *DATA* BLOCK to WRITE CLOCK DATA. READ/REFERENCE CLOCK and READ DATA are measured at the drive as are and WRITE CLOCK and WRITE DATA are measured at the controller.

G.2.2 Allowable Skews

Table G-1 shows allowable skews (READ/REFERENCE CLOCK to WRITE CLOCK) for selected data rates.

		Data Rate in Megabits/second				
		5	10	15	20	24
tA (1/F)	(nsec)	200.0	100.0	66.7	50.0	41.60
Low Speed Port						
tB min. (.45tA)	(nsec)	90.0	45.0	30.0	22.5	18.70
tC min. (.21tA)	(nsec)	42.0	21.0	14.0	10.5	8.73
Total skew	(nsec)	48.0	24.0	16.0	12.0	9.96
High Speed Port						
tB min.(.408tA)	(nsec)	81.6	40.8	27.2	20.4	17.0
tD min.(.312tA)	(nsec)	62.4	31.2	20.8	15.6	13.0
Total skew	(nsec)	19.2	8.6	6.4	4.8	4.0

TABLE G-1 ALLOWABLE SKEW

G.2.2 RS-422 DEVICES

Table G-2 lists data for RS-422 devices appropriate for ESDI applications:

PART NO/TYPE	SKEW (nsec) (max)	SKEW (nsec) (typ)	TEMP	PWR SUP	STATUS
XX3486 Quad Receiver	NA	NA	25C	5V	ind.std
XX3487 Quad Driver	NA	2	25C	5V	ind.std
XX26LS31 Quad Driver	6	2	25C	5V	ind.std
XX26LS32 Quad Rcvr	NA	NA	25C	5V	ind.std
DS8921 Single Xcvr					
Receiver	5.0	0.5	0-70C	5V+-10%	NSC
Driver	6.0	0.5	"	"	"
DS8922/23 Dual Xcvr					
Receiver	5.0	0.5	0-70C	5V+-10%	NSC
Driver	6.0	0.5	"	"	"
DS8921A Single Xcvr					
Receiver	3.5	0.5	0-70C	5V+-10%	NSC
Driver	2.75	0.5	"	"	"
DS8922/23A Dual Xcvr					
Receiver	3.5	0.5	0-70C	5V+-10%	NSC
Driver	2.75	0.5	"	"	"

TABLE G-2. APPROPRIATE RS-422 DRIVERS/RECEIVERS/TRANSCEIVERS

G.3 Calculation of Allowable Skew

As an example of calculating allowable controller circuitry skew:

Assume: 24Mbits/Sec Data rate
0.25nsec cable skew
2X typical transceiver performance
High Speed Port specification.

Allowable skew = 4.0 - (0.25 + 1.0 + 1.0) nsec
= 4.0 - 2.25 nsec
= 1.75 nsec

Comment: It's not clear what the derivation of the allowable skews are and allowed for what? In any case, I think they will need to be revisited when the Standard is finalized. I think the material on these two pages, when fully resolved with the standard would in deed be useful.

Page App-22

o Servo embedded continuously around the disk: In this scheme servo data is frequently written around the disk. The drive makes this invisible to the controller by extending the read clock (extended periods). This technique is invisible to the controller, though the drive may place some restrictions on where data is written. This method is more common with optical disks.

Comment: Is extended clock synonymous with the figure which violates the 2 missing periods requirement? Or is it really referring to filling in clocks?

Head switch times: Drives which do not use servo data embedded on data tracks can typically switch heads within the same cylinder in a very short time (< 15usec). Drives with embedded servo data typically require a longer head switch time, around 1 ms to 5 ms. ESDI reports this fact via a general configuration bit. For long head switch times the drive must negate COMMAND COMPLETE until the head switch is complete and the controller must wait for COMMAND COMPLETE assertion before operating on the new track.

Page App-25

The minimum pad size that a controller must account for record is defined by the formula below:

Architectural Comment:

In the early days of the ESDI definition, there was a concept accepted that further expansion of the serial command interface would be implemented by a link command. Somewhere along the line this concept was dropped.

On the surface this does not seem to be a problem since in theory there could be in the order of 64K commands which is adequate even for optical drives. However the ESDI has been organized to branch off of 16 potential categories. This simplified structure suggests in the future more main branches may be desirable.

I think we should consider using Command Function Bits 15-12 set to 1111 as a Reserved Link Command Function.

I hope that you will find the foregoing helpful in the final edit of the ESDI standard. However, I do apologize for the paper this method consumes. In addition I urge that the committee approve the few technical changes I have requested, which for the most part were communicated in my earlier letters. Please do not hesitate to contact me if any of the points require further clarification.

G.E. Milligan
Member X3T9.2/3

cc: John Lohmeyer Chairman X3T9.2