X3T9.2/87-134

CONTROL DATA CANADA, LTD.

1855 Minnesota Court
Mississauga, Ontario
L5N 1K7

(416) 826-8640

August 5, 1987

TO: X3T9 Working Group

FROM: Roger Cummings

Please find attached a draft of the minutes of the last working group, which was held at the Fairtech center in Cupertino Ca. on July 16 and 17 1987. I apologize for the delay in getting them distributed.

If there are any corrections required or omissions noted please call me at (416)826-8640 or send MCI Mail to Roger Cummings, Canada (MCI ID: 289-5060).

As agreed at the meeting, the next working group will be held on August 19 and 20 i.e. the two days following the X3T9.2/X3T9.3 plenaries in Colorado Springs. Please see the minutes and Attachment 10 for details of the hotel.

Roger Cummings

Roger Cummings
Principal Engineer
Systems and Strategies
Control Data Canada Ltd.

#ny0/rc

DRAFT MINUTES OF JOINT ANSI X3T9.2 AND X3T9.3 WORKING GROUP HELD AT FAIRCHILD, CUPERTINO ON JULY 16 AND 17, 1987

The meeting of the IPI/HSC working group was hosted by Gary Murdock of Fairchild Semiconductor at the Fairtech Center, 10400 Ridgeview Ct.,Cupertino, California on July 16 and 17, 1987. Attendees included:

ALLIANT COMPUTER SYSTEMS	Steve Caldara
AMD	Jayshree Ullal
AMD	Sarosh Vesuna
AMDAHL	Masanori Motegi
CDC CANADA	Roger Cummings
CDC	Wayne Sanderson
CDC-MPI	Tom Leland
CDC-MPI	Rick Mansfield
CONVEX COMPUTER	Tom McClendon
DUPONT ELECTRONICS	Michael Kaplit
ENDL	I. Dal Allan
ETA SYSTEMS	Bill Hohn
FAIRCHILD SEMICONDUCTOR	Steve Kaufman
FAIRCHILD SEMICONDUCTOR	Jim Mears
FAIRCHILD SEMICONDUCTOR	Gary Murdock
FUJITSU AMERICA	Bob Driscal
FUJITSU AMERICA	Jim Luttrull
GOULD ELECTRONICS	Ed Balogh
GP ASSOCIATES	Robert Grow
GP ASSOCIATES	Ronald Perloff
HITACHI MICROSYSTEMS	Sam Karunanithi
HNSX	Will Leslie
IBM	Richard Bono
IBM	Henry Brandt
IBM	Ken Moe
IBM	Horst Truestedt
INTEGRATED PHOTONICS	Michael Pugh
INTEGRATED PHOTONICS	Wally St John
JOHN VON NEUMANN CENTER	Peter Paluzzi
LOS ALAMOS NATIONAL LABORATORY	Gene Dornhoff
LOS ALAMOS NATIONAL LABORATORY	Don Tolmie
MADISON CABLE	Robert Bellino
MULTIFLOW COMPUTER	Lynn D'Amico
NATIONAL SEMICONDICTOR	Kumar Sivasothy
NATIONAL SEMICONDUCTOR	Joel Martinez
ULTRA	Newt Perdue

The first morning of the meeting was taken up with presentations to the committee.

The first of these was by Jim Mears of Fairchild concerning their F100250 ECL part and some of the problems of NRZ transmission. The 100250 part was described as being a bidirectional transceiver with a 2.5 ns propogation delay, a 2 ns edge speed and a corner frequency of 500 MHz. It was built for Siemens whose application was to drive 15 meters of 30 AWG cable, hence the data sheet figure. It was stated, however, that a speed of 25 MHz over 50 feet of IPI cable would most likely be possible. Jim then presented some slides on transmission characteristics. Using NRZ encoding was described as becoming much more difficult over long line lengths due to dc level problems and limited common-mode range to to the low level of the power supply rails in the interface. The solution to this was stated to be encoding the data or using an ac transmission scheme and isolating the interface from the line by transformers or fiber optics. Jim's slides compared various encoding schemes, included a graph showing the effect of modulation rate and line length on jitter and also illustrated the effect of bias distortion and dc level problems in NRZ transmission. These slides are Attachment 1B, the F100250 data sheet being Attachment 1A.

Sarosh Vesuna of AMD then presented an update on the testing of the TAXI chips that they had presented the details of at the last working group. The TAXI chips have pseudo-ECL serial interfaces (they operate between +5 and 0 volts) that are designed to work with fiber optics. AMD expect the cost of fiber optics to decrease dramatically this year and stated that already the cost of fiber optics is comparable to that of best quality cable at a distance of 100 feet (NOTE: this was later discovered to be in error due to a lost order of magnitude). Sarosh described a test setup (pages 3 and 4 of the slides which are Attachment 2) which used simple ac coupling in place of transformer coupling and separate RG-58/U cables for each side of the differential interface (i.e. not triax). A simple go/nogo criterion was used for the test by having the logic analyzer compare the input and output data. Under these circumstances operation at 75 MHz was found to be possible over 120 feet of cable, and Sarosh stated that only 1 ns of jitter had been seen at the receiver which can handle 3 ns. He noted that they had not yet even tried operation at 200 feet, and that they recognized that the quality of the cable was important in determining the maximum distance at a particular frequency. It was also found to be important to string the cable out as coiling it generated considerable interference.

Ken Moe of IBM then briefly described some work that he is doing in updating his 1985 analysis of current mode differential timing which was presented at the last working group. He believes that analysis to have been somewhat pessimistic and that operation at 10 Megabytes per second can now be proven by simple arithmetic means. There is also a good chance that with the proposed new IPI cable the current differential parts can operate at 25 Megabytes/s over 200 feet of cable. A complete description of the new analysis was promised for the next working group.

Gene Dornhoff of Los Alamos then presented a timing analysis derived from some HSC work. The analysis assumed 100K ECL logic and transmitters and receivers and a 25 meter cable and resulted in a total skew of 17.45 ns. Gene also transferred his figures to the Transmission Parameters worksheet to allow easy comparison with other analyses (Page 4 of his slides which are Attachment 3). The definition of the 100114 part as the receiver sparked a discussion about common mode requirements which continued in the afternoon Physical Working Group.

Bob Bellino of Madison Cable indicated that if he received enough commitments of firm orders he would make a first run of 5000 feet of the proposed new IPI cable. A straw poll was taken that indicated that there was enough support for this course of action.

Don Tolmie of Los Alamos then presented an updated version of his HSC proposal. The first of his slides (page 1 of Attachment 4) summarized the changes. The replacement of Hamming code to byte parity was stated to be due to problems in supporting modular widths and the inappropriateness of Hamming to a serial (fiber) interface. Single edge clocking has been adopted because its simplicity outweighs any propagation problems. The IPI cables referenced are Bob Bellino's proposed new cables and not the existing IPI types. Wayne Sanderson of CDC questioned the use of a single clock across multiple data cables and Don replied that Cray saw that as no problem. Wayne then noted the difference between a single vendor solution and an industry standard.

Dal Allan of ENDL then presented a new alternative to the current IPI Physical definition. This was based on the specification of a Physical Layer Protocol (PHY) which allowed the separation of the interconnection technologies from protocol aspects. (It was noted that IBM have proposed a similar separation in SCSI such that fiber optic components can be used). As an example Dal's slides (Attachment 5) included an interconnection based on the AMD TAXI chips. Dal's definition could be used for a simplex, half-duplex or a full duplex interfaces but his stated preference was to disallow simplex and use a half-duplex scheme where a higher layer determined the active direction (to gain configuration flexibility). This statement began a discussion that was to continue sporadically for the entire meeting. Dal also noted that his Slave Selection transaction included a definition of the bus width in the response and thus allowed the Master to work dynamically with Slaves of different widths.

During the first afternoon, the meeting was split into two parts. A Physical Working Group chaired by Tom Leland of CDC-MPI met to discuss transceivers and cables in detail and the HSC group continued with the definition of HSC functional requirements.

The Physical Working Group discussed in detail the proposed new IPI cable. Bob Bellino offered a number of new configurations including drain wires etc. After much discussion it was agreed that the proposed new IPI cable should be as specified below:

Construction of
- 3 pairs inner layer
- 9 pairs second layer
- 15 pairs outer layer
- Aluminum/mylar tape (Al up)
- 85% braid
- Polyethylene sheath

Two pairs in the inner layer are dummy (clear)

Other pair is black/black+white and is ground or spare

Same color scheme as previous proposal

Outer layer overinsulated as before

Delta of 5 ns max per 50 meters between any pair in outer 2 layers

Delta of 8 ns max per 50 meters between inner pair and any other

Outside diameter of .505" (same as present)

Detail parameters are
- 106 +/- 6 ohms
- 17 pF/foot max
- 1.53 ns/foot max
- 0.65c

The group also continued the discussion about common mode range requirements. It was noted that the 100114 has only a 1 volt common mode range centered around Vbb (1290 mV). The current differential parts were stated to have a +/- 3 volt range and of course the RS 485 parts have an even wider range (+/- 5 volts). It was agreed that common mode is less important for a point-point interface like the one that Gene Dornoff had described in the morning session than a multi-drop one but nobody seemed to have a good idea of the magnitude of a range required in real-world situations. Apparently the RS-485 requirements were derived from the best that could be obtained with the then current technology. It was noted that in a multi-drop situation the common mode range of the drivers that are off is also very significant. Jim Mears undertook to provide a common mode range figure for the F100250.

The HSC group heard presentations on HSC applications and requirements from both Don Tolmie of Los Alamos and Tom McClendon of Convex Computer. Don's slides are Attachment 6 and Tom's Attachment 7. Other presentations without material attached were made by Ed Balogh of Gould, Wayne Sanderson of CDC Systems and Peter Paluzzi of the John von Neumann Center. The discussion on HSC functional requirements then continued. During a discussion about error rates a mistake was discovered in the minutes of the previous working group. The 10e-9 error rate should be 10e-15 to the next upper layer and 10e-21 at the application.

The second day began with summaries of the previous afternoon's separate meetings. Tom Leland summarized the activities of the Physical Working Group and Bob Grow of GP Associates was given the job of summarizing the HSC group's discussion.

Bob's summary lead to further discussion which occupied the rest of the day. Bob noted that a service interface needed to be defined between the link and physical layers and that the allocation of functions to those layers might be different from the allocations in the OSI model. He also noted the requirement for a "locking mechanism" to allow multiple bursts to be streamed and that defining an interface between the PHY and PMD (used in their FDDI sense) might be difficult because of the differences between serial and parallel schemes. Don Tolmie requested clarification in terms of the interface speed and the media length supported by both the protocol and the copper implementation. There was also a discussion of whether throttling was required. Tom McClendon of Convex argued strongly against throttling on the basis that any interface of the class required for HSC would incorporate a burst buffer. This lead to a discussion regarding message latency and it was agreed that a requirement should be for minimum latency. Roger Cummings raised a question about the standardization of higher-level protocols and after considerable discussion it was agreed that HSC applications were sufficiently undefined at this time as to make such standardization impractical.

Bob's final slides with all comments included are Attachment 8.

The discussion then returned to simplex vs half-duplex vs full duplex. Dal Allan produced a slide to clarify the terms which is Attachment 9. Michael Pugh of Integrated Photonics noted that the requirement for ECL mitigates strongly against bidirectional lines because both the driver and its termination have to be gated off the line for maximum performance. Jim Mears noted that there are ECL parts that can be gated off the line but that the techniques for doing this are all somewhat unsatisfactory. He also noted that the 100250 uses multiple level signalling to effectively provide separate paths in opposite directions across a single pair of wires. Jim undertook to provide a simplified 100250 schematic and full description of its operation for a future working group.

The issue of which type of interface to support was not resolved. There are strong preferences for half duplex to minimize the pin count required for a configuration and to support flexibility and thus decrease configuration cost. There are equally strong fears that supporting half duplex operation will make the protocol and transceivers required significantly more complex and thus violate the sacred principle of KISS.

The next working group was scheduled for the two days following the next plenary session. The dates are Wednesday August 19th and Thursday August 20th at the Clarion Hotel in Colorado Spring, Co. See Attachment 10.

The attendees were unanimous in their thanks to Gary Murdock for being an excellent host and providing both good facilities and fine food.

FAIRCHILD
A Schlumberger Company

F100250 Quint Line Transceiver

October 1986 PRELIMINARY INFORMATION

Memory & High Speed Logic

Description

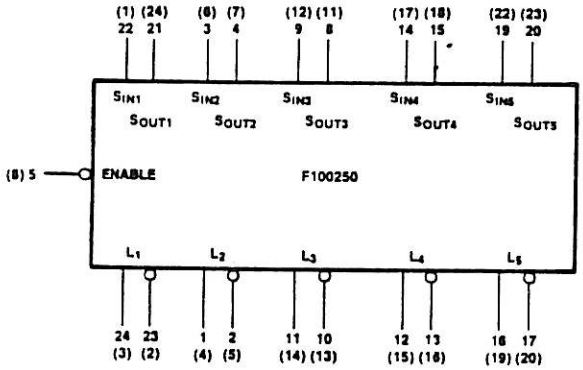
The F100250 is a quint line transceiver capable of simultaneously transmitting and receiving differential mode signals on a twisted pair line. Each transceiver has a signal input S_{IN}, a signal output S_{OUT} and two differential line inputs/outputs L and $\overline{L}$. Signals received from the lines L and $\overline{L}$ can be stored in an internal latch. The line outputs are designed to drive twisted pair lines. The $\overline{ENABLE}$ input is common to all five transceivers.

- **Full Duplex Operation**
- **Common Mode Noise Immunity of ± 1V**
- **Maximum Line Length of 15M (with 30 AWG Wire)**
- **Available in Ceramic DIP or Flatpak**

Pin Names

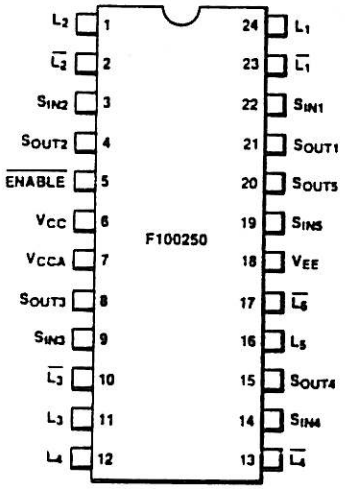
$\overline{ENABLE}$	Common Enable
S_{INn}	100K Signal Inputs
S_{OUTn}	100K Signal Outputs
L_n, $\overline{L_n}$	Differential Line Inputs/Outputs

Logic Symbol

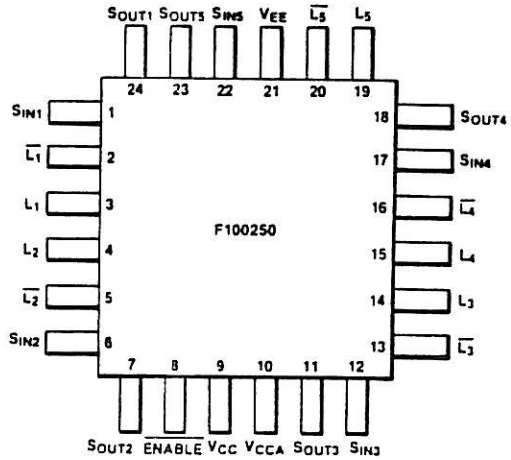


Connection Diagrams

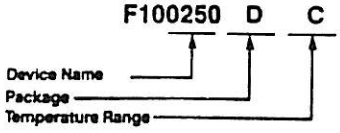
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Ordering Information



Packages
D = Ceramic DIP
F = Flatpak

Temperature Range
C = 0°C to +85°C

Fairchild Semiconductor Corporation, Memory & High Speed Logic
P.O. Box 5000, M/S 2C17, Puyallup, Washington 98373-0900

PRELIMINARY INFORMATION

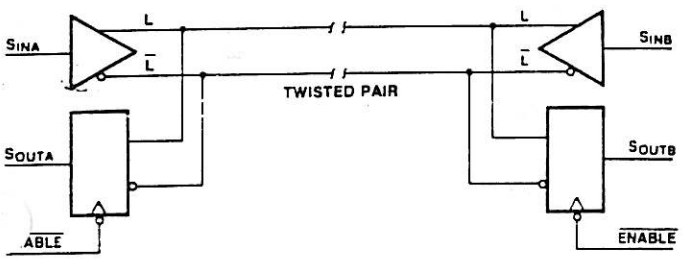
Absolute Maxiumum Ratings: Above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	-7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	-50 mA
Operating Range	-5.7 V to -4.2 V
Lead Temperature (Soldering 10 sec.)	300°C

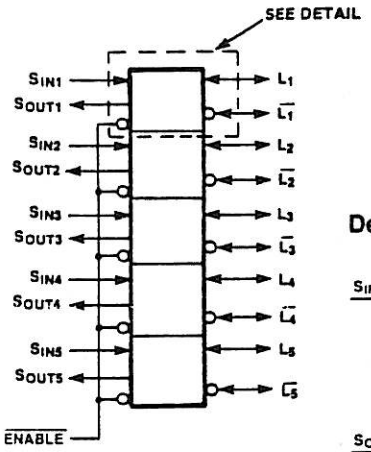
Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Case Temperature (T_C)
Min	Typ	Max	
−4.8 V	−4.5 V	−4.2 V	0°C to +85°C

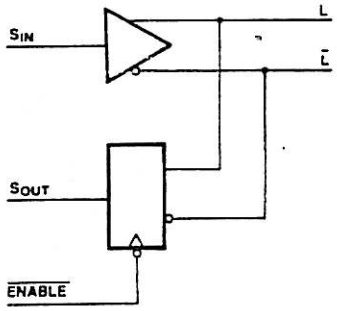
Figure 1 Interconnection of Two F100250 Circuits



Logic Diagram



Detail



Truth Table

$\overline{ENABLE}$	S_{INA}	S_{INB}	S_{OUTA}	S_{OUTB}	L	$\overline{L}$
H	X	X	$S_{OUTA(n-1)}$	$S_{OUTB(n-1)}$	*	*
L	L	L	L	L	U_L	U_H
L	L	H	H	L	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	L	L	H	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	H	H	H	U_H	U_L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
n-1 = Previous State
* = Dependent on S_{INA} and S_{INB}

$U_L \approx -1.27$ V
$U_H \approx -0.27$ V
$(U_L + U_H)/2 \approx -0.77$ V

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, $V_{CC} = V_{CCA}$ = GND, T_C = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current S_{INn} / $\overline{ENABLE}$			200 250	μA μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−280	−267	-180	mA	Inputs Open

ATTACHMENT 1A
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PRELIMINARY INFORMATION

DC Characteristics: V_{EE} = —4.5 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	-1025	-955	-880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to -2.0 V
V_{OL}	Output LOW Voltage	-1810	-1705	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1035	—	—	mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage	—	—	-1610	mV		
V_{KH}	Line Output HIGH Voltage	-370	—	-220	mV	No Load	
V_{KL}	Line Output LOW Voltage	-1400	—	-1090	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	
V_{IH}	Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50	—	—	μA	V_{IN} = $V_{IL(min)}$	

DC Characteristics: V_{EE} = —4.2 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	-1020	—	-880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to -2.0 V
V_{OL}	Output LOW Voltage	-1810	—	-1605	mV		
V_{OHC}	Output HIGH Voltage	-1030	—	—	mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage	—	—	-1595	mV		
V_{KH}	Line Output HIGH Voltage	-350	—	-200	mV	No Load	
V_{KL}	Line Output LOW Voltage	-1300	—	-990	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	
V_{IH}	Input HIGH Voltage	-1150	—	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50	—	—	μA	V_{IN} = $V_{IL(min)}$	

PRELIMINARY INFORMATION

DC Characteristics: V_{EE} = —4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions[4]	
V_{OH}	Output HIGH Voltage	-1035	—	-880	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to -2.0 V
V_{OL}	Output LOW Voltage	-1810	—	-1620	mV		
V_{OHC}	Output HIGH Voltage	-1045	—	—	mV	V_{IN} = $V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage	—	—	-1610	mV		
V_{KH}	Line Output HIGH Voltage	-400	—	-250	mV	No Load	
V_{KL}	Line Output LOW Voltage	-1500	—	-1190	mV	V_{IN} = $V_{IH(max)}$ or $V_{IL(min)}$	
V_{IH}	Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	—	-1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50	—	—	μA	V_{IN} = $V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at —4.2 V to —4.8 V
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Figure 2 S_{IN} to Differential Line

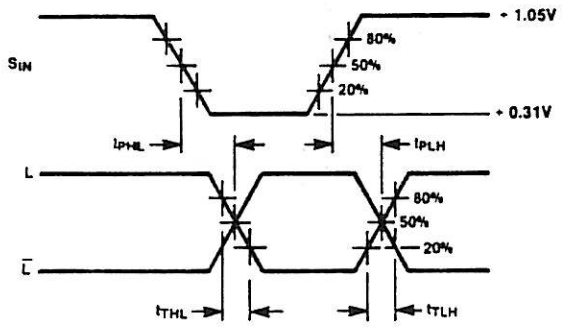
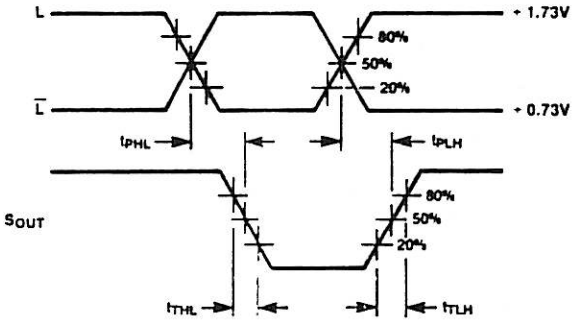


Figure 3 Differential Line to S_{OUT}



PRELIMINARY INFORMATION

Flatpak AC Characteristics: V_{EE} = —4.2 V to —4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_{IN} to S_{OUT}	2.0	6.0	2.0	6.0	2.0	6.0	ns	Figures 4 and 8
t_{PLH} t_{PHL}	Propagation Delay $\overline{ENABLE}$ to S_{OUT}	1.4	2.5	1.4	2.5	1.4	2.5	ns	Figures 5 and 8
t_{PLH} t_{PHL}	Propagation Delay S_{IN} to L, $\overline{L}$	1.2	2.5	1.2	2.5	1.2	2.5	ns	Figures 2, 3, and 7
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_{OUT}	1.0	4.1	1.0	4.1	1.0	4.1	ns	
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	1.9	0.5	1.9	0.5	1.9	ns	
t_S	Set-up Time L, $\overline{L}$	1.3		1.3		1.5		ns	Figure 6
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Ceramic Dual In-Line Package AC Characteristics: V_{EE} = —4.2 V to —4.8 V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_{IN} to S_{OUT}	2.0	6.0	2.0	6.2	2.0	6.2	ns	Figures 4 and 8
t_{PLH} t_{PHL}	Propagation Delay $\overline{ENABLE}$ to S_{OUT}	1.4	2.9	1.2	2.7	1.2	2.7	ns	Figures 5 and 8
t_{PLH} t_{PHL}	Propagation Delay S_{IN} to L, $\overline{L}$	1.2	2.9	1.2	2.7	1.2	2.7	ns	Figures 2, 3, and 7
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_{OUT}	1.0	4.0	1.0	4.3	1.0	4.3	ns	
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	2.0	0.5	2.0	0.5	2.0	ns	
t_S	Set-up Time L, $\overline{L}$	1.3		1.3		1.5		ns	Figure 6
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Figure 4 S_{IN} to S_{OUT}

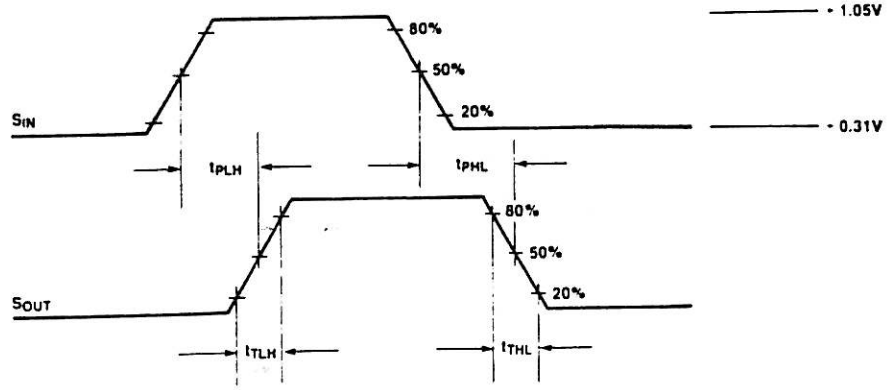


Figure 5 $\overline{\text{ENABLE}}$ to S_{OUT}

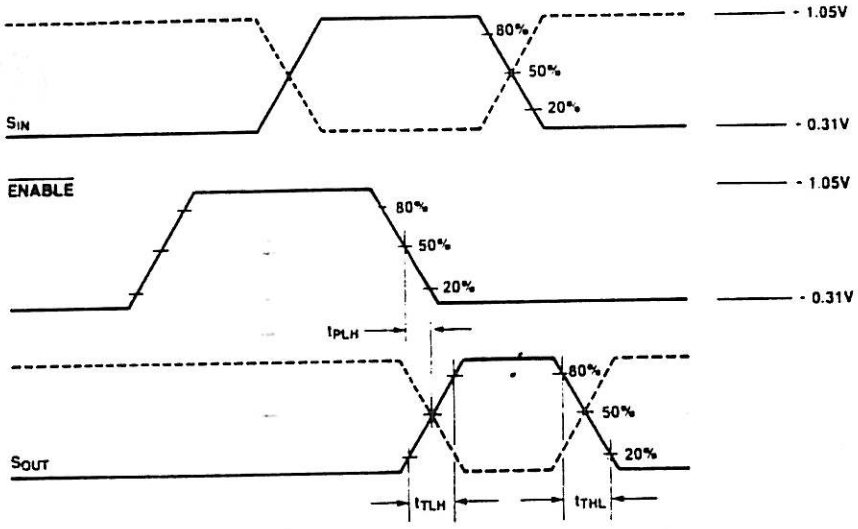
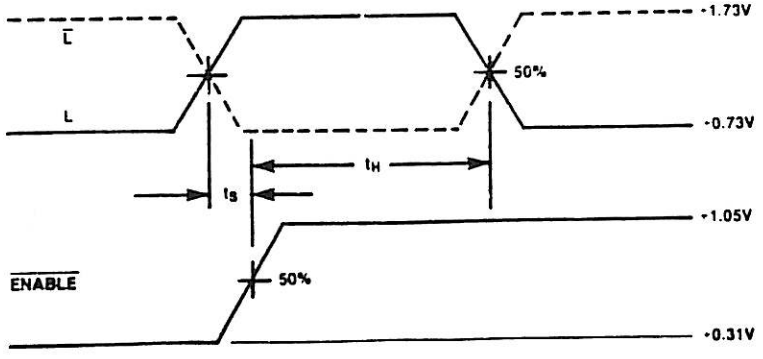


Figure 6 Line Data Setup and Hold Time

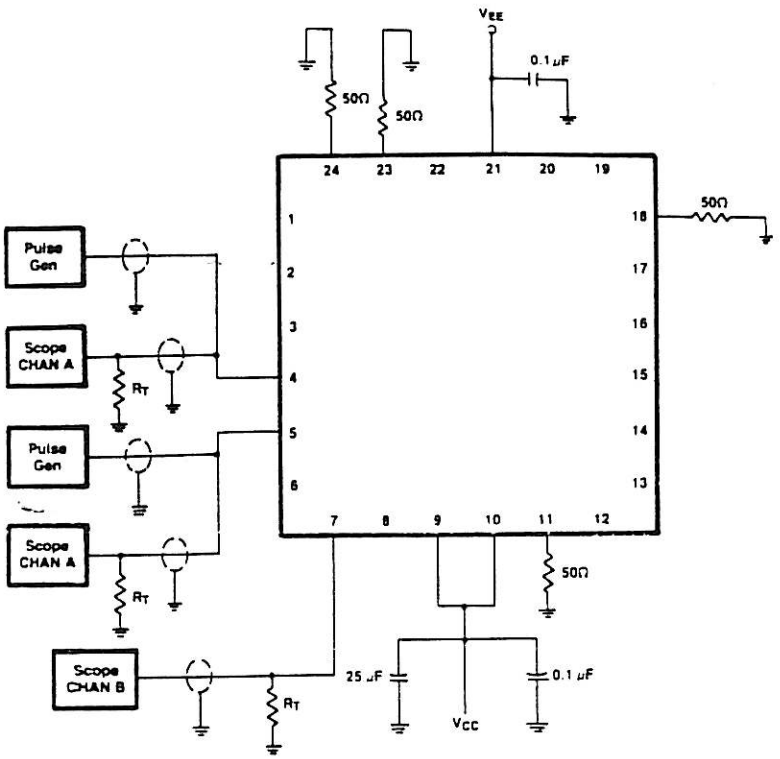


Notes

t_S is the minimum time before the transition of the clock that information must be present at the data input

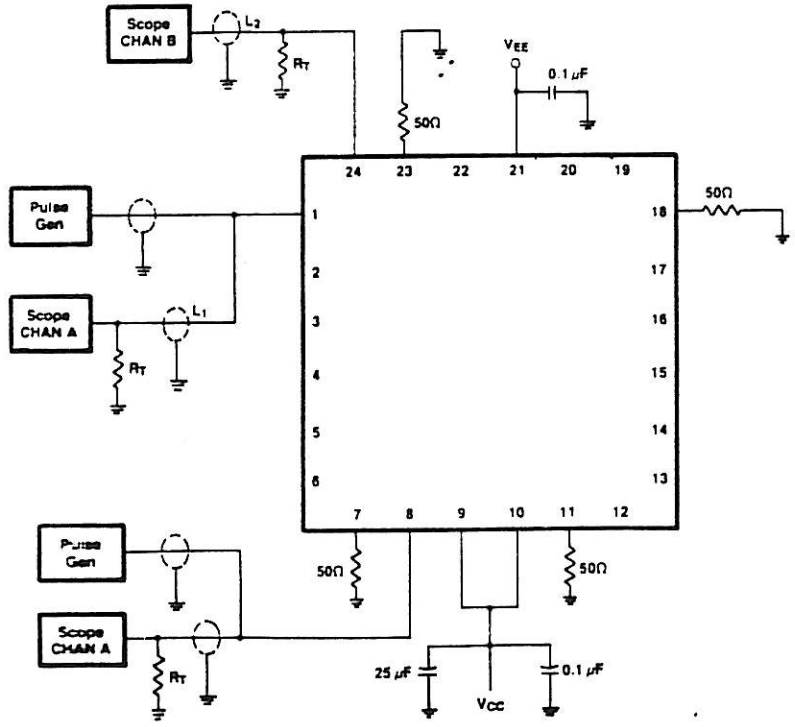
t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input

Figure 7 AC Test Circuit Differential Line to S_{OUT}



Notes = V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = fixture and stray capacitance ≤ 3 pF

Figure 8 AC Test Circuit S_{IN} to S_{OUT} and $\overline{\text{ENABLE}}$ to S_{OUT}

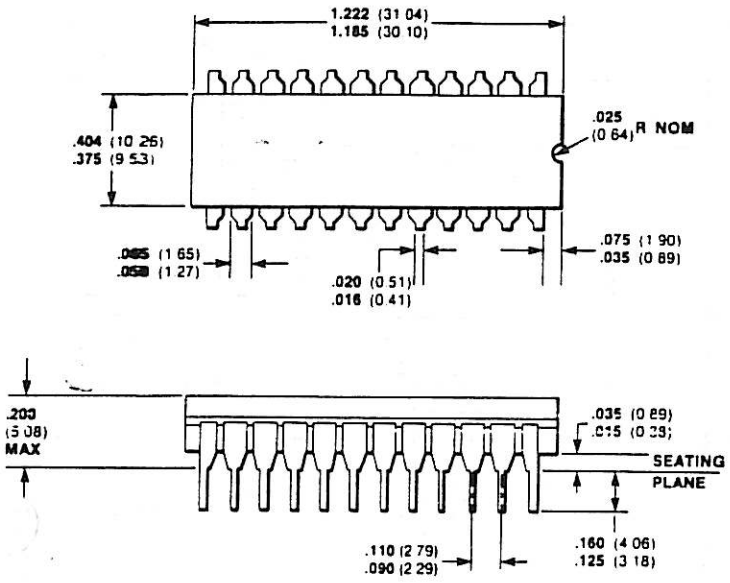


Notes = V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1µF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.
All differential line outputs on AC fixture should be cut open as close to the DUT as possible.

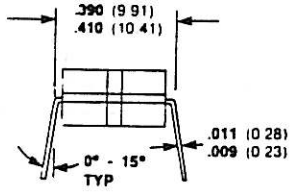
PRELIMINARY INFORMATION

Package Outlines

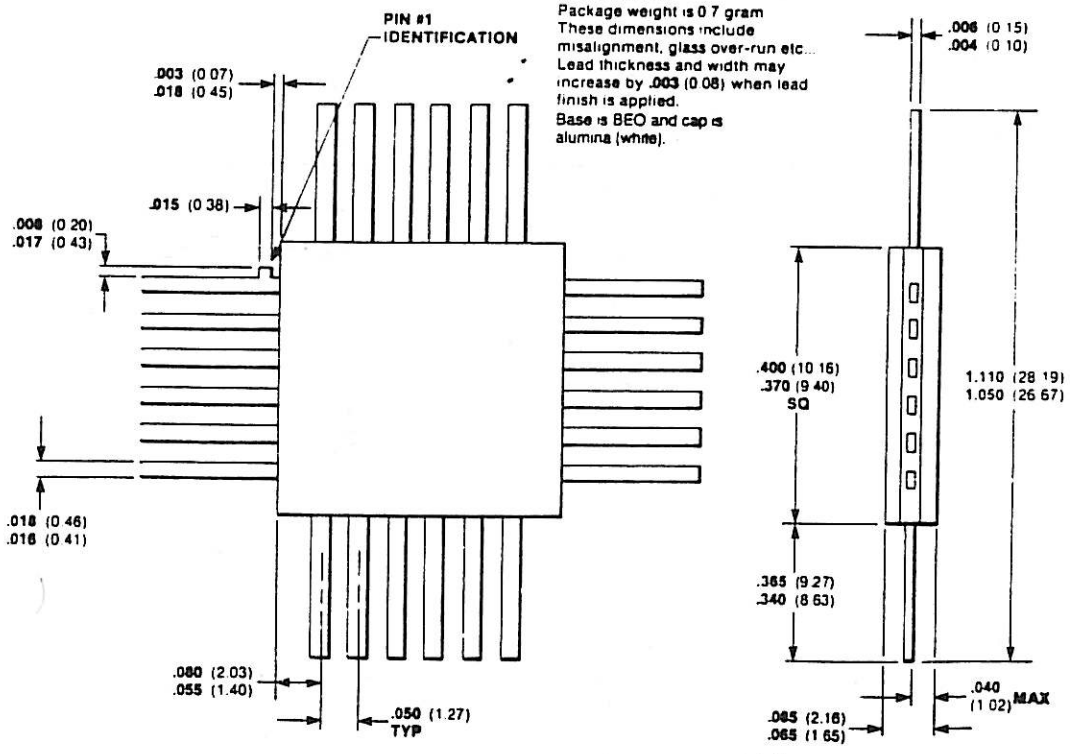
24-Pin Ceramic DIP



Notes
Pins are solder or tin-plated alloy 42 or equivalent
Hermetically sealed alumina package
Pins are intended for insertion in hole rows on .400 (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 6.0 grams
Board-drilling dimensions should equal your practice for .030 (0.76) inch diameter holes
These dimensions include misalignment, glass over-run etc.
Lead thickness and width may increase by .003 (0.08) when lead finish is applied

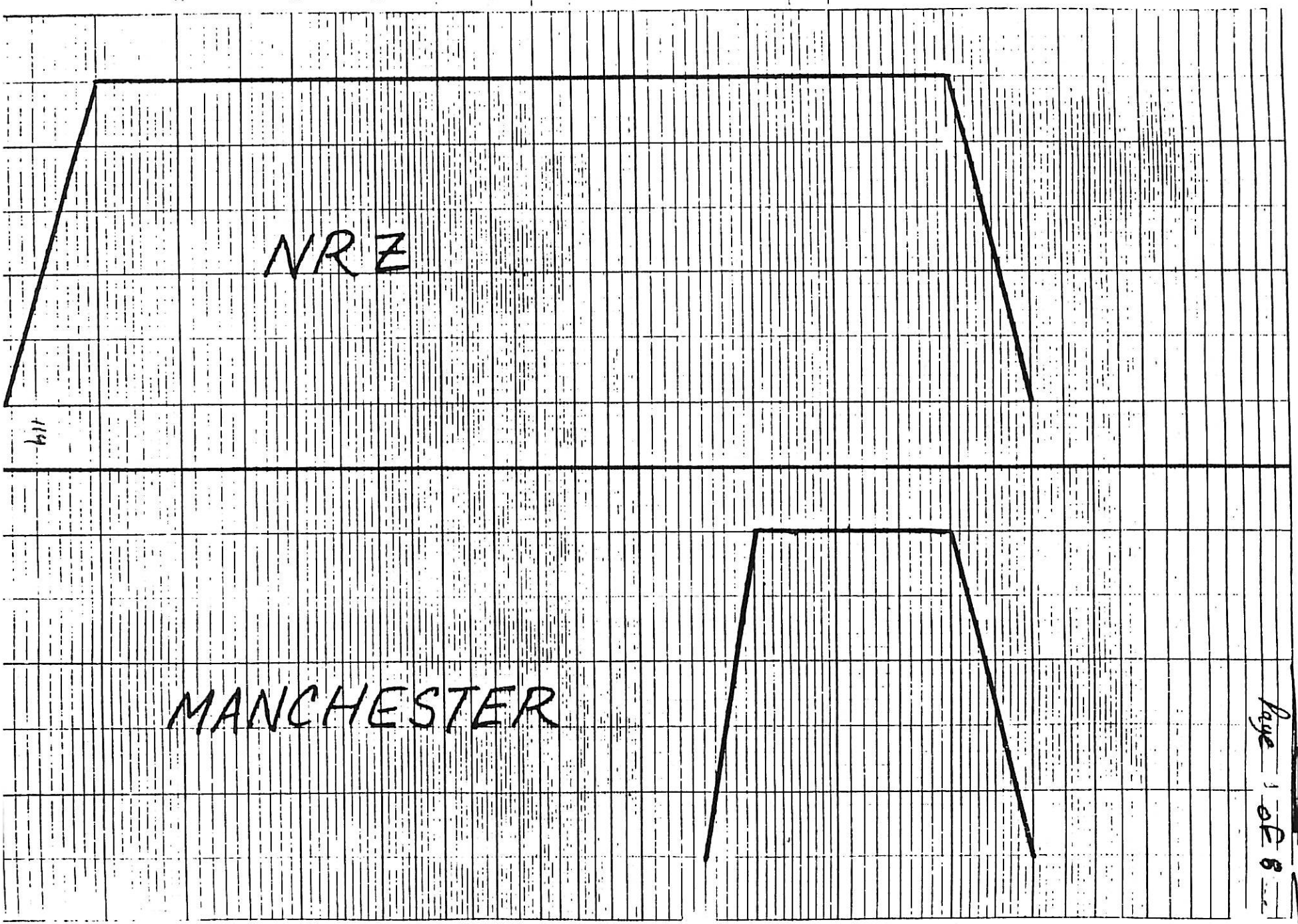


24-Pin Quad Cerpak



Notes
Pins are solder or tin-plated alloy 42 or equivaqlent
Package weight is 0.7 gram
These dimensions include misalignment, glass over-run etc...
Lead thickness and width may increase by .003 (0.08) when lead finish is applied.
Base is BEO and cap is alumina (white).

FREQUENCY SPECTRA



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Parameters of encoding schemes used in serial data communication

Code	Bandwidth F_L	Bandwidth F_H	Self-clocking	DC Presence	Bandspread ratio	Modulation Rate (symbols/data cell)
NRZ	0	0.5	no	yes	∞	1
RZ	0.25	1.0	yes	yes	4	2
Biphase	0.5	1.0	yes	no	2	2
Double-density (DM, MFM)	0	0.5	no	yes	2	2

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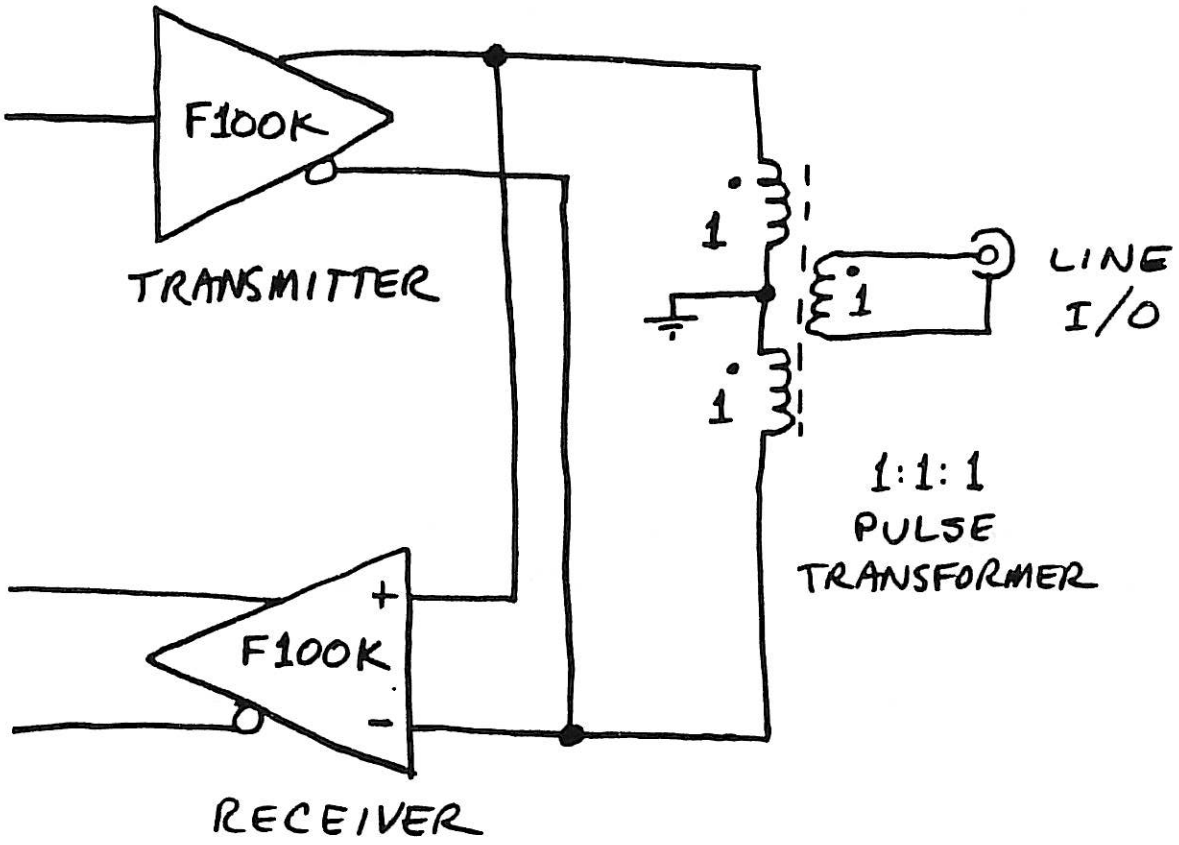
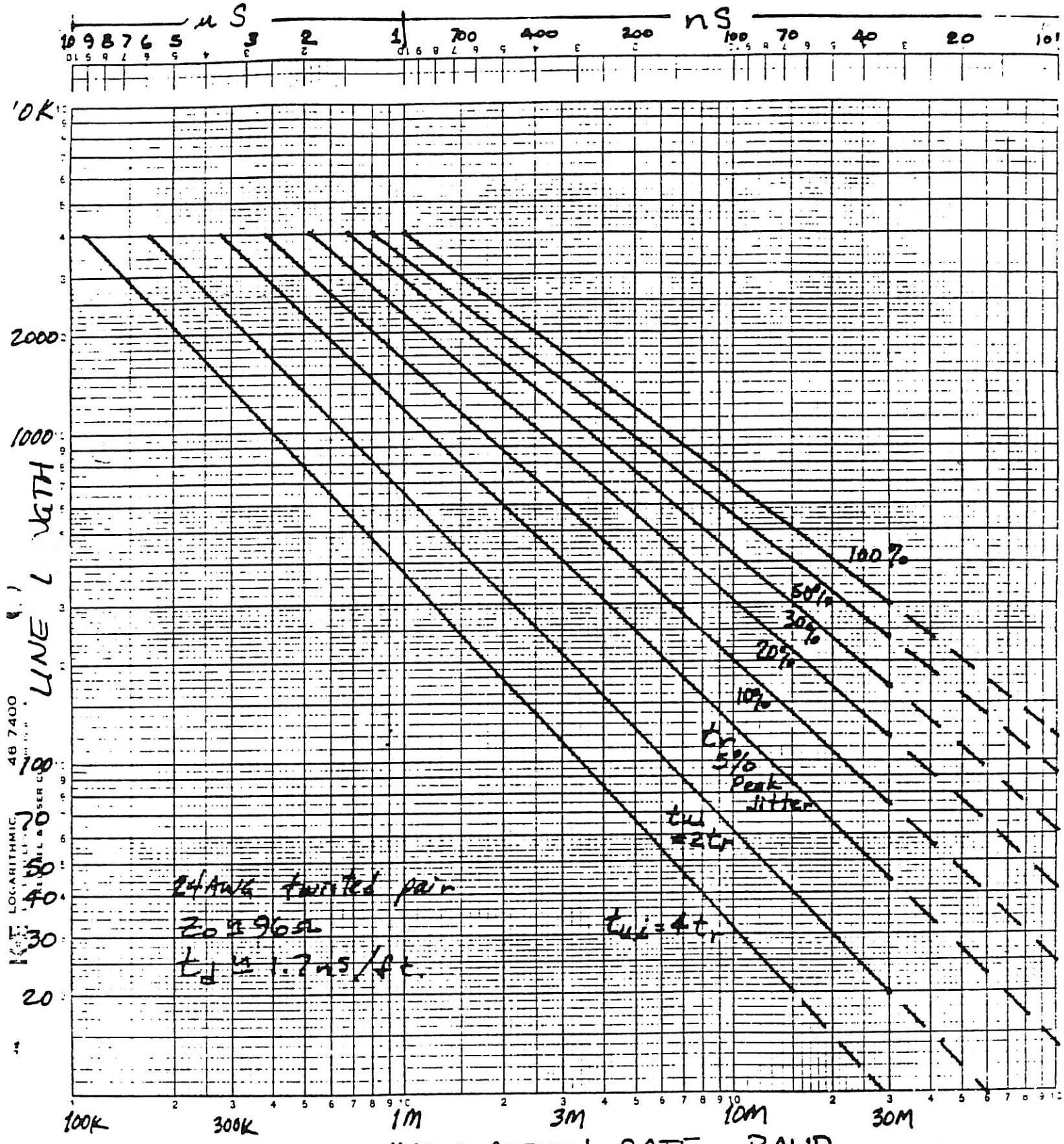
A.C. - COUPLED TRANSCEIVER




μS
nS
10K
2000
1000
100
LINE LENGTH (FT.)
100%
60%
30%
20%
10%
5%
Peak Jitter
$t_{ui} = 2t_r$
$t_{ui} = 4t_r$
24 AWG twisted pair
$Z_o = 96\Omega$
$t_d = 1.2$ ns/ft.
100K
300K
1M
3M
10M
30M
MODULATION RATE - BAUD
LOGARITHMIC
46 7400

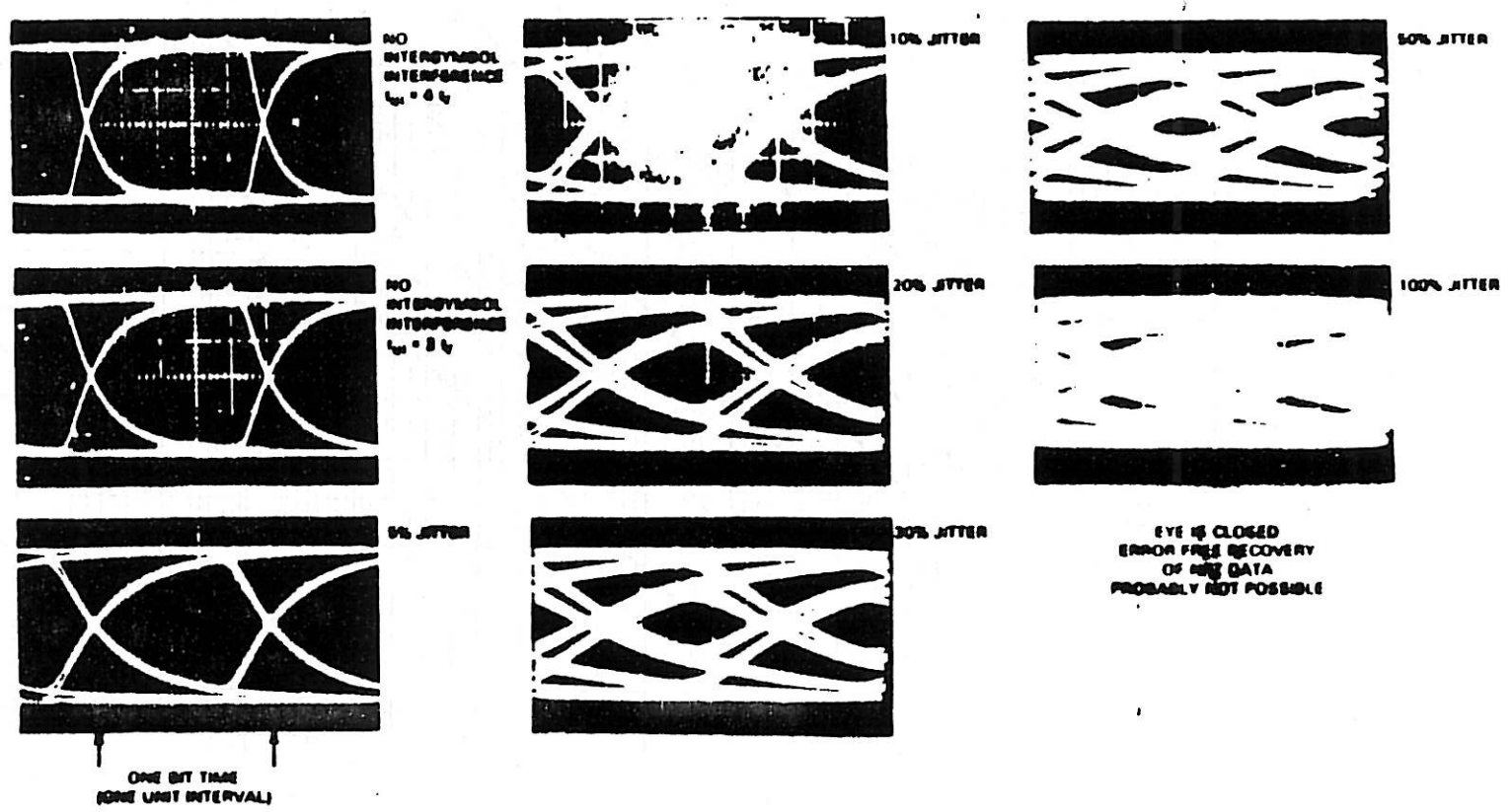


Fig. 10. Eye Patterns for NRZ Data Corresponding to Various Peak Transition Jitter

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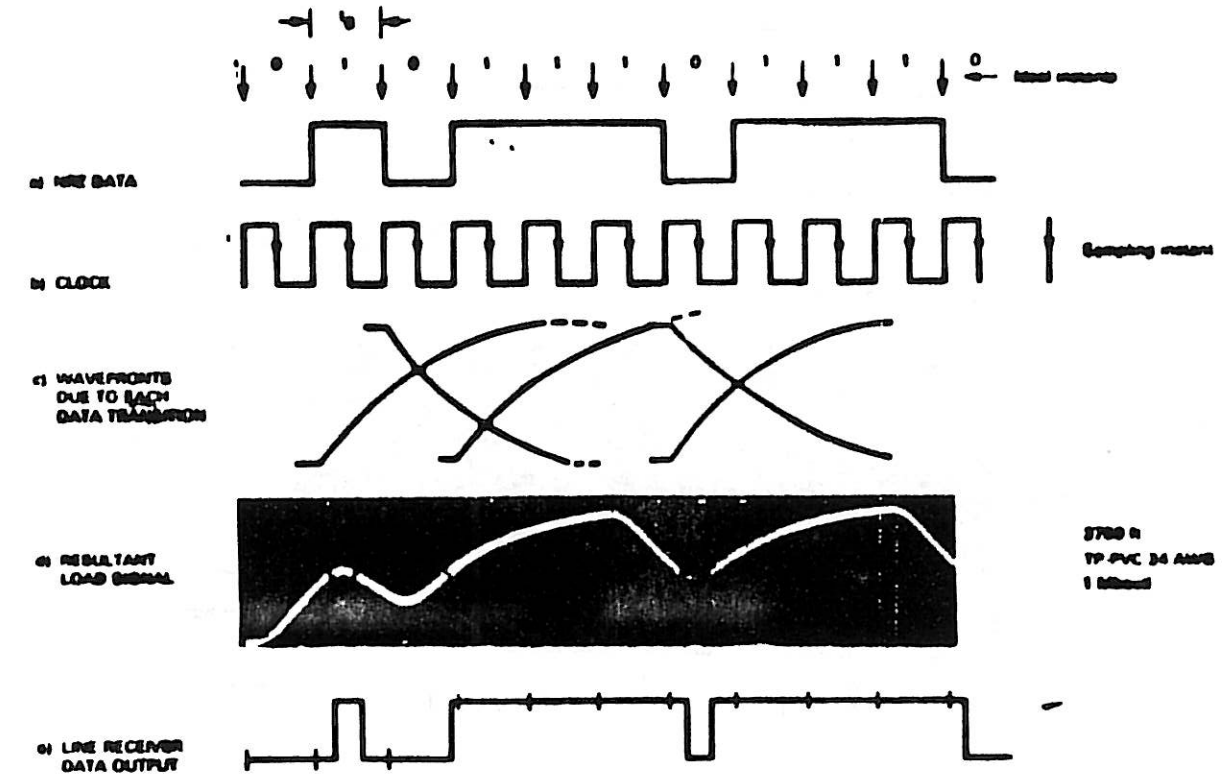

Fig. 2. NRZ Signaling

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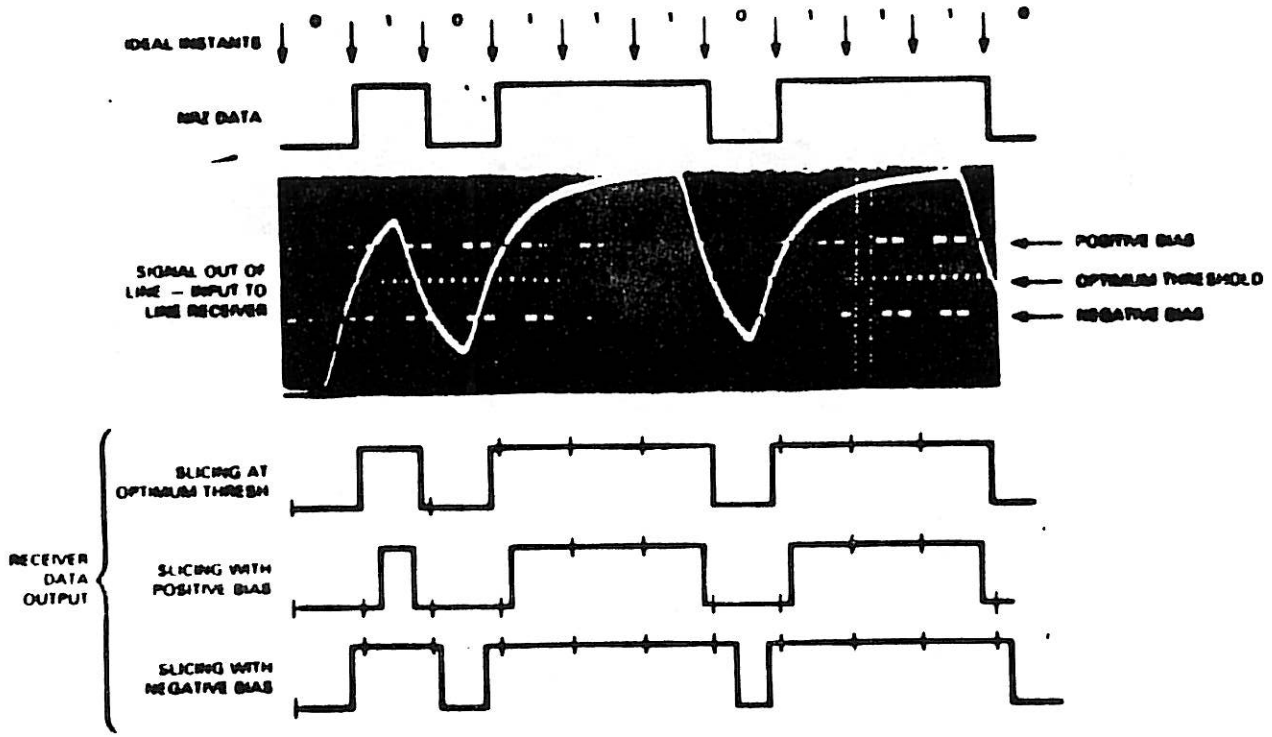

Fig. 3. Bias Distortion

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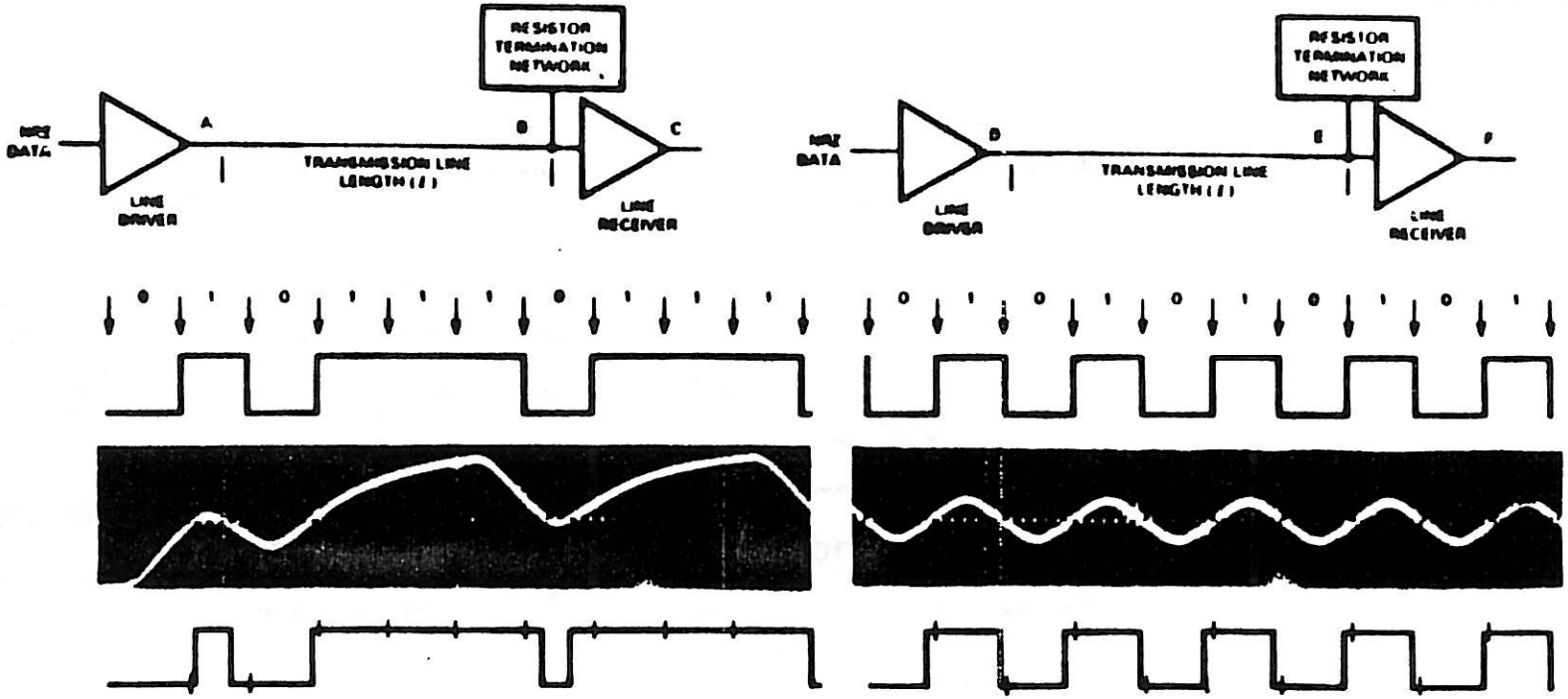

Fig. 4a. Comparison of NRZ Random Data and Dotting Signals

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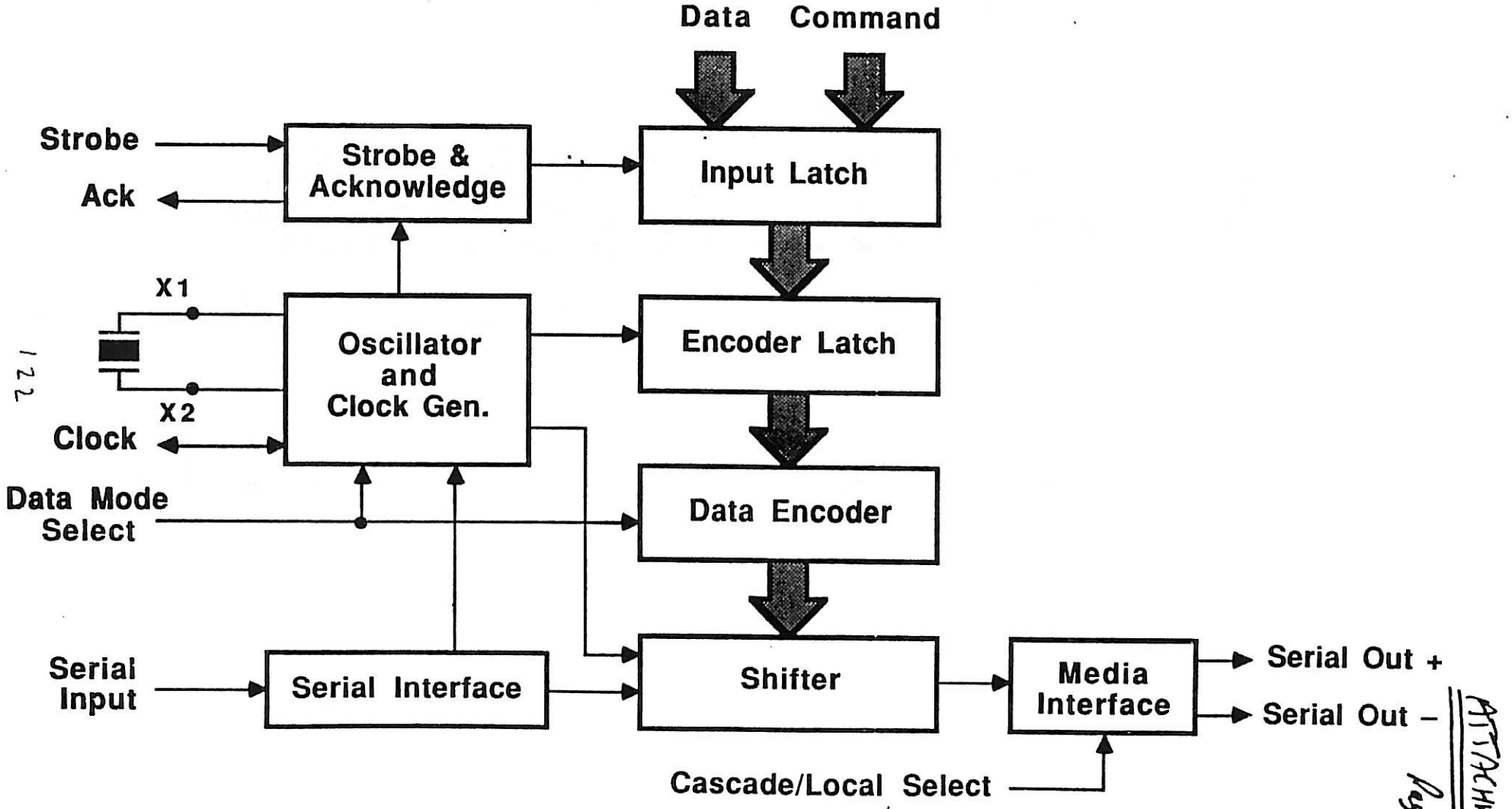
Am7968 TAXI Transmitter



096TAXI-005

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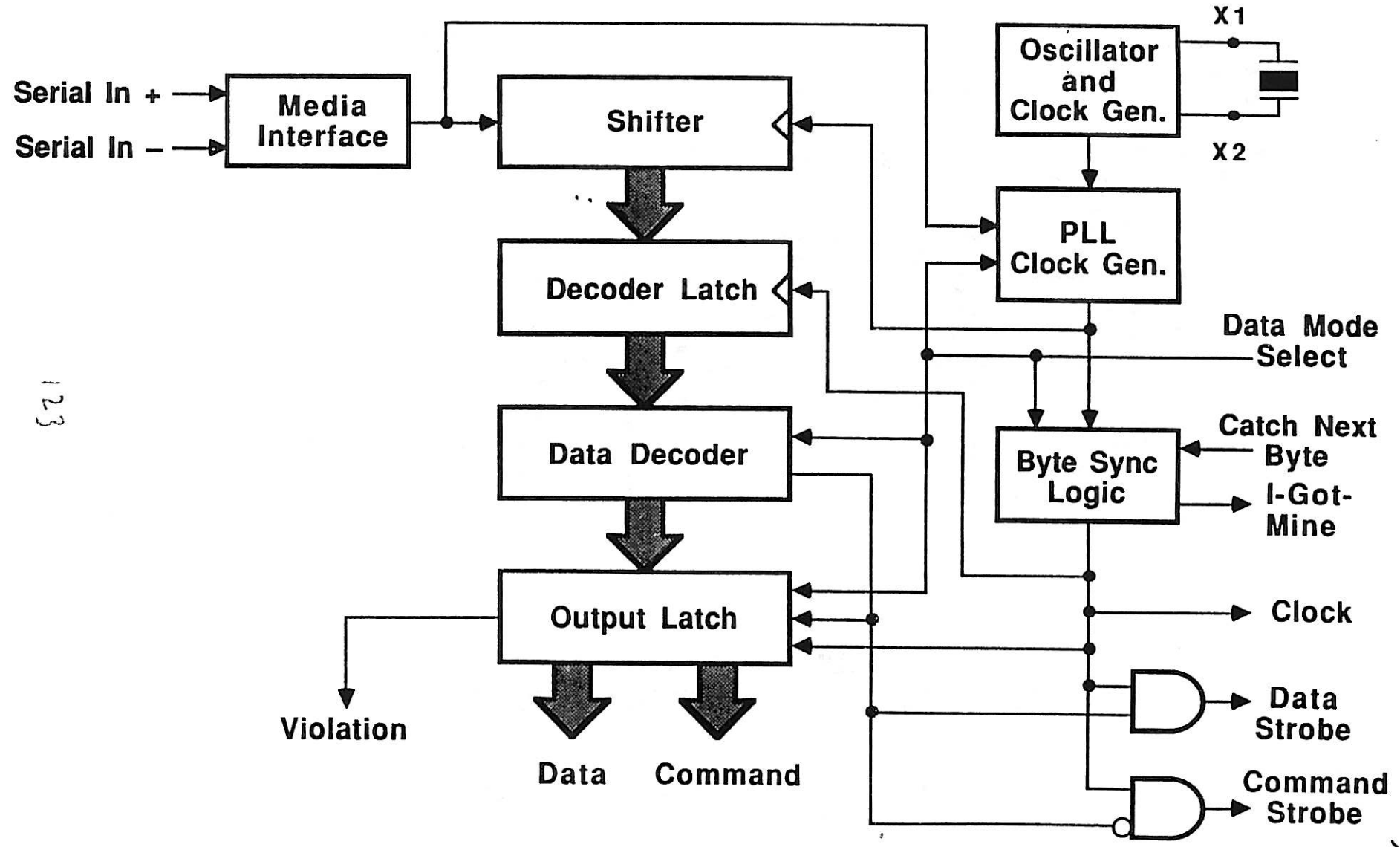
Am7969 TAXI Receiver



096TAXI-006

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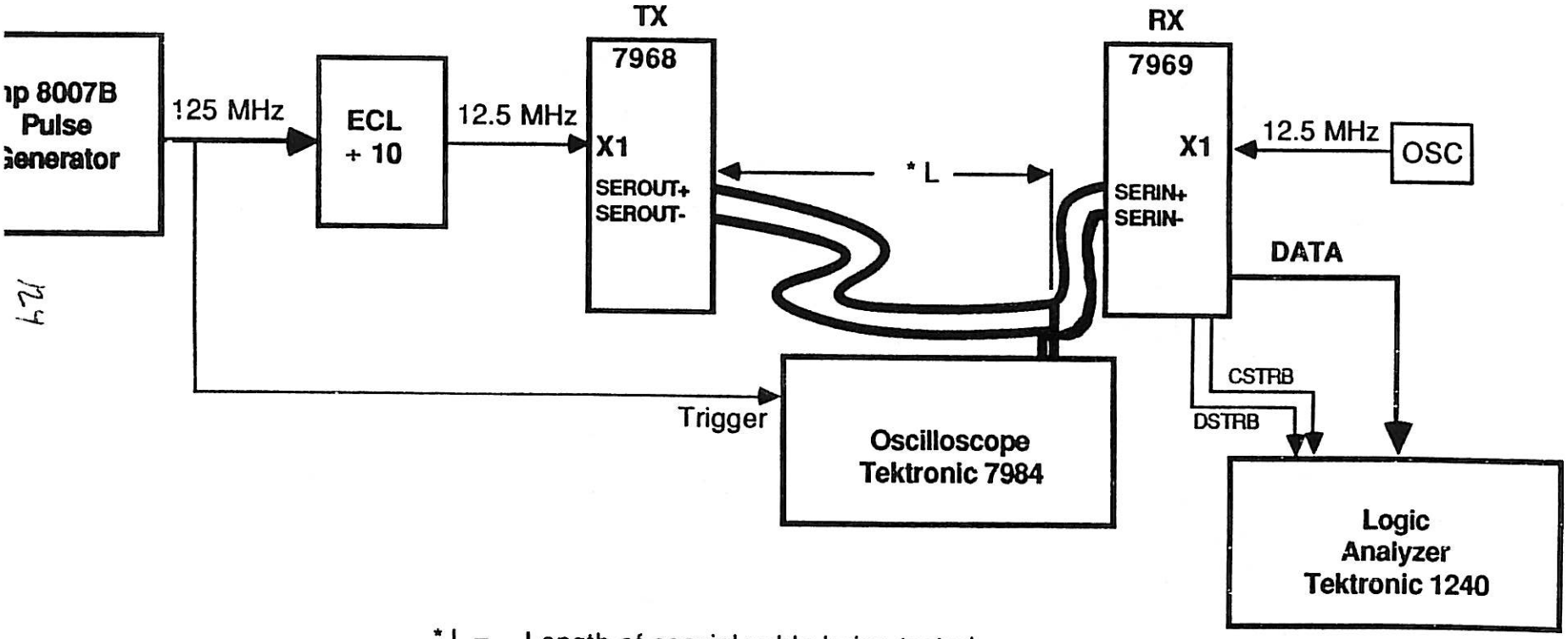
Block Diagram of Test Setup

Determination of maximum coaxial cable length over freqency range



* L = Length of coaxial cable being tested
RG58/U 53.4Ω

IK-6/87

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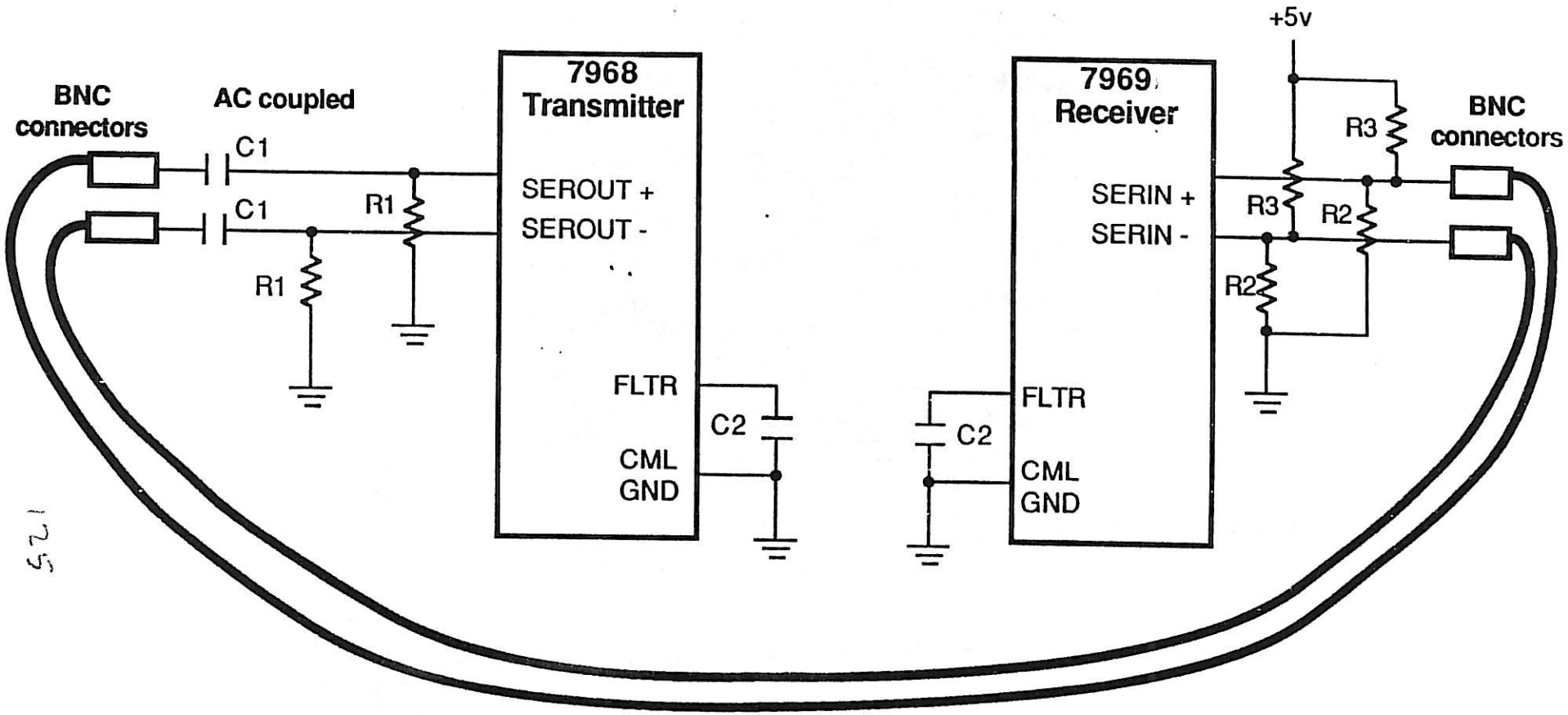
TAXI Interface



R1 = 500 Ω (CELL PULLDOWN)
R2 = 68 Ω
R3 = 160 Ω
C1 = 0.47 µF
C2 = 47000 pF

Coaxial Cable
RG58/U 53.4Ω

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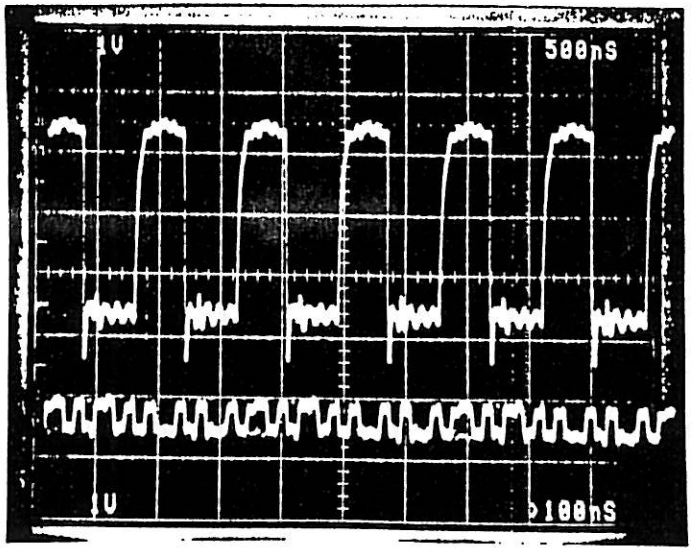
TX CLK & RX SERIN+

Voltage = 5.00
AC coupled
Temperature = Room temperature
Frequency = 6 MHz
Termination = 500Ω pull down @ transmitter,
voltage divider 160Ω/68Ω @ receiver
Length of Coaxial Cable = 160 feet

CLOCK

SERIN +



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Test Conditions

Data Patterns:

Three types
1. FDDI (DDJ Test pattern)
2. 0-255 counting pattern
3. 00,FF alternating pattern

Packet:

512 bytes
Three JK's during every test cycle

Operating Conditions:

Voltage (V_{CC})
Temperature (room)
Frequency (40 MHz – 70 MHz)
Termination
Length of Coaxial Cable (75 feet and 120 feet)

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ATTACHMENT 3

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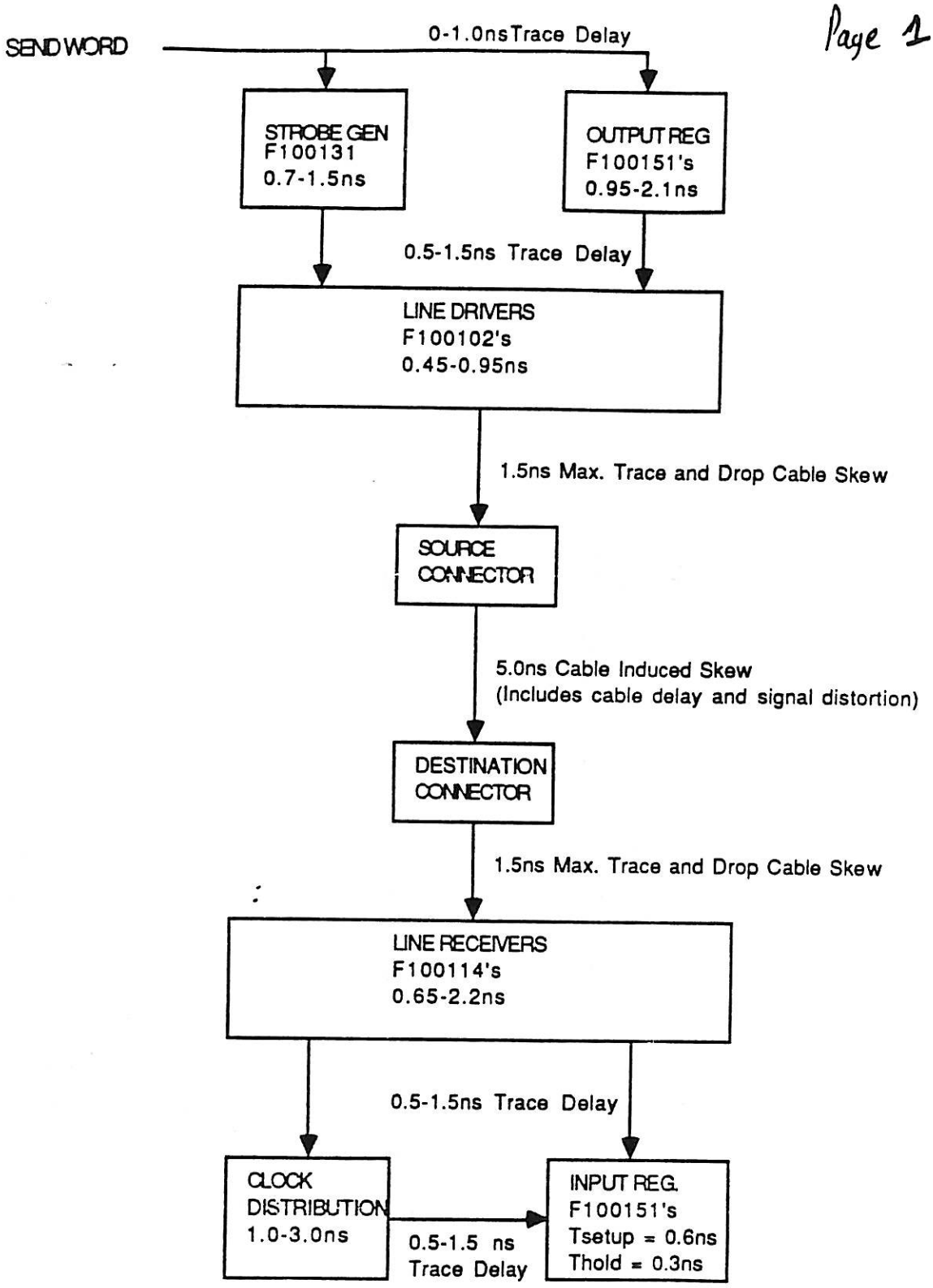

Component	Skew	Cumulative Skew
	L = Logic skew P = Pysical skew	
Tsk1	1.0ns (P)	1.0ns
Tsk2	1.4 (L)	2.4
Tsk3	1.0 (P)	3.4
Tsk4	0.5 (L)	3.9
Tsk5	1.5 (P)	5.4
Tsk6	5.0 (P)	10.4
Tsk7	1.5 (P)	11.9
Tsk8	1.55 (L)	13.45
Tsk9	1.0 (P)	14.45
Tsk10	2.0 (L)	16.45
Tsk11	1.0 (P)	17.45

Total estimated logic skew: 5.45 ns
Total estimated physical skew: 12.0 ns

Table 5.1: Sample skew calculation (F100K)

Tsk1: The time variation allowed for the Send Word signal to arrive at the inputs to the source output data register and the source strobe generator. It is assumed that the strobe will be generated by a single FF that will be reset with similar accuracy to generate the trailing edge of the strobe pulse. Data skew is assumed to be similar with respect to either edge of the strobe pulse (this is somewhat optimistic, but the figures for source strobe generation and destination clock distribution are felt to be pessimistic and the sum realistic.)

Tsk2: The difference between the minimum delay through the strobe generator and the maximum through the output register.

Tsk3: The difference between minimum and maximum PCB trace delays from the strobe generator and the output register to the line drivers.

Tsk4: The difference between the minimum and maximum delays through the line drivers.

Tsk5: The difference between minimum and maximum propagation delays from the line drivers to the source output connector. This includes PCB trace delays and possible drop cables.

Tsk6: Includes cable propagation skew and skew induced by the fact that the cable causes distortion of the signal.

Tsk7: Drop cable and PCB skew in the destination.

Tsk8: The difference between the minimum and maximum propagation delay through the destination line receivers.

Tsk9: PCB trace skew from the line receivers to the clock distribution logic and the input data register in the destination.

Tsk10: The uncertainty in the timing of the output of the clock buffers in the destination.

Tsk11: PCB trace skew from the clock buffers to the input register.

TRANSMISSION PARAMETERS

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#	GROUP	DESCRIPTION		AVG	MIN	MAX	DIFF
1		Clock Offset					1.0
2	Config	Transmitting Logic Skew	#				1.4
3	Config	Foil Delay					1.0
4	Xcvr	Transmitter Prop Delay					
5	Xcvr	Transmitter Asymmetry					0.5
6	Xcvr	Transmitter Rise/Fall Time	#				
7	Xcvr	Bias Asymmetry					
8	Config	Foil Delay					0.5
9	Config	Drop Cable Prop Delay					1.0
		CONNECTOR (To be spec value)					
11	Cable	External Cable Prop Delay	#				
12	Cable	Duty Cycle Distortion					5.0
13	Cable	Intersymbol Interference					
14	Cable	Bias Distortion					
		CONNECTOR (IPI spec value)					
16	Config	Drop Cable Prop Delay					1.0
17	Config	Foil Delay					0.5
18	Xcvr	Receiver Prop Delay					
19	Xcvr	Receiver Jitter	#				1.55
20	Xcvr	Receiver o/p Rise and Fall Time					
1	Config	Foil Delay					1.0
22	Logic	Logic Setup/Hold					3.6
		TOTALS					18.05

a) # shows stat. indep items
b) no stubs or crosstalk incl.

Taking sq root of sum of squares saves ns giving ns total

RJC – 7/15/87

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What is new about the Los Alamos 6/18/87 HSC Proposal

1. Accomodates modular design for 50, 100, 200 MByte/s.

2. Distance goal of 25 meters with copper wire, 32 bits wide, running at 100 MByte/s. May reduce distance to 15 meters to meet 100 MByte/s goal.

3. Changed from ECC Hamming type checking to byte parity.

4. Left the possibility of a longitudinal check sum open.

5. Added an Interconnect signal to detect disconnected cables.

6. Clocking on only one edge of the strobe signal.

7. Added more timing specifications.

8. Are trying to use the IPI twisted pair cables and connectors. 50 MByte/s requires 1 cable per simplex channel, 100 MByte/s requires 2 cables, and 200 MByte requires 4 cables.

9. Assuming ECL differential line drivers, receivers, and ECL data registers.

10. Included some sample skew calculations

Los Alamos High Speed Channel Proposal

1.0 INTRODUCTION

1.1 General

This specification is presented in five sections. The first is an introduction and definition of terms. The second and third are the logical definition of the channel signals and examples illustrating their timing relationships. The fourth is the specification of timing and other quantitative data, and section five is a brief discussion of possible future implementations.

1.2 Objectives

The specification defines the physical link layer of a simple high speed channel for the transmission of digital data between pieces of data processing equipment. The channel is optimized for predictable transfers of large blocks of data such as used for raster scan graphics terminals or file transfers between supercomputer class machines, but will also accommodate smaller messages. The channel is kept as simple as practical to minimize implementation cost and to speed throughput. It is expected to be used for point-to-point links, but could be implemented as a multi-drop bus or in a cross-point switch for special requirements.

A block diagram of a simple point-to-point link is shown below.

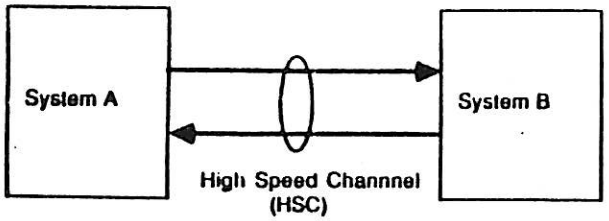

Figure 1.0. HSC System Block Diagram

1.2.1 Performance Goals

The dominant goal of the HSC is to provide a burst data rate between two systems of nominally 100 MByte/s with a data bus width of 32 bits. The channel is defined with a modular design so that a 16 bit wide data bus can be used to deliver 50 MByte/s, and a 64 bit wide bus can be used to deliver 200 MByte/s. A goal for distance with copper wire has been set at 25 meters. If necessary to meet the data rate goal, the distance will be reduced, but to not less than 15 meters. Signalling and control sequences are kept simple to allow average transfer rates for large (multi-megabyte) file transfers to approach the burst transfer rate.

The distance goals are set assuming standard ECL differential signal levels on twisted pair wire will be used. Copper wire to fiber optics converters will be used for longer distances.

The complete HSC is composed of two independent simplex channels, one in each direction. It may be considered either a single full duplex channel or two simplex channels. In some installations, such as an output-only link to a graphics terminal, only one simplex channel can be used.

1.3 Definition of Terms

High Speed Channel (HSC): The specifications and rules for connection and the transfer of data between pieces of equipment. The only physical equipment included is the cable and connectors used to make the physical connection between interfaces. The specification is symmetrical, and accommodates full duplex communications.

Source: The equipment at the end of the link from which data flows. May be used interchangeably with the terms Transmitter or TX Interface.

Destination: The equipment at the end of the link to which the data flows. May be used interchangeably with the terms Receiver or RX Interface. When it is necessary to distinguish between a Destination physically connected to a link and an addressed Destination elsewhere in a network, the physically connected Destination will be referred to as the Local Destination. This is often the case when a

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switching node is between the Source and the ultimate addressed Destination.

Word: 32 bits of data transferred across the channel from the source to the destination by a single strobe edge.

Doubleword: 64 bits of data transferred on a 64 bit wide channel from the source to the destination by a single strobe edge.

Halfword: 16 bits of data transferred on a 16 bit wide channel from the source to the destination by a single strobe edge.

Burst: A group of up to Bmax words sent by a source to a destination. No acknowledgement by the destination is required during the burst, but handshakes are required before the first burst and for each subsequent burst.

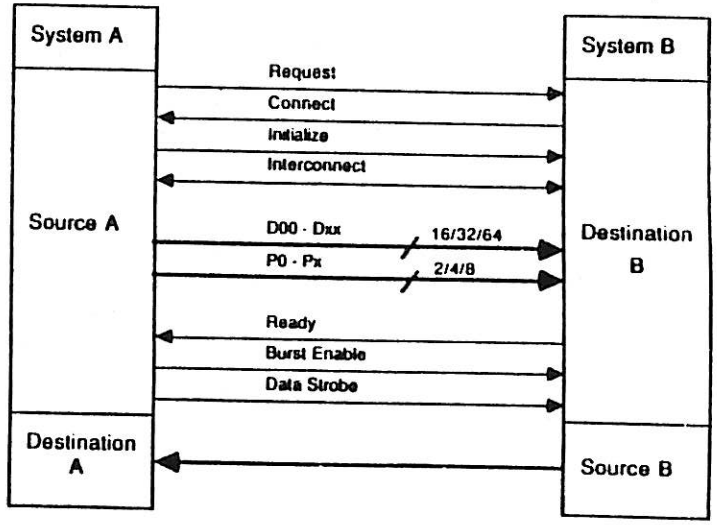
Packet: A group of data sent during one logical connection of the channel, composed of one or more bursts. No maximum size is specified by the channel, but a maximum may be required by a given interface or by a higher level software protocol.

Request Information Field: A single word of information that may optionally be sent from a source to a destination as part of the sequence of operations establishing a link from a source to a destination. The contents of this field must be defined at a higher level. An example of the type of information that may be useful would be an address.

Burst Trailer Field: A single word of information that may optionally be sent from a source to a destination at the end of each burst. This is being considered as a means to send a longitudinal check character with each burst to improve hardware checking of data integrity. The source would place the information or check bits on the D bus before negating Burst Enable. The trailing edge of Burst Enable would clock the information into the destination.

2.0 SIGNAL DEFINITIONS

A diagram of a simple system including two subsystems interconnected by one HSC is shown below. The arrows indicate the directions of the signals. Only one half of the full duplex channel is shown in detail. The second half is the mirror image.



B to A signals are the mirror image of A to B signals.

Figure 2.0. System Functional Block Diagram

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2.1 Channel Signal Groups

For convenience, the signals have been ordered into groups of related signals. Connector specifications and pin assignments are given in Section 4.

2.1.1 Data Bus (D00 - Dxx)

The data bus consists of 16, 32, or 64 parallel lines of data or address information. It is also used for any other information fields defined in this specification.

2.1.2 Error Control Bus (P0-Px)

Each 8 bits of the data bus word is accompanied by a single odd parity bit. Parity bit P0 is calculated from D0-D7, P1 from D8-D15, and Pn from D(8n)-D(8n+7).

2.1.3 Packet Control Lines

Request: Asserted by the source to notify the destination that the transmission of a packet is desired. The Request will remain asserted for the duration of the packet. When not asserted, Request indicates that none of the other source channel signals except Initialize are valid, and that the source will ignore any signals asserted by the destination. Request should not be asserted unless Interconnect is true.

The Request may be accompanied by a Request Information Field (I-Field) on the data bus. This is a single word whose meaning is defined at the next higher link layer. If used, the word must be asserted on the data bus RIsetup before Request is asserted, and must remain asserted until the destination returns Connect.

If a source times out an attempted connection before Connect is returned to the source, the source must implement a second time delay before attempting a new connection. The period of these delays will be system dependent.

Connect: Asserted by a destination in response to Request to notify the source that it is operational and available for data transfers. It may be dropped at any time during a transfer to indicate to the source that the connection is no longer available. When not asserted, the source will assume that none of the other signals asserted by the destination are valid. Whenever it is asserted, Ready must be in a valid state.

When both Request and Connect are asserted, a Connection is said to be established, or the Link is Connected.

If the optional I-Field is used, the Destination must not assert Connect until it is acceptable for the Source to remove the I-field word from the data bus.

Initialize: Asserted by the source to notify the destination that the source is going to "back up 15 yards and punt". The destination is responsible to take whatever action, if any, it must to start over. No response from the destination to the source is required at the physical link level.

The value of this signal is primarily to higher (software) levels, and will depend on the specific HSC implementation. At the hardware level, it simply means that the current packet (if any) has ended, and the next data transferred will be a new packet. It normally is asserted in response to an error condition, or as part of an initial power up sequence.

Two methods of implementing Initialize are provided. The simplest is a purely asynchronous pulse which may be asserted by the Source at any time Request is not asserted. It will not propagate beyond the Local Destination, and is intended only to establish the lowest level of communication. For the second method, the Source first establishes a link to the Destination. An I-field of information may be included if so defined for the interfaces involved. The Source then asserts the Initialize pulse, and completes the sequence by negating Request.

Interconnect: This signal is used to indicate to both the source and destination that the associated cable is connected. One pair in each cable is used for this function. The source drives the cable with a nominal current of Ict to the + pin of the cable pair and sinks the return current into the - pin. The destination completes the current

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loop when the cable is connected. Both the source and destination sense the current to determine that the cable is connected. If a current of the proper magnitude is sensed, Interconnect is considered to be logically true. If Interconnect is false, the cable is assumed to be disconnected and all received signals are ignored.

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2.1.4 Burst Control Lines

Ready: Asserted by the destination after a connection is established to indicate that a burst not to exceed Bmax words may be sent. The destination must negate Ready between bursts, and the source must not begin a second burst until Ready has been re-asserted.

A single burst lookahead function may be implemented in the destination such that the destination may drop Ready at any time following the start of the burst and re-assert Ready as soon as the destination can predict that it will be able to accept a second burst immediately following the current burst (for example, a double-buffered destination could accept two bursts before waiting). A source must implement the look-ahead function to be compatible with all destinations.

A source will recognize only one pending Ready beyond the burst currently in progress.

Burst Enable: Asserted by the source as a burst delimiter to the destination. Setup and hold times TBEsetup and TBEhold are measured with respect to the nearest data strobe active edge. The signal is asserted for the first and subsequent words including the final word in the burst. It is negated after the final word.

Data Strobe: Asserted by the source as a timing reference for data word transfers. The strobe will be asserted at the same time new information is placed on the data bus, and negated Tstb+ later. Timing of the strobe is asynchronous in that only the minimum width of the strobe, and the minimum time between between strobes (Tstb-) is specified. Pauses between strobes are permitted (but discouraged) as long as Burst Enable is left asserted. Extraneous strobes between bursts may be ignored.

The optimum time to sample the input data at the destination will be somewhat dependent on the design of the destination, but should normally be slightly after the trailing edge of the strobe pulse. This allows time for distribution delays on the destination PCB(s).

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3.0 TRANSACTION EXAMPLES

Logical timing diagrams are shown for several sample channel transactions.

3.1 Channel Selection

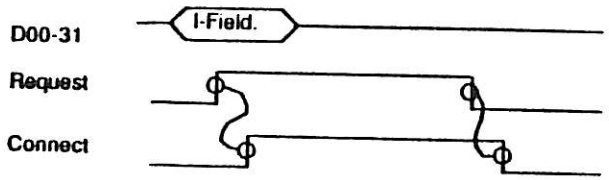

Figure 3.1. Link Connection Sequence

The source places the I-field (if used) on the data bus, and then asserts Request. The local destination responds to Request by asserting Connect when the I-field may be removed. The local destination will wait until any remote destination returns Connect, if a remote destination is involved, before it asserts Connect to the source. The source is then free to remove the I-field from the data bus.

After the end of the data transfer, the Source will drop Request. The destination will respond by dropping Connect.

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3.2 Aborted Channel Selection

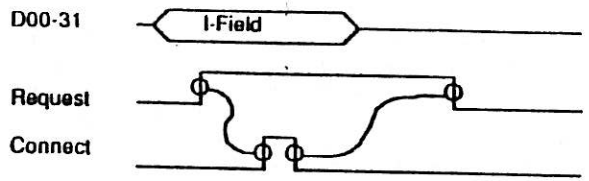

Figure 3.2. Aborted Channel Selection Sequence

The source places the I-field (if any) on the data bus, and then asserts Request. The local destination responds, and finds the destination is unavailable. (For example, the local destination is a port into a switch, and the destination is a host machine connected to another port on the switch, with that machine being down at this time.) The local destination signals to the source that a link cannot be established by asserting Connect and then negating Connect before asserting Ready.

Note that this transaction is just a degenerate special case of an illegal end where the destination terminates a transfer. In this case, the destination terminates the transfer without accepting any data.

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3.3. Initialization Sequences

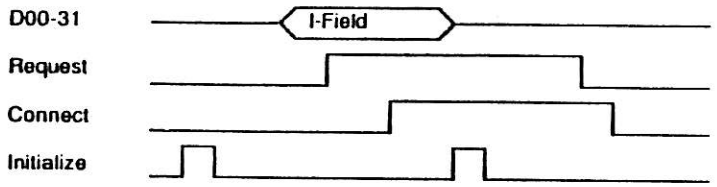

Figure 3.3. Initialization Sequences

The source asserts and negates Initialize without Request to reset the local destination. For the simplest Initialize, that is all that need be done. If the next level of Initialize is required, the source would begin by placing the I-field (if any) on the data bus, asserting Request, and waiting for Connect. When Connect is received, the source would then send an Initialize pulse to the destination. The source would then negate Request, ending the connection.

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3.4 Normal Data Transfer

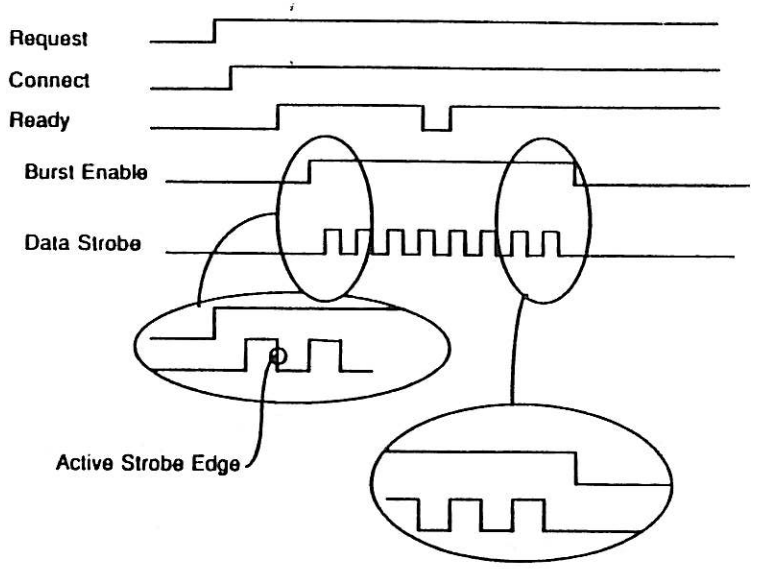

Figure 3.4. Normal Data Transfer

The start of a packet transfer is shown. For clarity, only 8 words are shown in the burst. The sequence begins with a normal link connection operation, with the source asserting Request and the destination responding with Connect. The sequence continues with the destination asserting Ready to signal to the source that a burst may be sent. The source then places data on the data bus and asserts Burst Enable. (The data bus is not shown. Data is asserted along with the leading edge of the strobe, and must meet the setup and hold times with respect to the active strobe edge as specified in section 4.) Data is clocked into the destination by the trailing edge of the strobe as shown. After the final word of the burst, Burst Enable is negated following the hold time specified in section 4.

If the Burst Trailer Field defined in paragraph 1.3 is implemented, the source would place the information or check bits on the data bus

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before negating Burst Enable, and hold the data valid long enough for the trailing edge of Burst Enable to clock the data into the destination. (Details will be added at a later date if this field is used.)

The destination may drop Ready at any time following the start of the burst, then re-assert it to indicate the destination can accept the next burst. Note that this destination has implemented the lookahead Ready sequence, by dropping and re-asserting Ready during the burst. If the source had more data available and ready for transfer, it would have permission to begin sending the second burst immediately after the end of the first. Following bursts are sent exactly as the first.

At the end of the packet, the source will drop Request and the destination will drop Connect.

It should be noted that the specification does not require the burst to be sent as a continuous stream - - there may be pauses between strobe edges as long as Burst Enable is left asserted.

Flow control is exercised by the destination by not asserting Ready until it is able to accept a full burst of up to Bmax words at the maximum channel speed.

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3.5 Data Timing

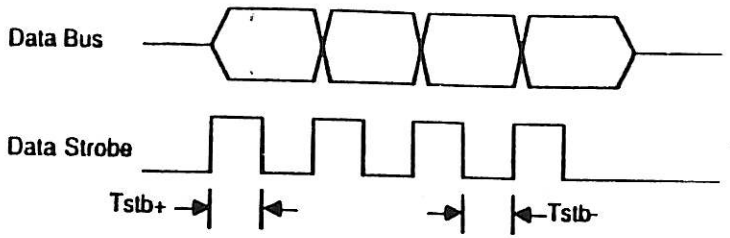

Figure 3.5. Data Bus Timing

The source asserts the strobe at the same time the data is placed on the data bus. The strobe remains asserted for Tstb+, and must be negated for a minimum time period of Tstb-. A burst should be sent as a continuous stream, but short pauses are not prohibited as long as the burst is completed within the time period Tbmax.

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3.6 Illegal End Transfer

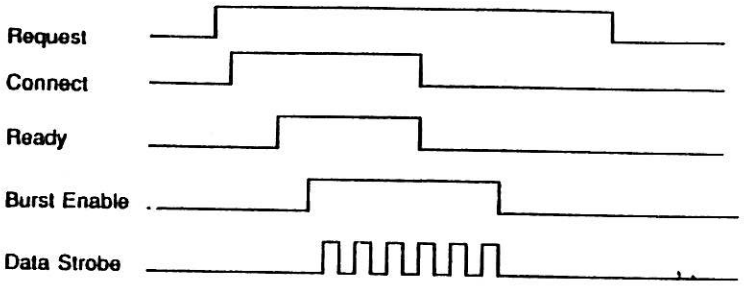

Figure 3.6. Illegal End Transfer

The source and destination start a transfer normally. At some time during the transfer, the destination detects a non-recoverable error. To terminate the transfer, the destination negates Connect (and Ready, since Ready should not be asserted without Connect). A link propagation delay later, the source detects the negation of Connect. In response, the source will drop Burst Enable and stop sending data strobes. Request will also be negated as soon as possible, but this may happen more slowly.

4.0 SIGNAL SPECIFICATIONS

All times are specified to be measured at the connector of the device generating the signal.

TDmin	Minimum time/word	40ns
BPSmax16	Maximum data rate (16 bit channel)	400 Mbit/s
BPSmax32	Maximum data rate (32 bit channel)	800 Mbit/s
BPSmas64	Maximum data rate (64 bit channel)	1.6 Gbit/s
TCmin+	Minimum time Connect is asserted	100ns
TCmin-	Minimum time Connect is negated	100ns
TImin	Minimum time Init is asserted	100ns
TImax	Maximum time Init is asserted	1000ns
Tstb+	Minimum time strobe is asserted	20ns
Tstb-	Minimum time strobe is negated	20ns
Tsetup	Min. data setup before trailing stb. edge	13ns
Thold	Min. data hold after trailing strobe edge	13ns
TBEsetup	Min. time BE is stable before strobe	100ns
TBEhold	Min. time BE is stable after strobe	100ns
TBEmin-	Minimum time BE is negated	100ns
Bmax	Max. number of words/burst	256
Tbmax	Maximum time to complete burst	50 microsec.
RIsetup	Minimum setup time for I-field	100ns
Ictmin	Minimum Interconnect loop current	2 mA
Ictmax	Maximum Interconnect loop current	5 mA
Vctmax	Max. Ict. loop drop at Destination	2 V

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4.1 Cable and Connector Specifications

Detailed specifications will be added as soon as testing and prototype evaluation is completed. The prototype cables will be IPI-type cables and connectors, with data and timing-critical signals assigned to the outer layers of the cable. The signal assignments will follow the modular definition of the channel, with a 16-bit implementation using one cable in each direction, a 32-bit channel using 2, and a 64-bit channel using 4. All cables will be identical, with one end having a female pin connector and one end a male. Cables will include an overall shield tied to the shell of the connector. Source connectors will be male, and will be designated T1 -Tn. Destination connectors will be female, and will be designated R1 - Rn.

Signals have been given the preliminary cable assignments below. Unused conductors will be tied to ground.

16-bit, 50 Mbyte/s Channel:

Connector T1: D00 - D15, P0 - P1, Strobe, Ready, Burst Enable, Request, Connect, Initialize, Interconnect 1

Connector R1: Same as T1

32-bit, 100 Mbyte/s Channel:

Connector T1: Same as above
Connector T2: D16 - D31, P2 - P3, Interconnect 2

Connector R1: Same as 16-bit R1
Connector R2: Same as T2

64-bit, 200 Mbyte/s Channel:

Connector T1: Same as above
Connector T2: Same as above
Connector T3: D32 - D47, P5 - P6, Interconnect 3
Connector T4: D48 - D63, P7 - P8, Interconnect 4

Connector R1: Same as T1
Connector R2: Same as T2
Connector R3: Same as T3
Connector R4: Same as T4

5.0 Relevant System Implementations

5.1 Switching Nodes

An early anticipated usage of the HSC is in the hub of a star network of machines interconnected with HSC's. The hub would be implemented as a fully connected crossbar switch. It is in anticipation of this application that the optional I-field has been included as part of the Connect sequence. In this application, the I-field will contain an address for a machine elsewhere in the network, not just at the far end of the link physically connected to the source machine.

The 32-bit address field is large enough to allow several logical fields to be included, if desired, to identify such things as message type as well as physical or logical addresses for the actual destination. 16-bit implementations will restrict the size of addresses or other information fields.

5.2 Serial Implementations (Fiber optics)

It is anticipated that long distance links will be implemented using fiber optics. Serial or parallel/serial connections would be used between channel adapters that convert the parallel HSC to a suitable serial optical format. Except for the unavoidable delays, the fiber repeaters should be transparent to the remainder of the system.

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5.3 Sample skew calculations

A sample calculation of approximate data and clock skews to be expected in an implementation of the channel has been done for the subsystem shown in Figure 5.1. The diagram starts at the data output register of the Source, and follows thru to the input register of the Destination. The design uses 10KH logic throughout, including line drivers and receivers. It assumes that the source has stable data available in a register at the time a "send word" signal is generated. The "send word" signal is the time reference for the skew calculations. The limit on acceptable worst case skew is one half of the strobe period less the larger of the destination input register's setup or hold time; in this case 18.5ns. A description of the individual terms is given, along with a table of the results.

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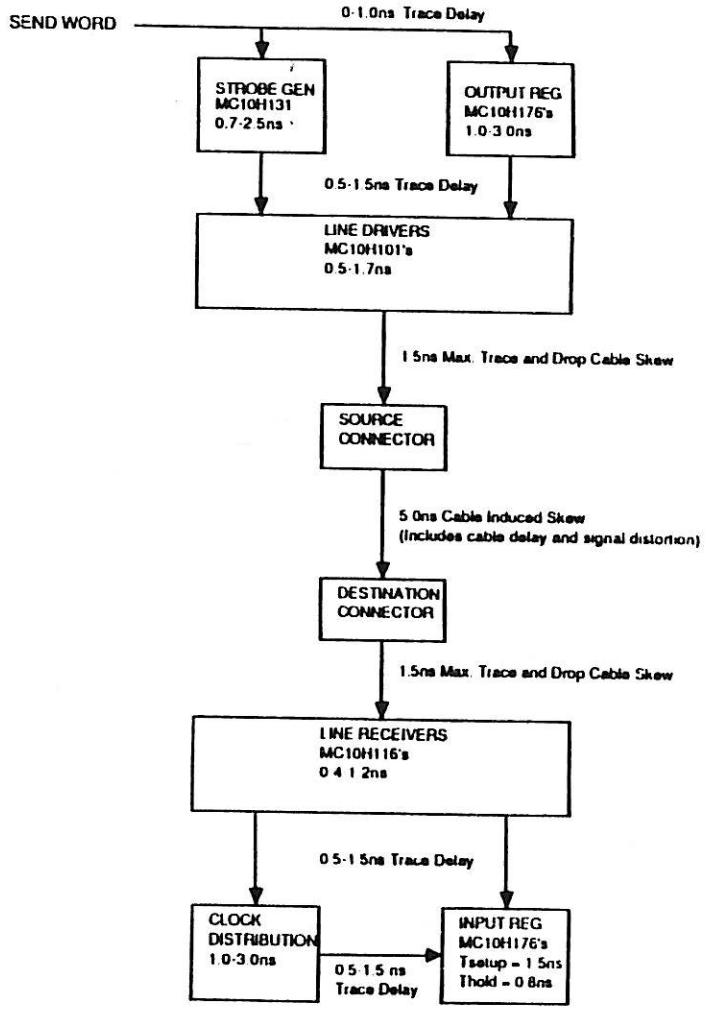

Figure 5.1 Sample Skew Calculation Block Diagram

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Tsk1: The time variation allowed for the Send Word signal to arrive at the inputs to the source output data register and the source strobe generator. It is assumed that the strobe will be generated by a single FF that will be reset with similar accuracy to generate the trailing edge of the strobe pulse. Data skew is assumed to be similar with respect to either edge of the strobe pulse (this is somewhat optimistic, but the figures for source strobe generation and destination clock distribution are felt to be pessimistic and the sum realistic.)

Tsk2: The difference between the minimum delay through the strobe generator and the maximum through the output register.

Tsk3: The difference between minimum and maximum PCB trace delays from the strobe generator and the output register to the line drivers.

Tsk4: The difference between the minimum and maximum delays through the line drivers.

Tsk5: The difference between minimum and maximum propagation delays from the line drivers to the source output connector. This includes PCB trace delays and possible drop cables.

Tsk6: Includes cable propagation skew and skew induced by the fact that the cable causes distortion of the signal.

Tsk7: Drop cable and PCB skew in the destination.

Tsk8: The difference between the minimum and maximum propagation delay through the destination line receivers.

Tsk9: PCB trace skew from the line receivers to the clock distribution logic and the input data register in the destination.

Tsk10: The uncertainty in the timing of the output of the clock buffers in the destination.

Tsk11: PCB trace skew from the clock buffers to the input register.

Component	Skew	Cumulative Skew
Tsk1	1.0ns	1.0ns
Tsk2	2.3	3.3
Tsk3	1.0	4.3
Tsk4	1.2	5.5
Tsk5	1.5	7.0
Tsk6	5.0	12.0
Tsk7	1.5	13.5
Tsk8	0.8	14.3
Tsk9	1.0	15.3
Tsk10	2.0	17.3
Tsk11	1.0	18.3

Table 5.1: Sample skew calculation

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ENDL
CONSULTING

July 15, 1987

To: X3T9.3 Working Group

Subject: Faster-Wider IPI/High Speed Channel

Attached is a copy of my proposal for the ENDL-HSC, an alternative to the current IPI Physical definition. The working group effort to extend X3.130 has focused on differential drivers/receivers used with twisted pair cable.

Results to date indicate that using the highest technology driver/receivers and optimized cable the fastest repetition rate is around 12.5 MBs. Cray is shipping a 100 MBs channel with a 64 bit bus that is limited to 25 meters.

New technology parts are coming to market which require us to re-examine the way interfaces are configured. At the last meeting, AMD presented the TAXI, a part developed for FDDI. The TAXI is specified at 100 Mbs repetition rate (bit serial) and provides an 8 bit memory interface to on-board logic.

A number of companies have either begun development on, or are shipping, a high performance channel. It is desirable that a standard permit these to comply with the logical protocol and logical command set layers.

One of the Functional Requirements decided upon at the last meeting was that we need an interface specified as a PHY (Physical Layer Protocol). A defined PHY would permit implementations at the board level to map to a number of different physical implementations. The ENDL-HSC is defined in the manner of a PHY, so that it can be transported to other physical implementations which do not rely on the TAXI chip. It is modular in design, with 12 conductors offering 100 MBs half duplex or 50 MBs duplex.

This proposal should be evaluated on two points:

- o the concept of a PHY with defined states that establish the sequences.
- o the use of TAXI chips with coaxial or fiber optic media.

Considerations of timing are not included but will be left to the activities of the "Law of Physics" working group.

I. Dal Allan

ENDL High Speed Channel

General

uded is an introduction and definition of terms used in the proposal. logical definition includes the channel control signals and the rmation Transfer protocol as well as examples illustrating their tionships.

Objectives

proposal defines the physical link layer and control protocol of a le, high speed channel for the transmission of digital data between es of equipment. The channel is optimized for predictable transfers of e blocks of data such as used for file transfers between processors er, mainframe, super-mini etc), storage systems (disk and tape), unications, and to output only devices such as laser printers and raster graphics terminals.

channel interface protocol is simple in order to minimize implementation and to enhance throughput. The transmission media is isolated from the rol protocol so that implementation of point to point links, multidrop crosspoint switches, or other special requirements may be made in a nology best suited to the environment of use.

ENDL-HSC may be configured as simplex, half-duplex, or full duplex.

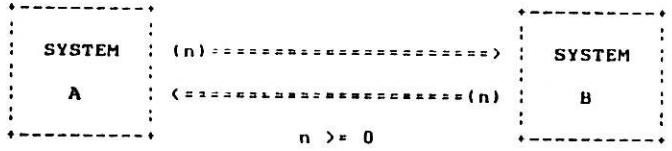


Figure 1-1 ENDL-HSC Block Diagram

l Performance Goals

primary goal of the ENDL-HSC is to provide a burst transfer rate of 50 (Megabytes per second) in a standard module of control signals and one Bus Group. A Data Bus Group has as many signals as is necessary to meet s. Additional Data Bus Groups may be added to increase the transfer rate, that four Data Bus Groups would provide a transfer rate of 200 MBs.

il for distance with copper has been set at 25 meters. The distance ation may be overcome with fiber optics, using the same signal and ol sequence schemes and the same components behind the transmitters/- vers. The fiber plant may be LED/multimode fiber at up to 2 KM or /single mode fiber at up to 50 KM.

il and control sequences are low in overhead. On large multiplexed file fers the effective transfer rate approaches nominal maximum.

plete HSC is composed of two independent control conductors, one in direction and a Data Bus Group which is capable of transferring

information in either direction (depending on choice of transmission media). The ENDL-HSC may be reconfigured by a higher level protocol to adjust transmission rates in either direction e.g. eight ENDL-HSCs could be reconfigured from 200 MBs in each direction to 400 MBs in one, 100 MBs in one/300 MBs in the other, or any other valid combination of Data Bus Groups. Reconfiguration is outside the scope of the proposal.

1.3 Definition of Terms

Burst

A variable length transfer of words sent by a source to a destination. Signal conditions established during transmission of a burst are used to identify whether or not an Information Transfer is to be terminated at the end of the burst or followed without interruption by another burst. The length of a burst is defined by a higher layer protocol.

Burst Transfer Prefix

Three words of information sent from a source to a destination as part of an Information Transfer sequence between the source and destination. This field consists (in order) of one word of packet length, a half-word Command Reference Number, and a 48 bit address.

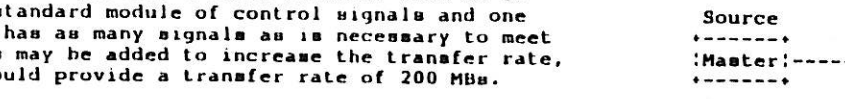
Burst Transfer Suffix

A single word of information sent from a source to a destination at the end of each burst. If the contents of the word are all zero there is no error checking on the integrity of the transfer. If the contents are nonzero, then the word contains the integrity check data for a polynomial previously agreed upon by the source and destination.

NOTE: Neither the Burst Transfer Prefix nor the Burst Transfer Suffix are included in the packet length.

Crosspoint Switch

A piece of equipment which accepts input as a slave on one port and redirects output as a master from another port e.g.



Data Bus Group

A set of conductors used to form a 50 MBs transfer rate. The number of conductors in the group is a function of the technology used.

Destination

This term describes the equipment to which information flows. A destination directly connected to the source is also known as a slave. NOTE: Information may be transferred by more than one master to more than one slave if a transfer from source to destination requires the use of more than one ENDL-

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Crosspoint Switch).

ıfications and rules for the connection, transfer of data, and
:tion between a master and a slave. The only physical equipment
is the cable and connectors used to make the connection between
es. The proposal may or may not be symmetrical, and accommodates
half duplex or full duplex communication.

lex

ıration consisting of at least two simplex ENDL-HSCs, each
ring in a different direction. Typically, but not necessarily, the
f Data Bus Groups in each simplex is the same.

lex

ıration of one ENDL-HSC which allows information to be transferred
ve to the master as well as master to slave. Transfers are not
ıt, with direction of transfer defined by a control exchange betwee
ıd slave prior to beginning an Information Transfer. NOTE: A source
slave transferring information under control of the master.

ion Transfer

ion transferred on the data bus which may be data, commands or
ı.

Connection

:e of one or more defined control exchanges between a master and
ior to performing an Information Transfer.

Disconnection

:e of one or more defined control exchanges between a master and
:er performing an Information Transfer. A logical connection is
to perform further Information Transfers.

ıty to intermix data bursts for each packet on the interface with
ıequences between each burst. Data bursts for different packets may
ıixed and are identified as such by the source.

:r sent during one logical connection which may be composed of one
ıursts. No maximum size is specified by the channel but a maximum
:quired by a higher level protocol.

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Simplex

An ENDL-HSC operated for unidirectional transfers from a master and slave.

Source

This term describes the equipment from which information flows. A full duplex configuration consists of one master and one slave at each end of two simplex configurations. The source is also referred to as the master on any one direct connection. NOTE: Information may be transferred by more than one master to more than one slave if a transfer from source to destination requires the use of more than one ENDL-HSC (see Crosspoint Switch).

Word

This term describes 32 bits of data transferred across the ENDL-HSC. The channel transfer rate depends on the repetition rate for each word and the number of words which are transferred simultaneously. The latter is a function of the number of Data Bus Groups used for the transfer. NOTE: there is no requirement that simplex channels transferring in opposite directions have the same carrying capacity in both directions e.g. a master with a transfer path of three Data Bus Groups out to a high performance graphics terminal may have only one Data Bus Group for keyboard input from that same terminal.

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ıal Definitions

es of different ENDL-HSC configurations are shown below. The arrows
:e the directions of the signals.

2-1 represents a 50 MBs full duplex configuration, which consists of
ıplex channels, each rated at 50 MBs.

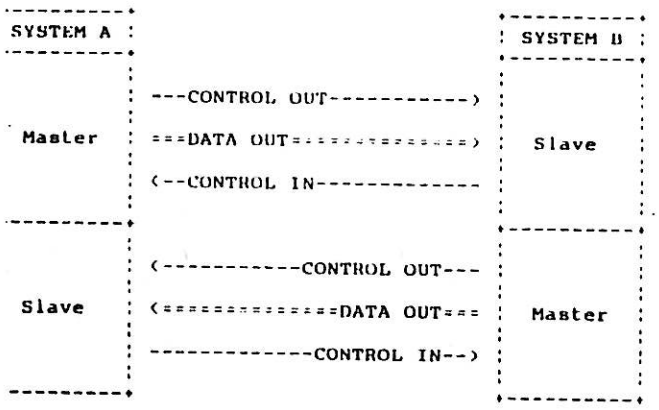

Figure 2-1 ENDL-HSC Full Duplex Configuration

2-2 represents a 100 MBs simplex configuration.

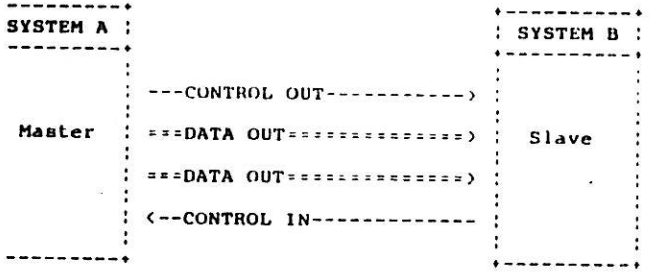

Figure 2-2 ENDL-HSC Simplex Configuration

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Figure 2-3 represents a 100 MBs half duplex configuration. The cable configuration is the same as a simplex. The logic to support half duplex operation varies at both the master and the slave e.g. the ability to turn around the direction of an Information Transfer. The transfer direction is defined by settings in the control sequences.

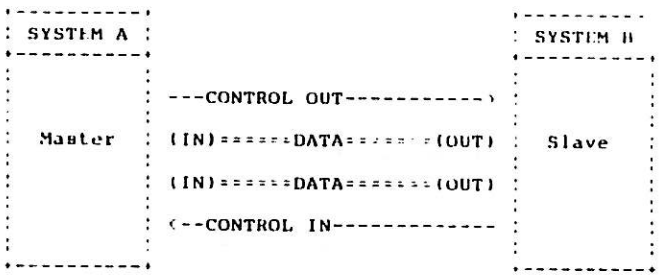

Figure 2-3 ENDL-HSC Half Duplex Configuration

2.1 Channel Signal Groups

Signal groups consists of two control conductors and one or more Data Bus Groups between the master and the slave. Each control conductor represents one byte of information i.e. it is a one byte transfer path.

2.1.1 Data Bus Group

The Data Bus Group consists of modules of conductors capable of transferring data at 50 MBs. Multiple Data Bus Groups may be coupled to achieve higher transfer rates. In a half duplex configuration, when a slave is selected, each additional Data Bus Group shall assert its bus number (1 to n). Bus ID 1 is the first expansion Data Bus Group. The master is assumed to check that all data buses are operational and that they are in the proper sequence, none are missing, and there are no duplicates.

2.1.2 CONTROL OUT

This conductor is used by the master to advise the state in which the equipment is operating.

States initiated by the master are:

BUSCTL
IDLE
~~DAT~~ IDS
PDS
REQUEST
SELECT
XFRRDY
MASTEND

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.3 CONTROL IN

s conductor is used by the slave to advise the state in which the
ipment is operating. These states are operated by a slave in response to
rations initiated by the master and indicate that the slave is
rational and available for Information Transfers.

tes initiated by the slave are:

BUSACK
IDLE
DESEL
RESETSEL1
SLAVACK
SLAVEND
XFRST

.4 Burst Control

.4.1 PDS (Prolong Data Streaming)

n this state is active, the master is indicating to the slave that the
rent data burst is to be continued and that the normal burst ending
uence and bus controls states are to be avoided so that the burst
nsfer rate can be maintained.

.4.2 IDS (Interrupt Data Streaming)

s state is asserted by the master to indicate to the slave that the
rent burst is to be interrupted at the earliest possible time by the
ve. The master has a need to perform some other operation(s) before
uming the data burst transfer. When the master re-initiates the
ormation Transfer sequence, this burst will be continued by the slave. It
not possible for the master to initiate transfer of another burst unless
Initialize sequence precedes the Information Transfer.

3. Transaction Examples

In the following sequences, the boxes slanted to the left are states asserted by the master, slanted to the right are asserted by the slave, and rectangular boxes represent bytes of information.

3.1 Slave Selection

The master asserts a SELECT state as the first byte on CONTROL OUT followed by a one byte slave address. The slave responds by asserting the SLAVACK state, followed by its selection address.

The SELECT state, followed by the selection address will be repeated on CONTROL OUT until the slave acknowledges selection on CONTROL IN or the master chooses to deselect (timeout).

In a simplex or full duplex configuration this sequence need be executed only once after power on or a reset, to originate the connection between master and slave.

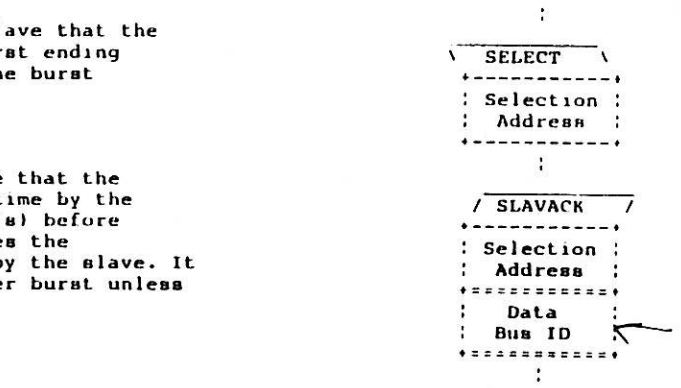

Figure 3-1 Selection Sequence

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annel Deselection

ister asserts the DESEL state on CONTROL OUT. The slave responds serting the IDLE state. The DESEL state may follow selection or at the [Information Transfer.

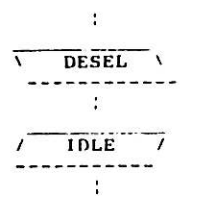

Figure 3-2 Deselection Sequence

nitialize Sequence

aster asserts REQUEST state followed by the slave address to initiate a ata transfer control operation in the slave e.g. if a data stream has interrupted and the master requires that a different data burst fer is to begin. Initialization is not required between successive s with the same slave. NOTE: A slave may be deselected between rupted streams.

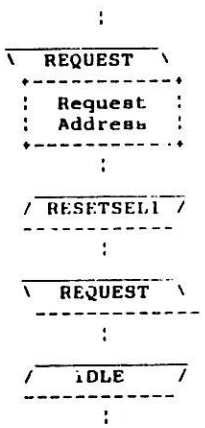

Figure 3-3 Initialization Sequence

3.4 Information Transfer

3.4.1 Normal Information Transfer

The master asserts the BUSCTL state followed by the Bus Control byte for the Information Transfer request. The slave responds, with BUSACK, followed by the Bus Acknowledge byte. The master acknowledges acceptance by asserting XFRRDY to begin an Information Transfer. The slave asserts XFRST. If the transfer direction is Out, the master initiates the Information Transfer on the data bus. If the transfer direction is In, the slave initiates the Information Transfer on the data bus.

The first word transferred contains the length of the packet and Command Reference Number of the Information Transfer being executed. The second word contains the address of the ultimate destination. NOTE: The selection mechanism ensures point to point connectivity with a limited number of masters and slaves. The 48 bit address is used to identify a destination in a network implementation). If the configuration is limited to that of the selection, then the address will be the same as that of the selected slave.

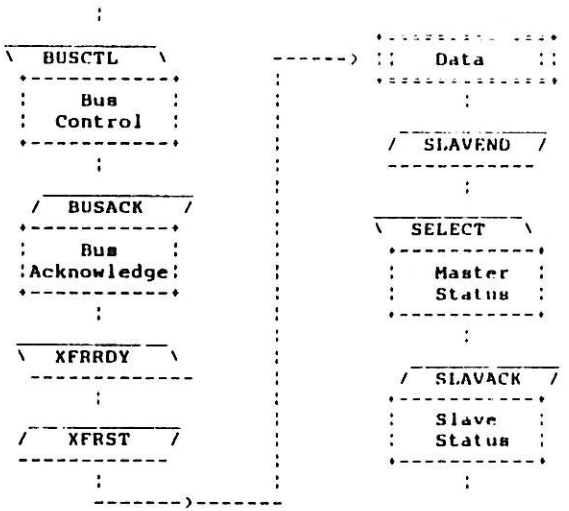

Figure 3-4 Normal Data Streaming Sequence

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Prolonged Data Streaming

: master wishes to stream data continuously then it asserts the PDS
on Control Out during an Information Transfer. The slave shall
ize this as an indication that the master wishes to continue transfer
: next burst (if any) without a control sequence at the end of the
it burst. This state occurs asynchronously to the Information Transfer

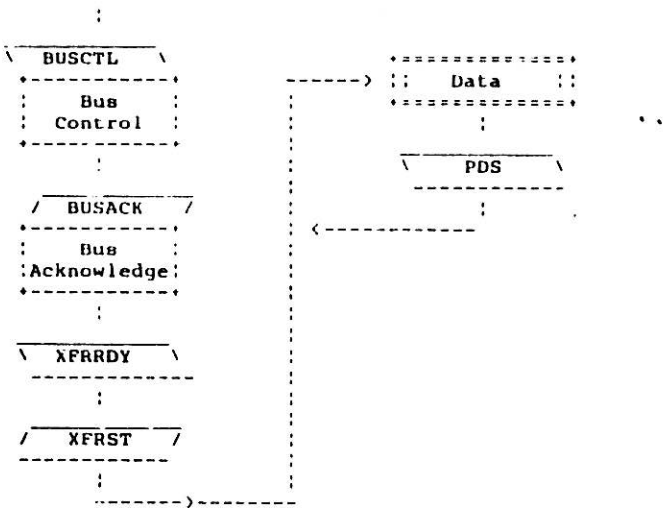

Figure 3-5 Prolonged Data Streaming Sequence

3.4.3 Interrupt Data Streaming

If the master wishes to interrupt the data stream then it asserts the IDS state on CONTROL OUT during an Information Transfer. The slave shall recognize this as an indication that the master wishes to interrupt the transfer of the current burst. This state occurs asynchronously to the Information Transfer.

The master may resume the Information Transfer by re-initiating the transfer sequence. The slave shall resume transmission at the point it ceased. An initialization sequence is required if the master wishes to change to a different Information Transfer, or begin the same burst at the beginning.

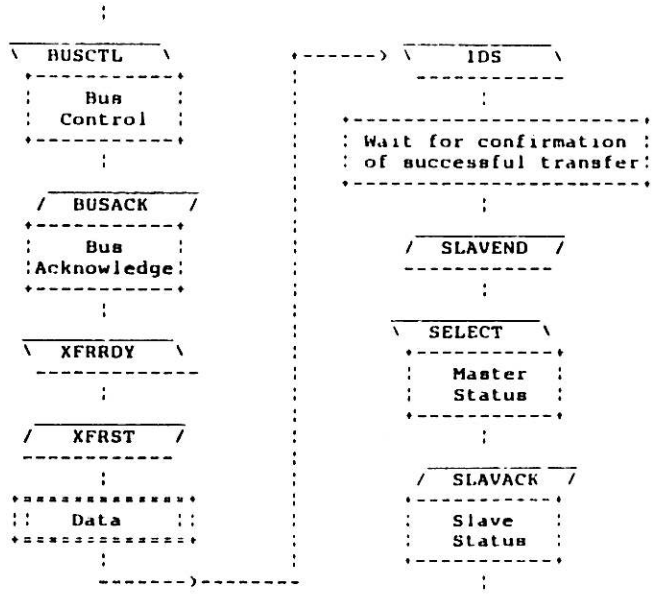

Figure 3-6 Interrupted Data Streaming Sequence

ATTACHMENT 5
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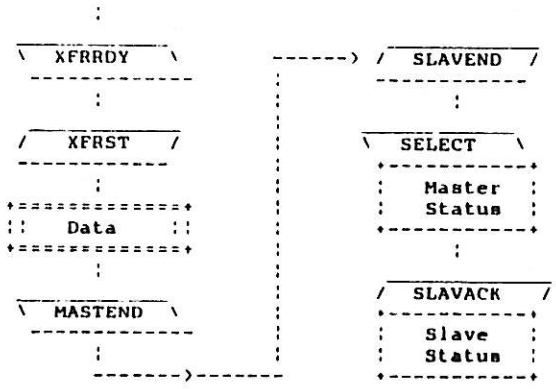
3.5 Information Transfer Timing

Data encoded by the TAXI chip is self-clocking. Strobing of data is done on a byte or word basis.

Timing charts and specific values for rise/fall times, clearing of cable delays, skew per cable etc to be specified by Law of Physics Working Group.

3.6 Unexpected Termination of Transfer

If the slave detects an error during transmission it terminates the Information Transfer and the contents of the Slave Status byte advises the master of possible cause. If the master detects an error during transmission or wishes to cease the transfer it initiates the termination by the MASTEND state. The slave terminates the sequence in a normal manner.



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4. Physical Specifications

4.1 Electrical

This proposal is based upon use of the AMD TAXI chip to serialize and deserialize the data. This part is currently available. Other competitive components offering similar capabilities are anticipated in the next two years.

Input to the TAXI chip is byte wide and the output is an encoded bit serial data stream suitable for export over coaxial or fiber optic cables. Each bit serial stream is rated at 12.5 MBs, thus a Data Bus Group need consist of only four conductors.

Suitable transmitters/receivers are needed to support the physical medium chosen.

4.1 Cable and Connector Specifications

The cables and connectors are TBS.

A suitable coaxial implementation may be satisfied with the IBM BMC (Block Multiplexer Channel) cables. A BMC consists of two cables, each with 24 coaxial conductors and serpentine connectors.

A half duplex configuration or simplex needs only one pair of conductors for control so 20 remaining could be used to achieve 250 MBs with 5 Data Bus Groups. Full duplex operation would require both cables of the BMC.

In the same cable/connector packaging as an IBM BMC which is currently limited to 3 MBs (4.5 MBs from Amdahl and 6 MBs from NAS), the ENDL-HSC uses the proposed state machine and TAXI chips to offer a 500 MBs transfer rate.

It is desirable that a more compact form factor be used to suit the smaller cabinetry of today's computers. Recommendations on these is solicited from connector and cable manufacturers.

Parallel fiber is becoming available and may be used for longer distances. Cable size is significantly smaller than coaxial but connectors are not very small. A package of 10 would provide one control pair and two Data Bus Groups so would provide a 100 MBs half duplex or simplex configuration.

A 12 conductor configuration could contain two ENDL-HSCs with one Data Bus Group each and offer a 50 MBs full duplex configuration.

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Application #1

HSC Attributes needed:

1. 100 MBytes/s burst bandwidth
2. High sustained bandwidth
3. Minimal error checking
4. Very large packets (3 MByte)
5. Mostly unidirectional data flow

1K x 1K pixels = 1M pixels per frame

8 bits each of red, green, blue per pixel ==> 3MBytes per frame

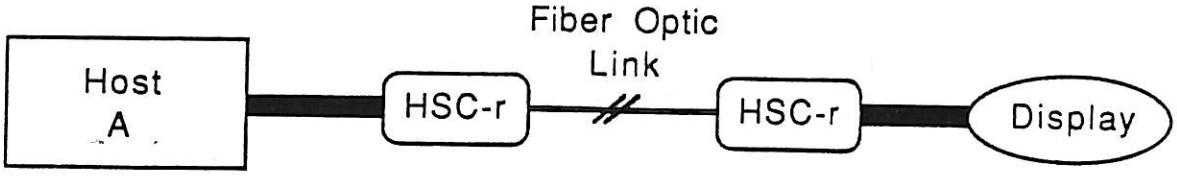
@ 18 frames per second ==> 54 MBytes per second

@ 24 frames per second ==> 75 MBytes per second

@ 30 frames per second ==> 90 MBytes per second

512 x 512 x 8 bits x 30 frames/s ==> 8 MBytes/s

Application #2



Functions of HSC Fiber Optic Repeater (HSC-r)

1. Accept parallel data from HSC

2. Format accordingly and send over long distance fiber at full HSC bandwidth

3. Recover signal from fiber and convert back to HSC, including control signals

Additional HSC Attributes needed:

1. Error checking sufficient to identify failing units.

Application #3

Additional HSC Attributes needed:

1. Bidirectional data path (full-duplex is preferred)

2. Ability to pass small (1024 Byte) packets as well as large packets

Application #4

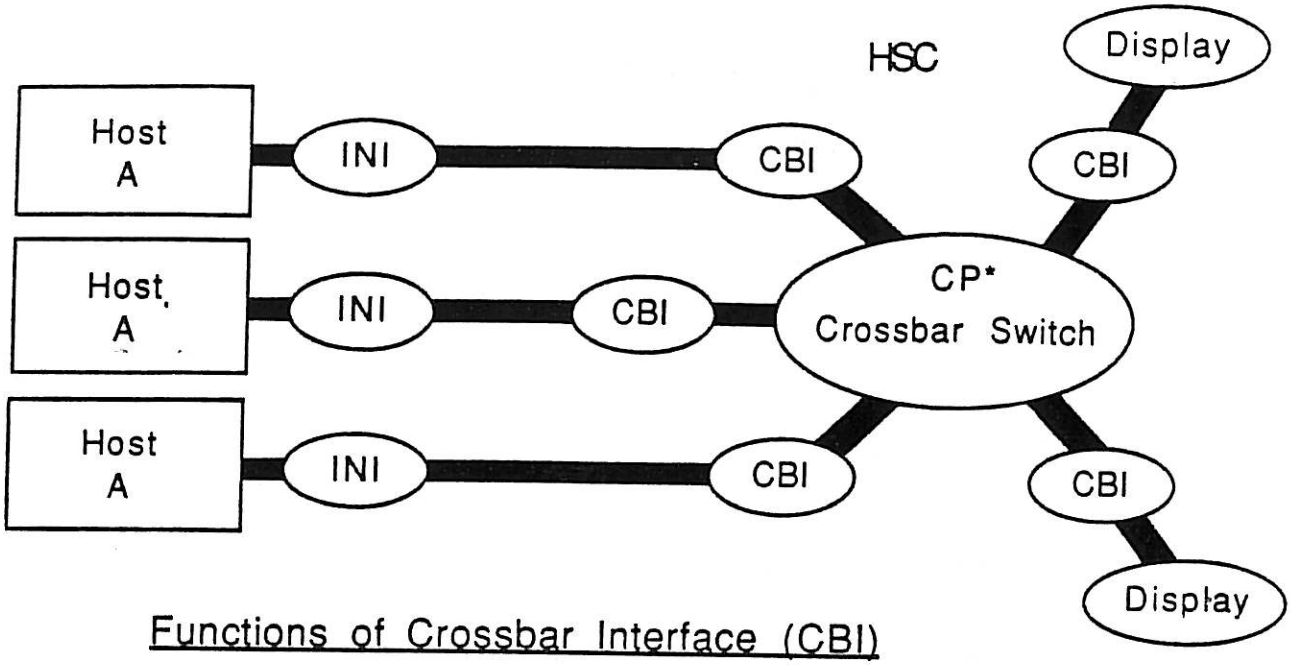
Functions of Intelligent Network Interface (INI)

1. Buffer the data
2. Accept native host sized transmissions, and split to HSC size (optional)
3. Generate/check checksums (optional)
4. Execute Data Link Layer and above protocol (optional)
5. Convert between Native Host Channel and HSC (optional)

Additional HSC Attributes needed:

1. Independence from upper layer protocols

Application #5



Functions of Crossbar Interface (CBI)

1. Buffer the data
2. Execute Data Link Layer protocol to generate an address for the crossbar
3. Check security of data path
4. Hardware will be very similar to INI

Additional HSC Attributes needed:

1. Convey an address to the crossbar
2. Unidirectional signal lines on HSC
3. Copper version of HSC

Los Alamos HSC Requirements

1. 100 MByte/s burst bandwidth
2. High sustained bandwidth over several kilometers
3. Talk to a crossbar switch
   * Copper version of HSC
   * Unidirectional signal lines on HSC
   * Address independent from upper layer protocols
4. Bidirectional data path
5. Error checking to identify failing hardware

NEW PRODUCT OFFERING

High Speed Parallel Port (HSP)

- Provides high bandwidth I/O
  - o Burst transfer rates of 80 MB/s
  - o Data transfers up to 1 GB in length

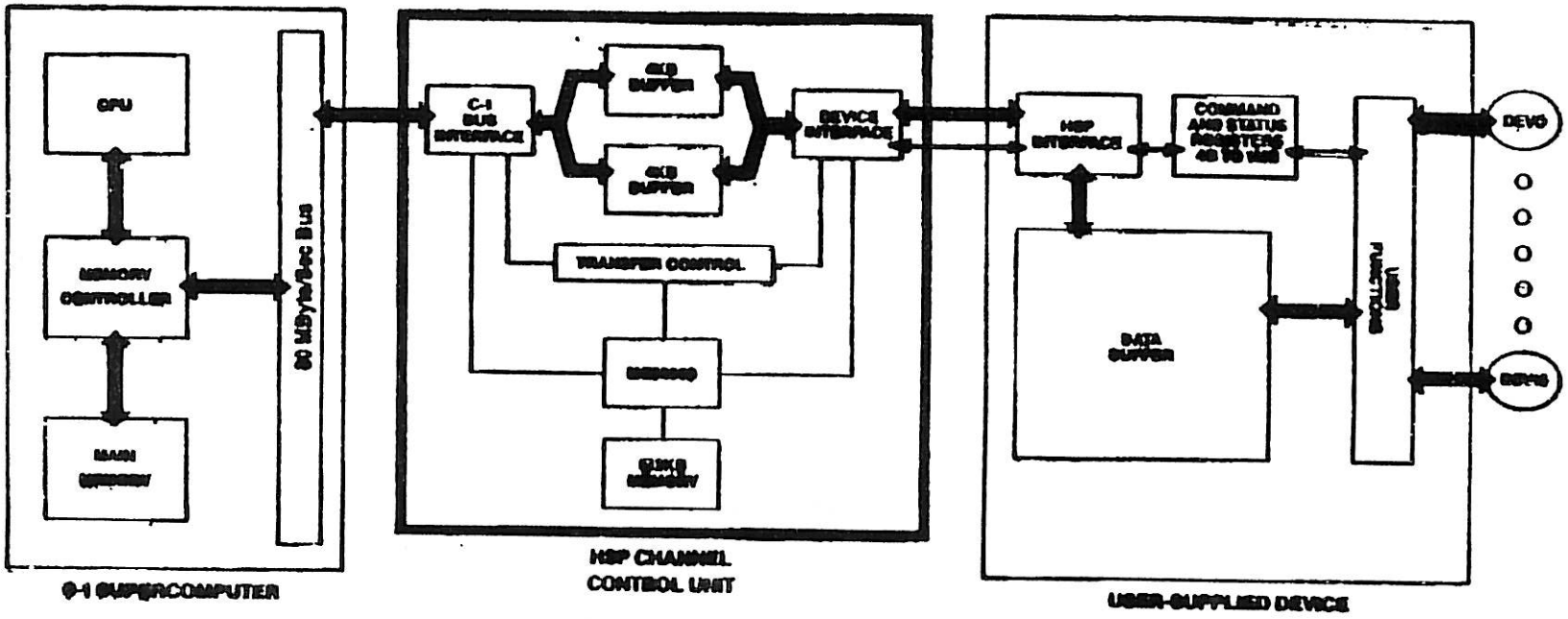
- 64 bit data bus with byte parity
  - o Asynchronous control transfers
  - o Synchronous block data transfers

NEW PRODUCT OFFERING

HSP

- Point to point interconnect
  - o Differential line drivers and receivers
  - o Max cable length over 100 feet
  - o 16 independent DMA channels

HSP Block Diagram



CONVEX

Jul 29, 1986

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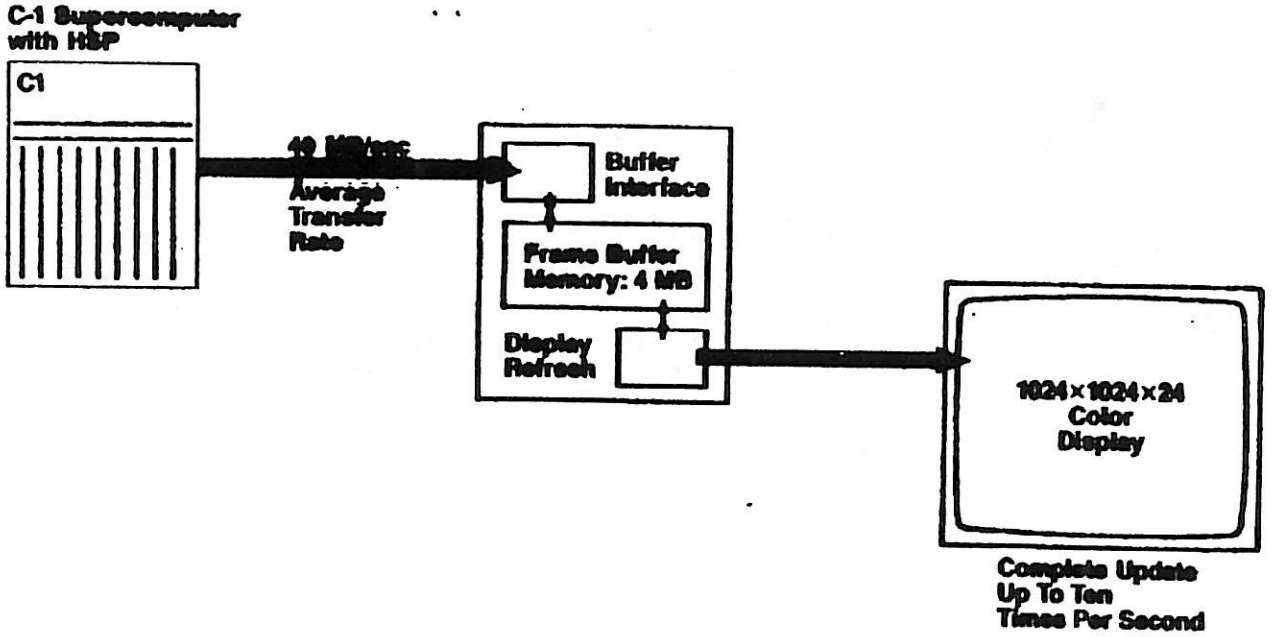
C-1 / HSP Application: Display Update



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Jul 28, 1986

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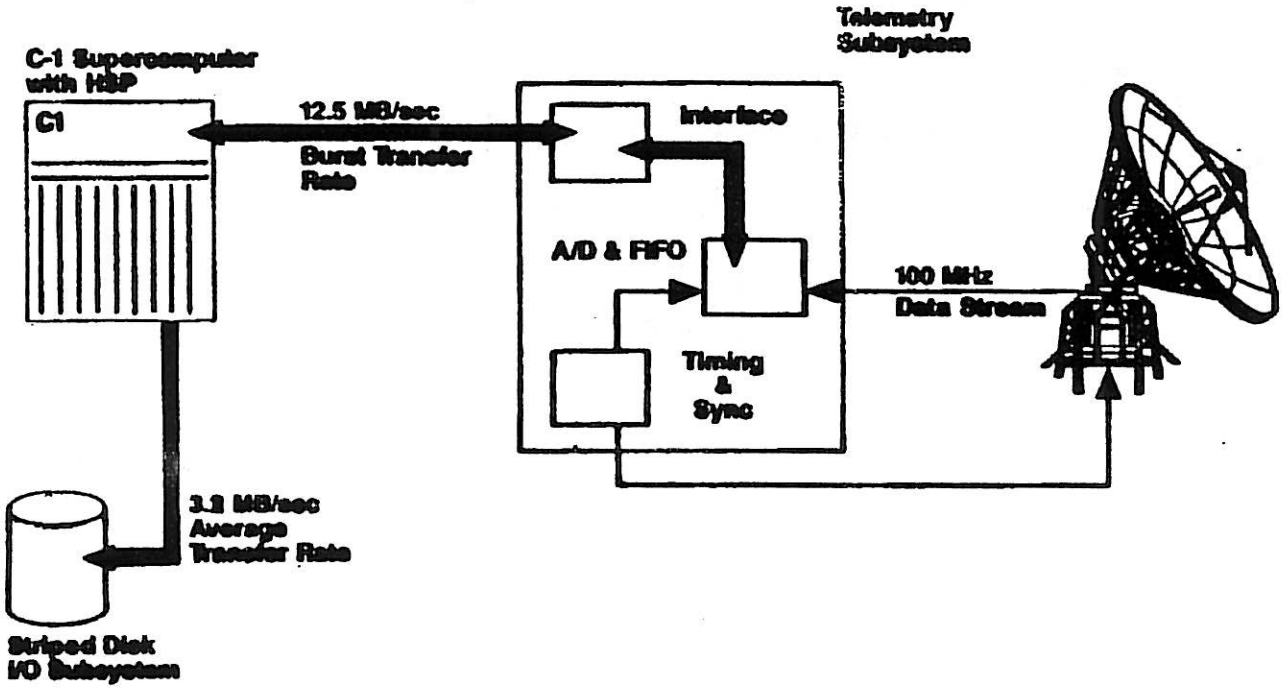
C-1 / HSP Application: High-Speed Data Acquisition



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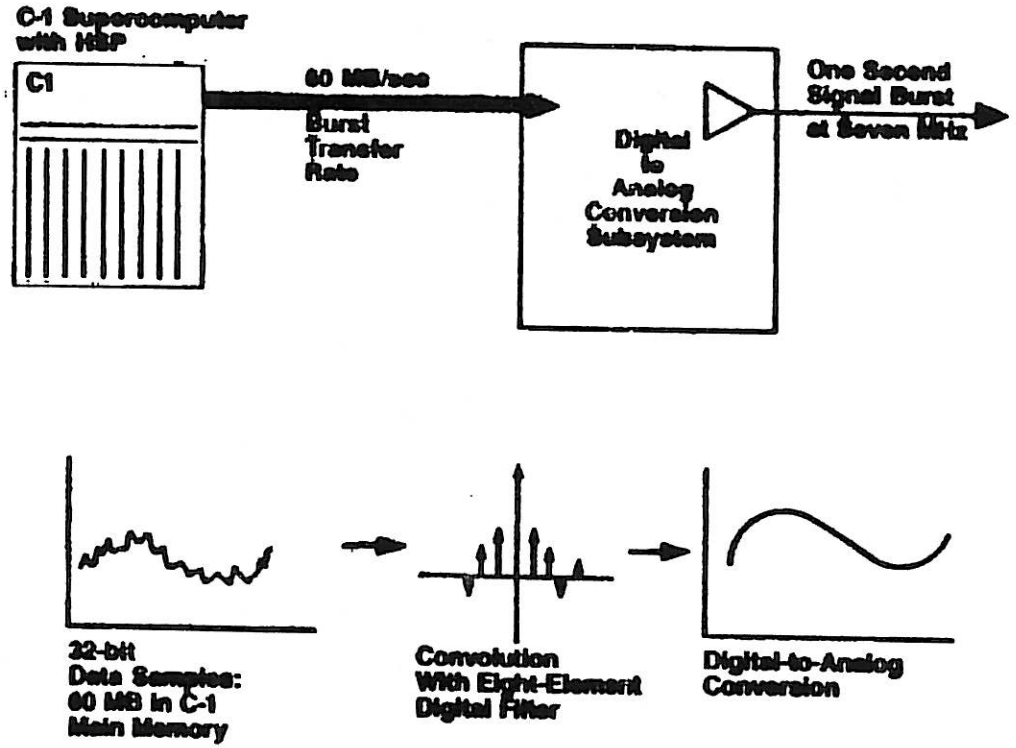
C-1 / HSP Application: Signal Synthesis



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SERVICE INTERFACE

- DATA WORD WIDTHS: 16, 32, 64 BITS
- NO SPECIFICATION OF AUTOMATIC WORD WIDTH CONFIGURATION

PHYSICAL LAYER

- 40 NANOSECOND WORD TIMING
- LOW RAW ERROR RATE (10^{-15} TO PROTOCOL LAYER)
- LOW UNDETECTED ERROR RATE (10^{-21})
- NOT DESIGNED FOR MULTIDROP
- COPPER INTERFACE TO BE STANDARDIZED FIRST
- TIMING OF FIBER STANDARD TO BE EVALUATED
- HALF DUPLEX DATA SIGNALS TO BE EVALUATED
- COPPER MEDIA LENGTH $\geq$ 25 METERS

PRINCIPLES

- K.I.S.S. (KEEP IT SIMPLE-STUPID)
- DEFINE MINIMUM SET OF PROTOCOL — PHYSICAL INTERFACE DEFINITION

BOB GROW
GP ASSOCIATES

HSC GOALS & ASSUMPTIONS

HSC SPEEDS OF 50, 100, AND 200 MBYTE

HSC IS A POINT-TO-POINT INTERFACE

THE INTERFACE WILL SUPPORT NETWORK ACCESS

THE STANDARD WILL DEFINE A LAYERED ARCHITECTURE

- OSI CONFORMANCE NOT REQUIRED
- PROTOCOL ("LINK") LAYER
- PHYSICAL LAYER

PROTOCOL LAYER

- SUPPORT EFFICIENT MULTIPLEXING (DATAGRAM)
- NO SPECIFICATION OF AUTO CONFIGURATION
- APPROPRIATE TIMING AND ADDRESSING FOR NETWORK
- APPROPRIATE CONTROL SIGNALLING FOR PHYSICAL SERIALIZATION
- SUPPORT MEDIA LENGTH $\simeq$ 2 km
- MINIMIZE MESSAGE LATENCY

BOB GROW
GP ASSOCIATES

DAL ALLAN'S CONFIGURATIONS SLIDE

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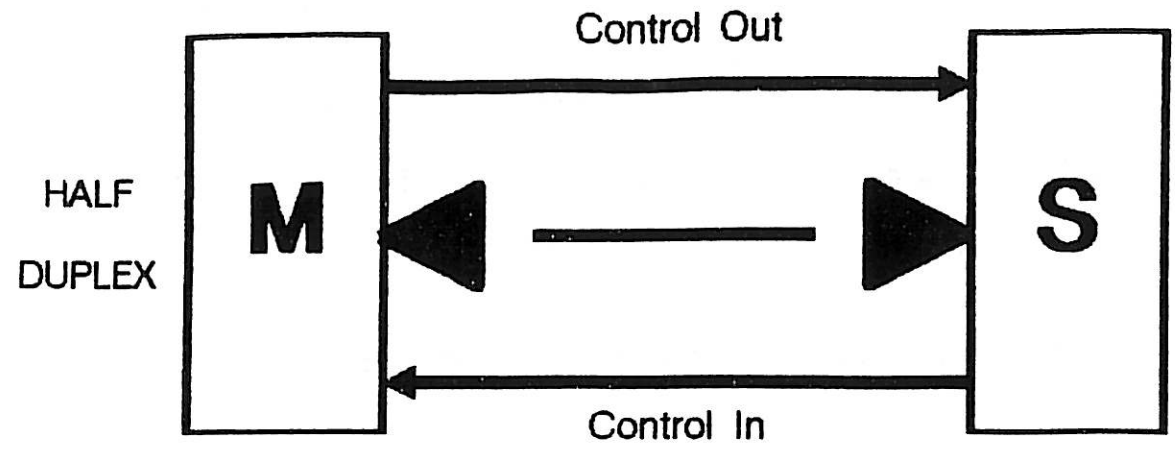

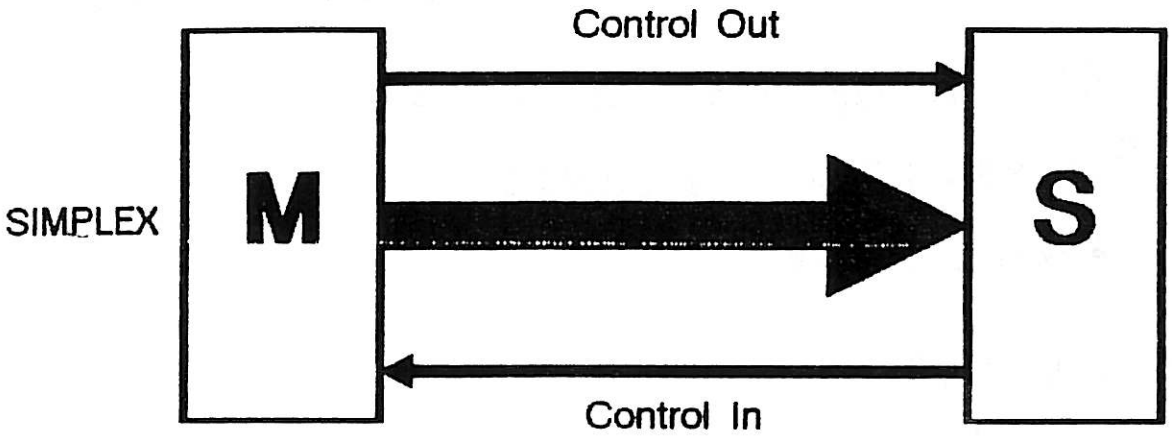

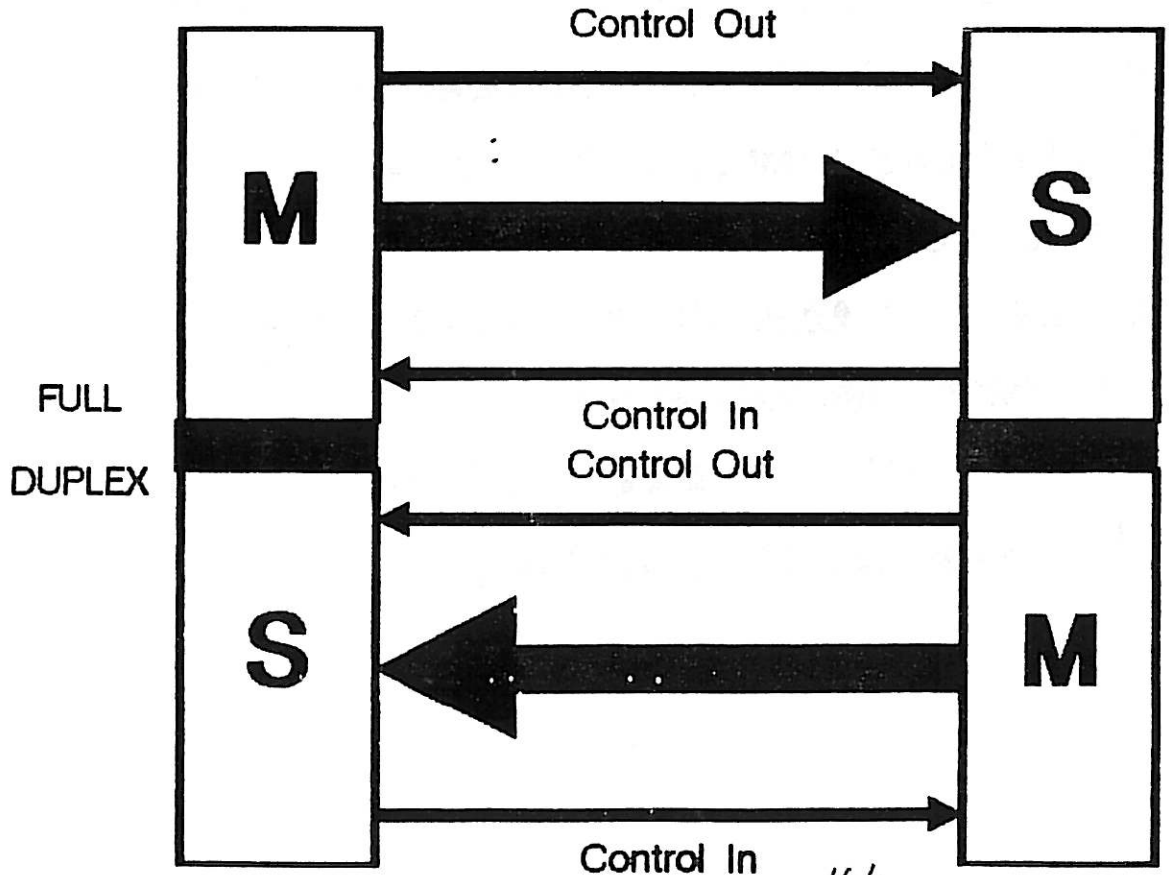

Classic Consulting International
203-788 Beatty Street, Vancouver, B.C., Canada V6B 2M1 (604) 682-2600
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A.N.S.I. X3T9 MEETING - AUGUST 17 - 21, 1987

THE CLARION HOTEL
2886 SOUTH CIRCLE DRIVE
COLORADO SPRINGS, COLORADO
80906
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The August A.N.S.I. X3T9 meeting, hosted by Gary Robinson of D.E.C., will be held at the Clarion Hotel in Colorado Springs, Colorado. The hotel is located in the beautiful, natural setting of the Rocky Mountain West, and is both a full service recreational facility, and conference centre.

The Clarion Hotel offers a complimentary airport shuttle service to and from the Colorado Springs Municipal Airport, a quick seven minute ride away. To contact the hotel, just pick up the courtesy telephone marked "The Clarion Hotel", located in the main baggage area of the Airport terminal (near the rent-a-car services).

If you rent a car:

- exit the airport and continue driving straight down Fountain Drive,
- when you reach Circle Drive, turn left and continue driving towards the sixth set of lights (approximately),
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The A.N.S.I. X3T9 attendees will receive a very special rate of $75.00 single occupancy and $85.00 double occupancy, including tax. Please use the pre-printed reservations cards to make your reservations. If you make your reservation by telephone, please be sure to tell the reservation clerk that you are with the A.N.S.I. X3T9 meeting.

The reservation cut-off date is July 26, 1987. Reservations made after this date will be subject to space and rate availability.

If you have any question, please contact:

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