Serial ATA II:
Cables and Connectors volume 1

Revision 1.0

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This 1.0 revision of the Serial ATA II: Cables and Connectors volume 1 ("Final Specification") is available for download at www.serialata.org.

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1. Serial ATA II Cables and Connectors Introduction

This specification defines enhancements to the Serial ATA 1.0 specification that provides capabilities required to enable Serial ATA in server and networked storage solutions while retaining Serial ATA 1.0 compatibility and desktop cost structure.

Requirements for this specification are:
- Maintain compatibility with Serial ATA 1.0
- New features/capabilities must be separable/optional proper supersets of 1.0
- Support the topologies expected for enterprise applications as shown in Serial ATA II Use Cases
- Support efficient connectivity of large number of drives
- Provide performance features enterprise-class systems
- Provide a means to supporting industry-standard enclosure services and device management services

Additional features and capabilities are defined in a way that allows them to be selectively deployed, as business and market conditions require. Capabilities are defined in a way that costs associated with new feature support are incurred where the benefit/value is realized.

1.1. Serial ATA II Cables and Connectors - Goals, Objectives, Constraints

- Support Serial ATA II Use Cases - Provide cable/connector schemes for multiple S-ATA channels with industry standard pin/conductor definitions which support the Serial ATA II Use Cases
- Time to market - Standard in place quickly to support emerging S-ATA storage enclosure and appliance early adopters.
- Inside the box – HBA/Motherboard to Backplane
- Within the Rack Enclosure – from server to adjacent JBOD within the same rack enclosure
- Contain cost of Inventory, minimize SKU proliferation
- Impose NO additional requirements on HDD (i.e. no HDD design changes to support grounding and extended signaling capabilities)
- Price Goals – less than equivalent SCSI-160 implementations
- Where possible, re-use existing proven designs (those already in high volume production, with established reliability)

1.2. Non-Goals

- Power distribution
- Definition of specific product implementations

1.3. Specification Overview, List of Services and Schedule

1.3.1. Features defined in this document include:
1. Connector locations on devices, keep out zones for mating
2. Multiple Channel Plug Stacking specification – connects a multiple channel RAID Host bus adapter to an internal backplane.
3. Backplane Connector

1.4. Conventions, Definitions, Dimensions and References

1.4.1. Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this document have a specific meaning beyond the normal English meaning. These words and terms are defined either in the definitions section or in the text where they first appear. The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE).

Precedence - If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and *then* text. If there is a direct contradiction between this specification and the Serial ATA 1.0 specification not accompanied by statements clearly indicating that this specification is changing the Serial ATA 1.0 standard, the precedence shall be the Serial ATA 1.0 specification.

Keywords - Several keywords are used to differentiate between different levels of requirements and optionality.

Expected - A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

Mandatory - A keyword indicating items to be implemented as defined by this standard.

May - A keyword that indicates flexibility of choice with no implied preference.

Optional - A keyword that describes features that is not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

Shall - A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

Should - A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase "it is recommended".

1.4.2. Dimensions

All dimensions are shown in millimeters unless otherwise noted.

1.4.3. References

This specification is an extension to the Serial ATA 1.0 specification. The Serial ATA 1.0 specification is presumed as the underlying baseline for this specification. This specification makes reference to the following specifications:

Serial ATA: High Speed Serialized AT Attachment revision 1.0. Available for download at www.serialata.org.

2. Connector Locations and Keep out Zones for mating

2.1. Purpose

This section is intended to ensure mating of devices to backplanes with proper mechanical and electrical interface and without physical conflict, the no encroachment area and its Z-dimension to a nominally flush receptacle shall not be occupied by any device materials or construction that might create a physical conflict.

2.2. Keep Out Zones on Devices
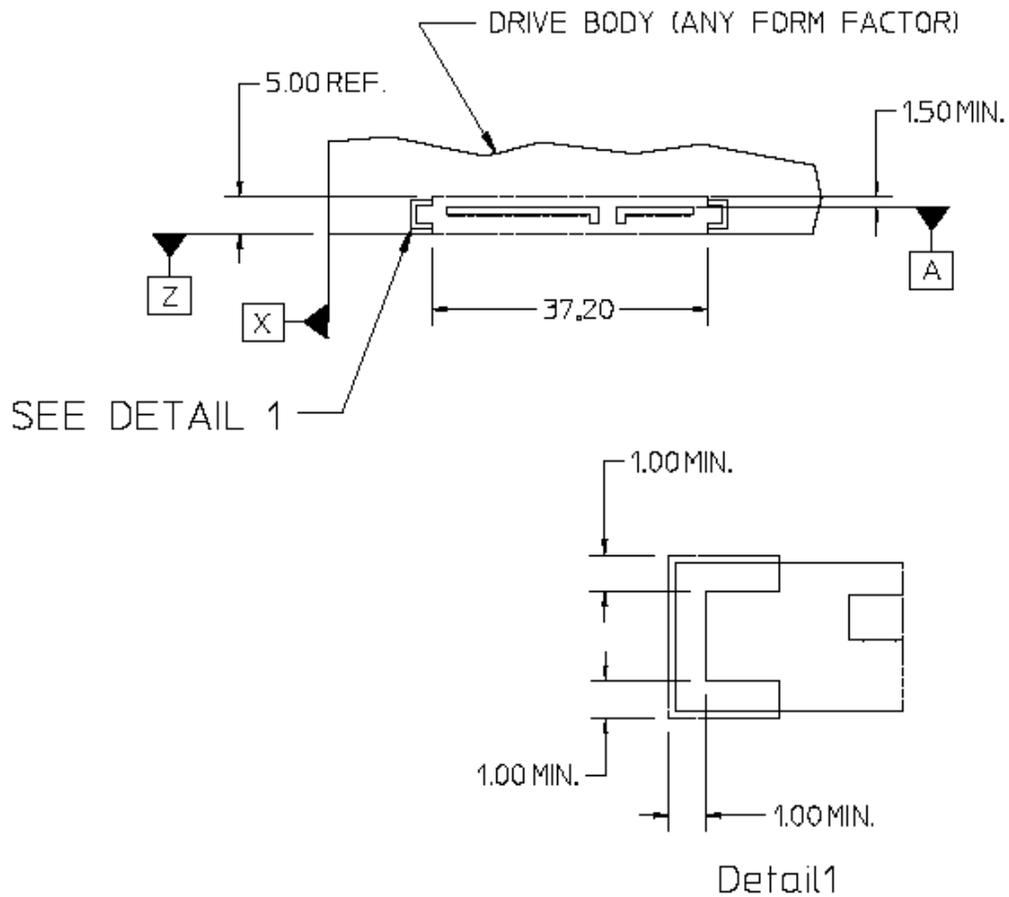
Figure 2.1 – Device Connector Keep out zones

2.3. SATA connector location on the 5.25" form factor

Compliant 5.25" form factor Serial ATA Devices <u>shall</u> have connector locations and keep out areas as follows. The SATA connector is nominally flush with the I/O connector end of the device form factor.
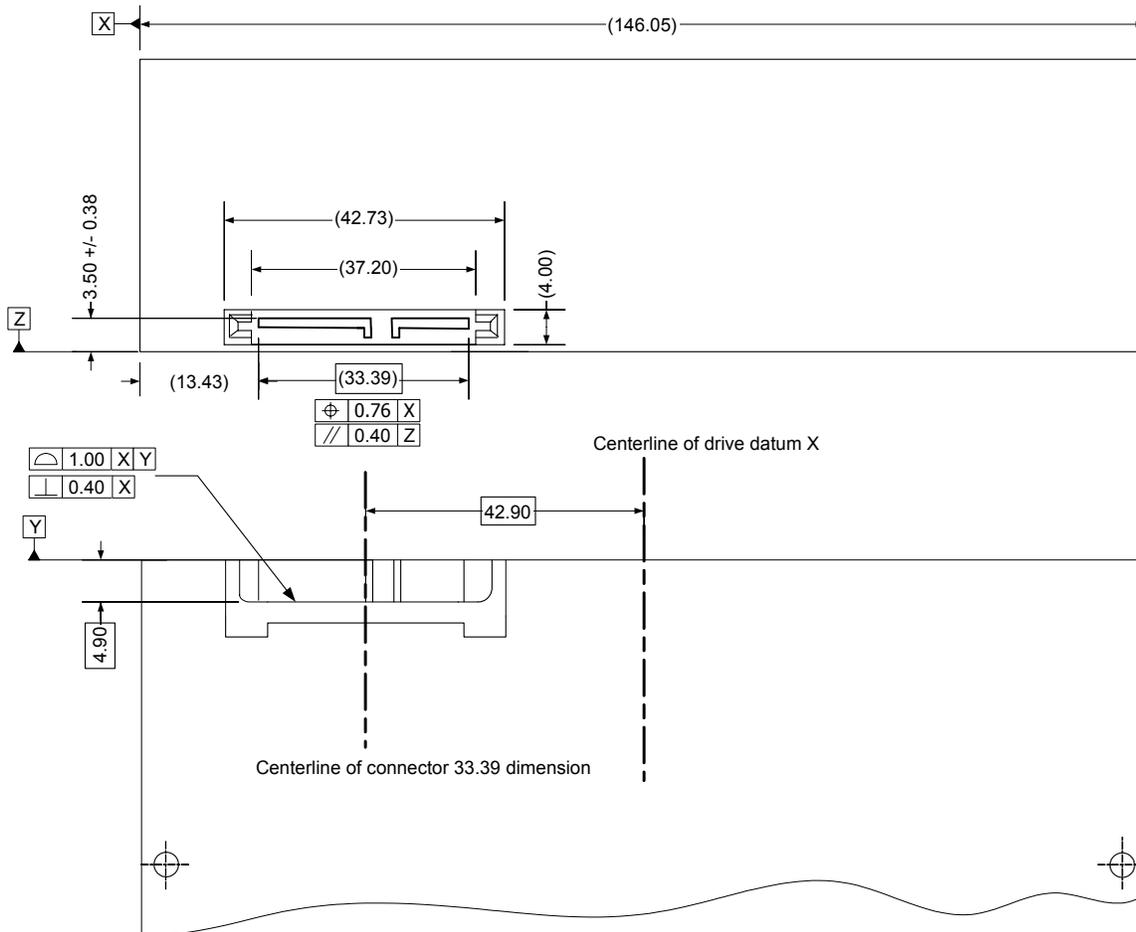
Figure 2.2 - SATA connector location on the 5.25" form factor.

3. Ganged internal plug stacking

3.1. Purpose

The purpose of this optional feature is to conserve motherboard, HBA and I/O controller printed circuit board space to support system density and size goals for such products. As Serial ATA requires a separate channel for each device connected to a controller or motherboard and it is expected that many connectors may consume large amounts of board space. Also, standard, high volume cables will be used wherever possible to contain the system cost.

There are two design goals …

1 - Maximize the density of connectors on printed circuit boards

2 – Allow optional use of standard PC-class cables where applicable and avoid the requirement for low volume, higher priced, specialty cables.

To be interoperable with this ganged internal plug stacking specification, printed circuit boards, including Adapter Boards, Motherboards and Device Backplanes, <u>shall</u> be capable of accepting multiple individual cables as specified in Serial ATA 1.0. And they <u>should</u> be capable of accepting multi-channel cable assemblies with multiple channel connectors as indicated in the conceptual figure below. Implementers of use cases with passive backplanes with additional connectors <u>shall</u> ensure electrical compliance to Serial ATA 1.0 specification at the HBA connector and at the HDD connector.
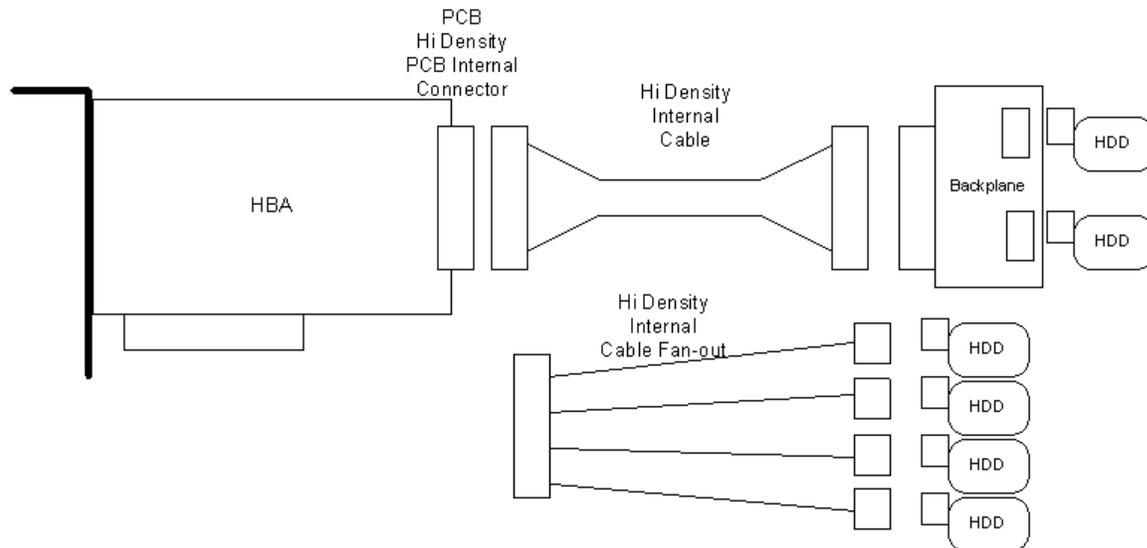
Figure 3.1 – Ganged internal plug stacking
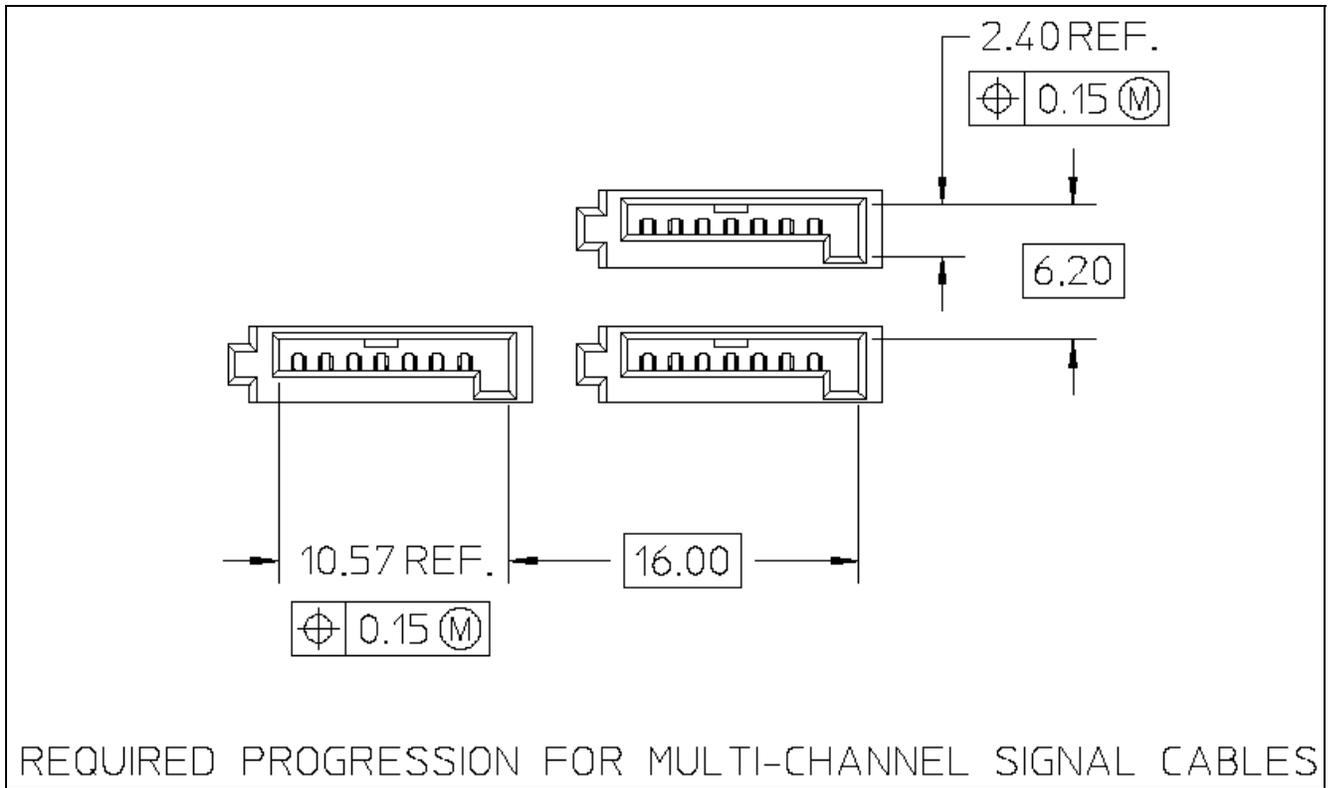
Figure 3.2 - Required Progressions for Ganged internal stacking <u>Cables</u>
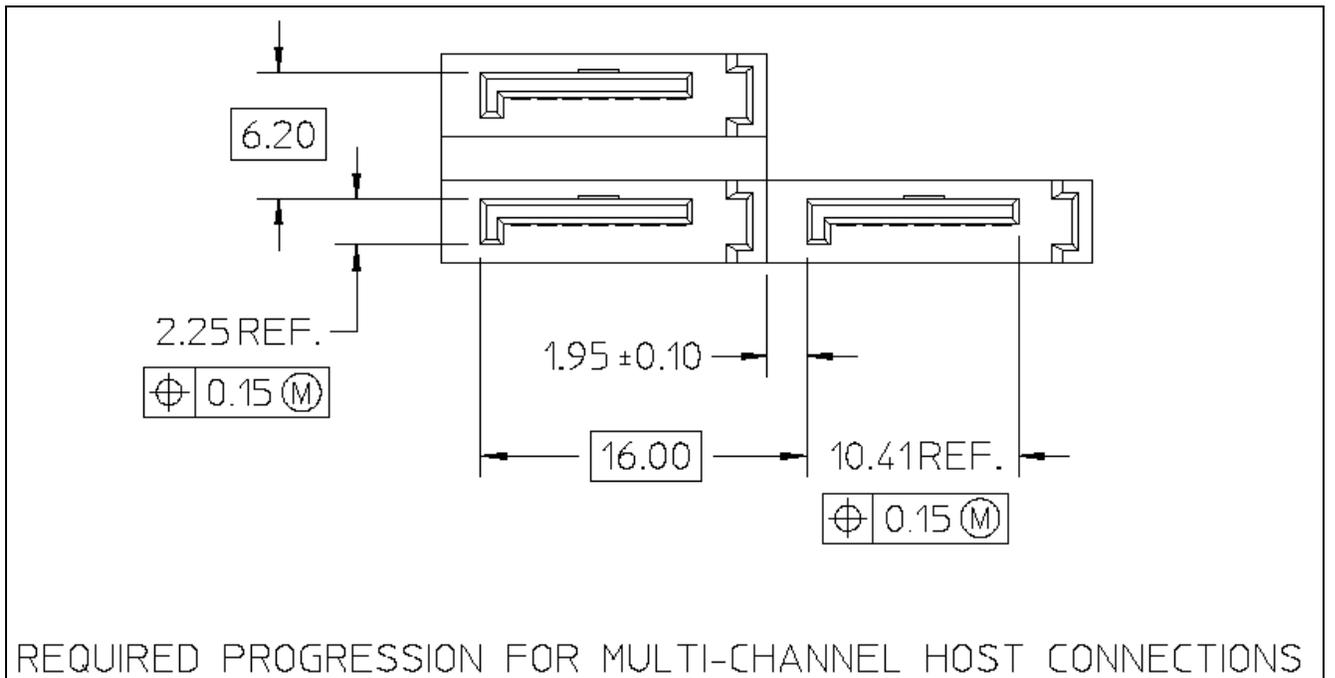
Figure 3.3 - Required Progressions for Ganged internal stacking plugs

4. Backplane Connector

4.1. Purpose, Scope and Goals

The purpose of this **optional** feature is to specify the IO Connectors (show with heavy outline below) that provide interconnection for power, data and enclosure services between I/O controller(s) and a Serial ATA disk backplane. This specification will define interoperability between I/O modules from one manufacturer, which will work with backplanes from a different manufacturer. This interoperability will include electrical, mechanical and enclosure management connections. Compliant I/O controllers and Serial ATA backplanes <u>shall</u> adhere to the specified connector placement, and connector pinout.
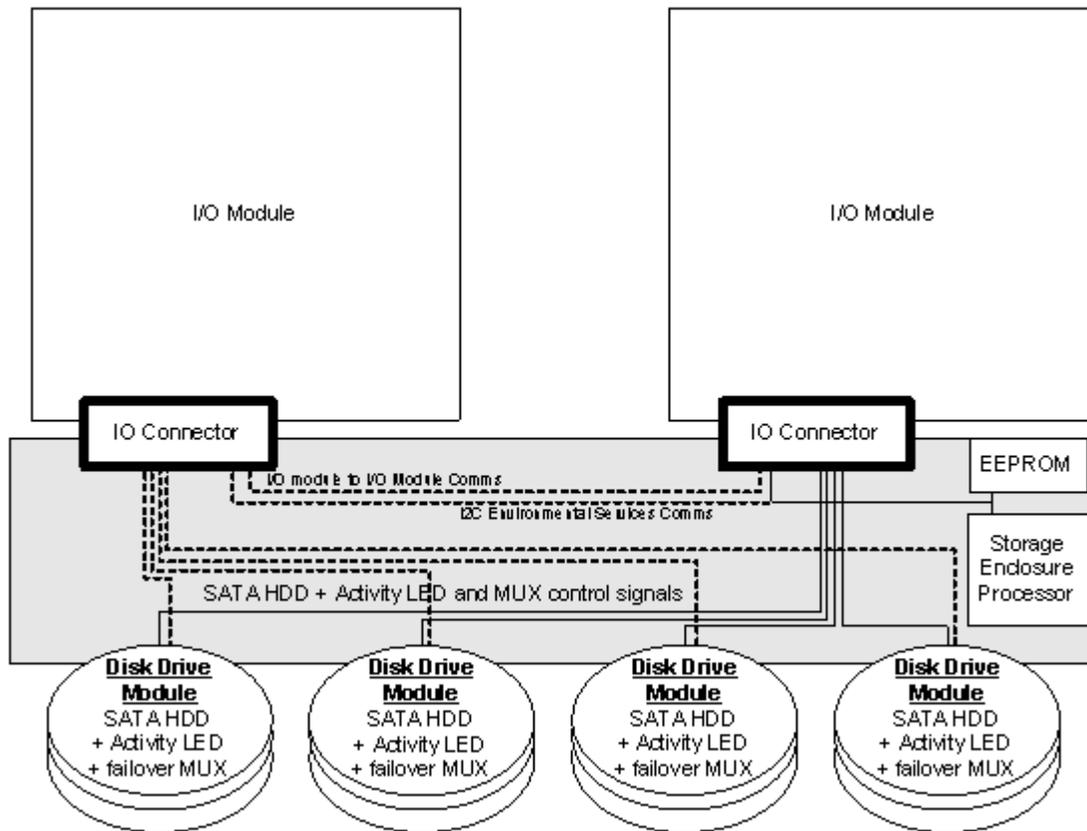
Figure 4.1 – Concept summary interconnect structure

❑ The I/O connector(s), shown in Figure 4.1 with the heavy outline, are the central items being specified.
❑ The I/O Module in dotted line format represents a secondary and optional I/O module.
❑ The shaded area represents the backplane.
❑ The Disk Drive Module is envisioned as a Standard Serial ATA Hard Disk Drive (HDD) within a carrier, including a power connection between the module and the backplane, including a data connection between the module and the backplane, probably including HDD activity LED, possibly including a failover Mux with a secondary data connection to the backplane.

4.1.1. The goals and objectives

- Define connector type, signal descriptions, connector locations and connection pinout
- Define a connection interface between the I/O controller and the enclosure backplane
- Ensure adequate flexibility to optionally implement storage enclosure features such as failover, I/O controller hot-swap, and disk and enclosure management.
- Use common electrical interfaces and protocols.
- Define a mechanical envelope for the I/O controller to allow interoperability with enclosures developed to this same definition.
- Define a power envelope for the I/O controller to allow interoperability with enclosures developed to this same definition.
- Define a software interface between the I/O controller and the enclosure management processor.

4.1.2. Non-goals

- This specification is not intended to define interoperability between I/O modules from separate vendors, which might co-exist within the same enclosure (in the case of multiple I/O controller enclosures).

4.2. Supported Configurations

Two configuration goals are supported by the connector specification:
1. Single I/O Controller System
2. Dual I/O Controller System with redundancy features (optional)

Each implementation will have mandatory and optional features supported through the use of the available signals.

4.2.1. Single I/O Controller Signals

- Serial ATA interface
- I/O controller to enclosure processor (SEP) communication
- Disk activity LED signals.
- I/O controller power and ground
- I/O controller identification and control (RESET)

Single I/O
Controller

FRU_ID_SCL
FRU_ID_SDA
ENC_PROC_SCL
ENC_PROC_SDA

ACT_LED_DR(15:0)_L

IO_SATA_Tx(15:0)+/-
IO_SATA_Rx(15:0)+/-
BOX_ID_BIT(2:0)

IO_SLOT_0_L = Low (Gnd)
ACT_LED_HOST_L

ES Processor

BOX_ID_BIT(2:0)
FRU_ID_SCL
FRU_ID_SDA
ENC_PROC_SCL
ENC_PROC_SDA

EEPROM

ENC_PROC_SCL
ENC_PROC_SDA

Disk Drive (1..16)
with MUX & Activity LED

Activity LED (optional)

SATA Rx+/-
SATA Tx+/-
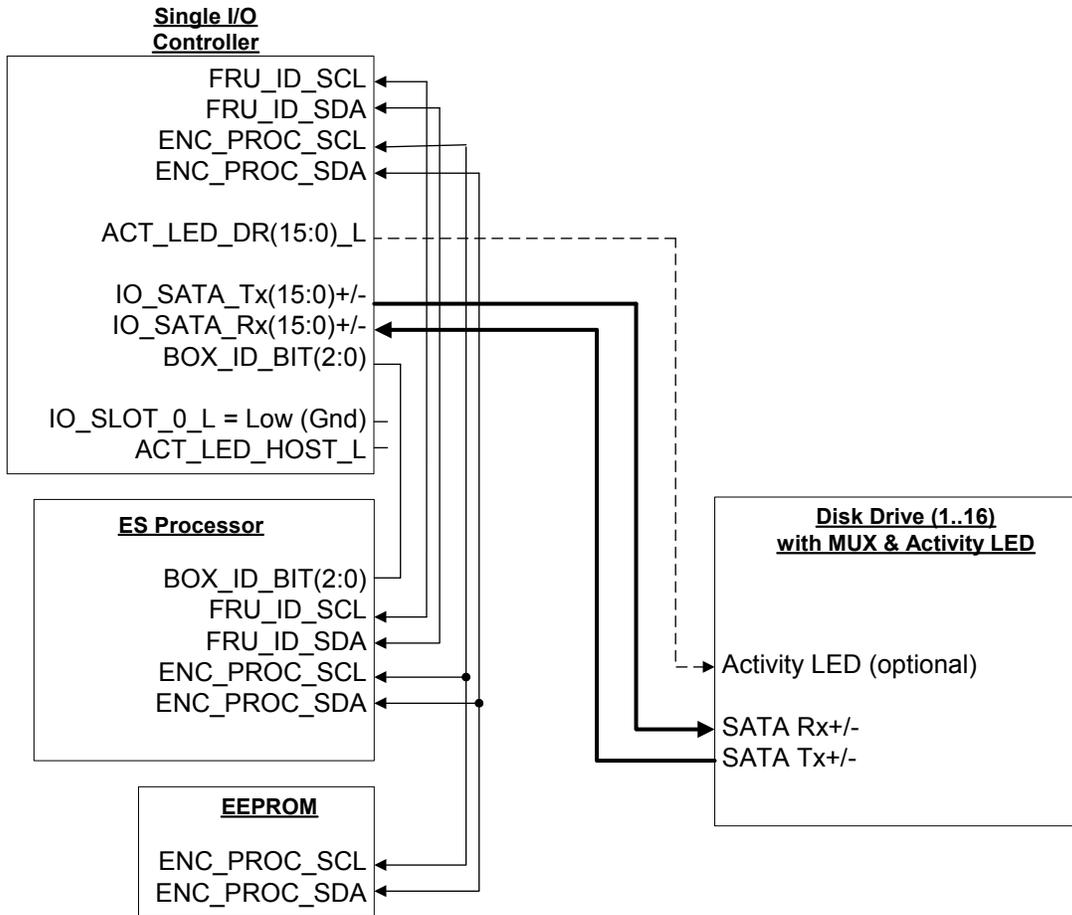
Figure 4.2 – An example of signal connections with one I/O Controller

4.2.2. Dual I/O Controller Signals

As for single I/O controller and in addition:

- Multiplexer control to provide dual access for I/O controller failover capabilities
- I/O controller to I/O controller communication

4.2.3. Further optional features

- RAID battery backup support
- Additional low and high speed communications for optional board-to-board communications. As this specification is not intended to define board-to-board for boards from different manufacturers; the actual implementation of signaling and protocol is left to the discretion of the I/O controller manufacturer.
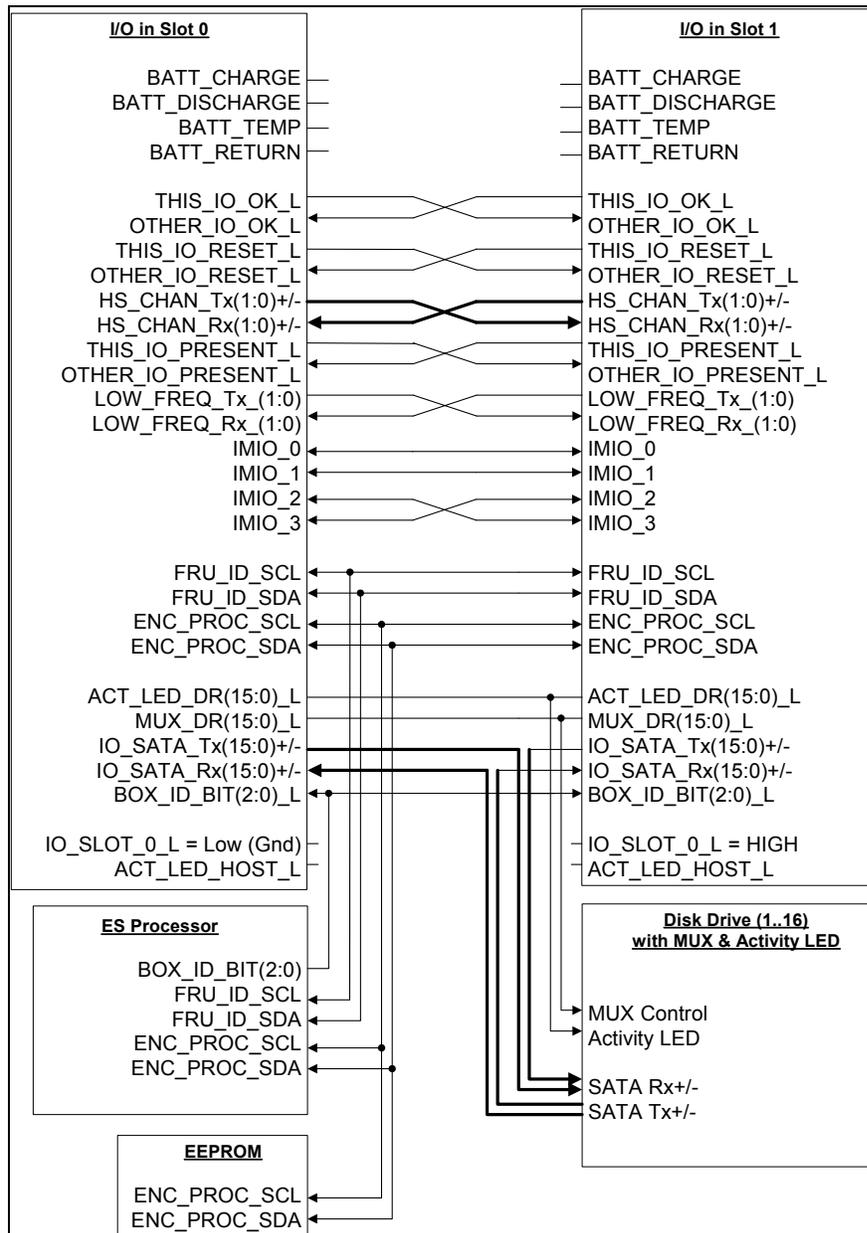
Figure 4.3 Example of signal connections with two I/O Modules

4.3. Optional High Speed Channel configurations

The optional High speed communications channels can be used for high speed differential communications between the two I/O controllers, or for I/O controller to host communications such as inclusion into a Fibre Channel loop. It is recommended that these signals should be 100 ohms differential characteristic impedance.

Actual usage is open to the user definition however the normative backplane routing should be either:

      1.   Configuration 0: Both channels link I/O controller to I/O controller

      2.   Configuration 1: One channel links the two I/O Controllers, and the other is router to a host connector.
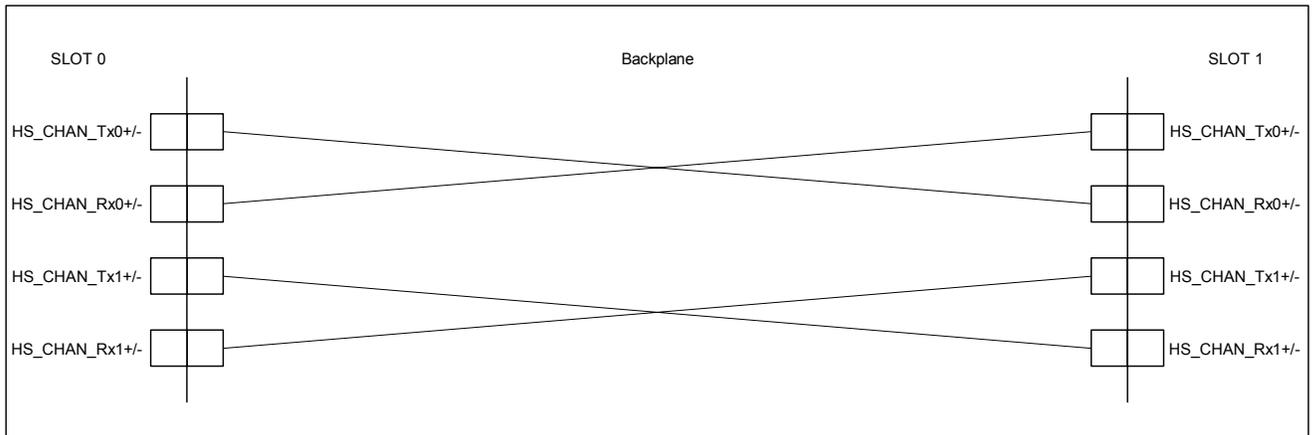
Figure 4.4 – High Speed Channels- Configuration 0
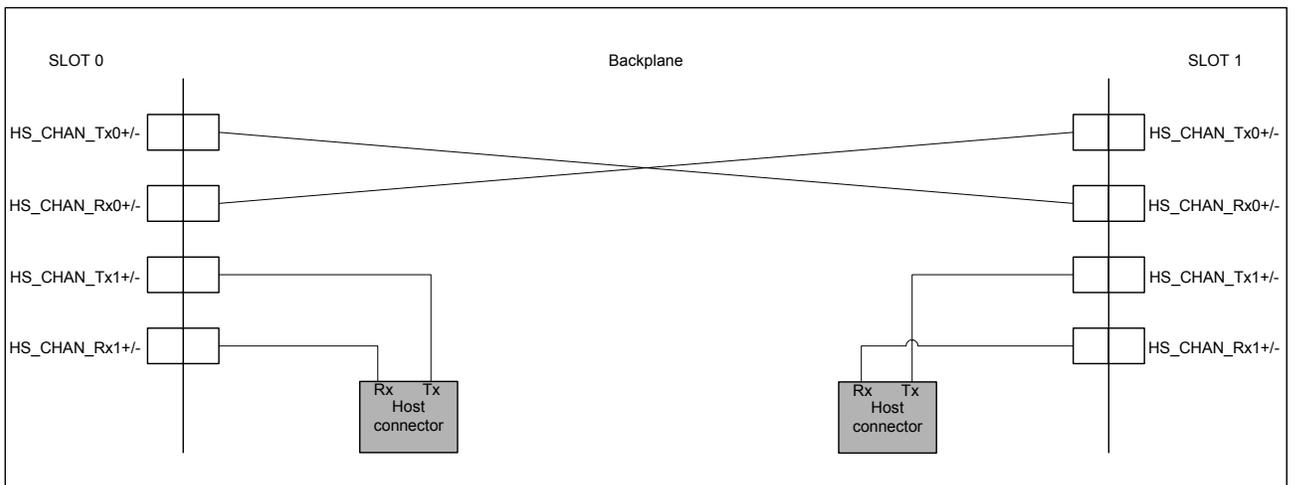
Figure 4.5 – High-Speed Channels - Configuration 1

4.4. Optional Low Speed Channel configurations

The optional Low speed communications channels can be used for end-to-end I/O controller to I/O controller communications. There is a pair transmit and receive signals for low frequency (<500 kHz) I/O controller to I/O controller communications.
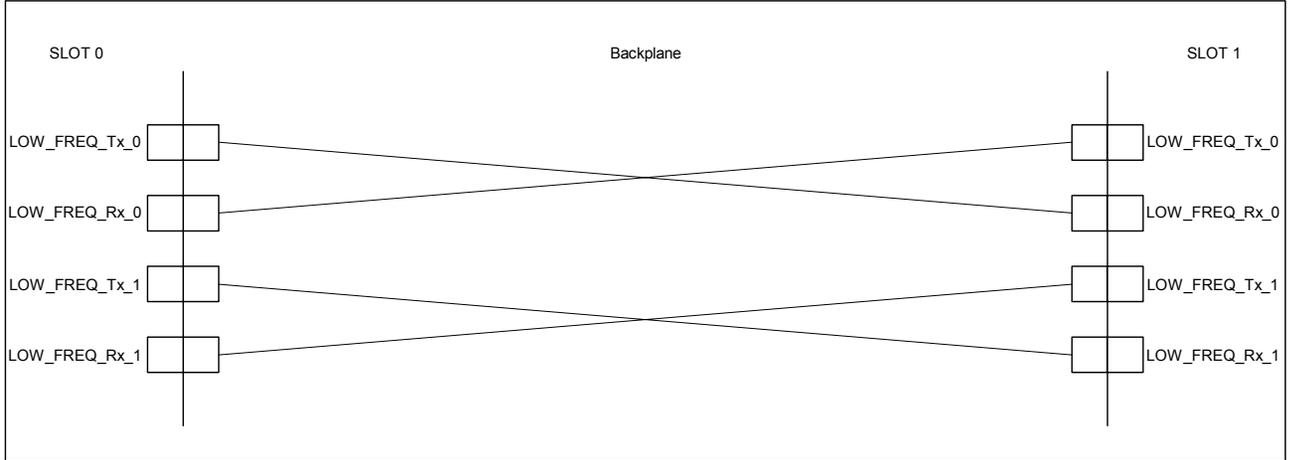
Figure 4.6 Low Speed Channels

There are 4 end-to-end signals that can be used for intermodule I/O communications.
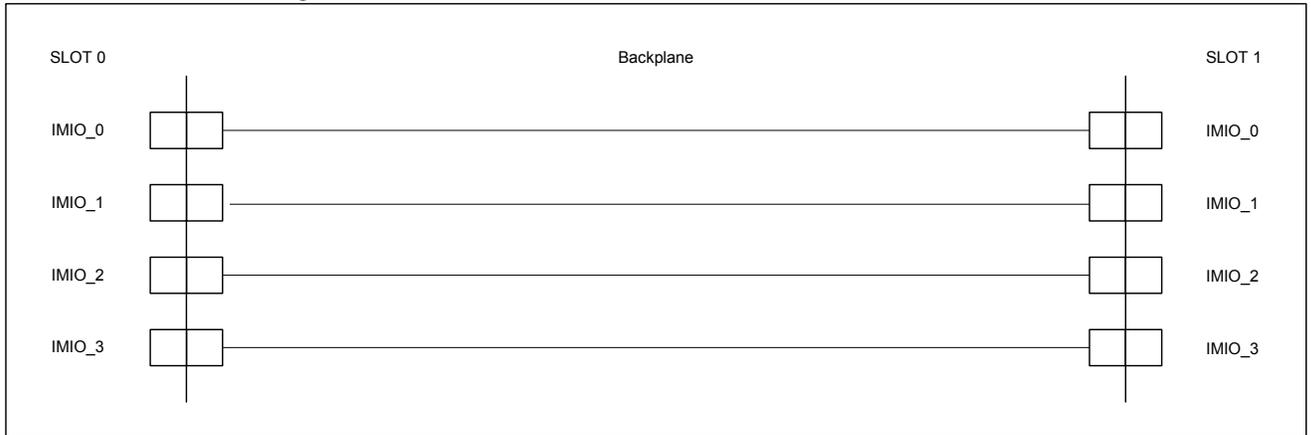
Figure 4.7 Interconnect Channels

4.5.   Backplane Connector

The interface connector that shall be used on the backplane is based on a Berg-FCI High Speed Metral 5x6 30-pin male header connector part number 59566-1001 or equivalent. Example prints are available on www.fciconnect.com Equivalent parts from ITT Cannon: on the backplane 5-row 4000 male CBC20HS4000-030WXP5-5yy-x-VR; and on the I/O controller 5-row 4000 std-female CBC20HS4000-030FDP5-500-x-VR.

4.5.1.   I/O Controller Connector

The interface connector that shall be used on the I/O controller is based on a Berg-FCI High Speed Metal 5x6 30-pin right angle female receptacle part number 52057-102. This connector is used for the 6 high-speed connectors.
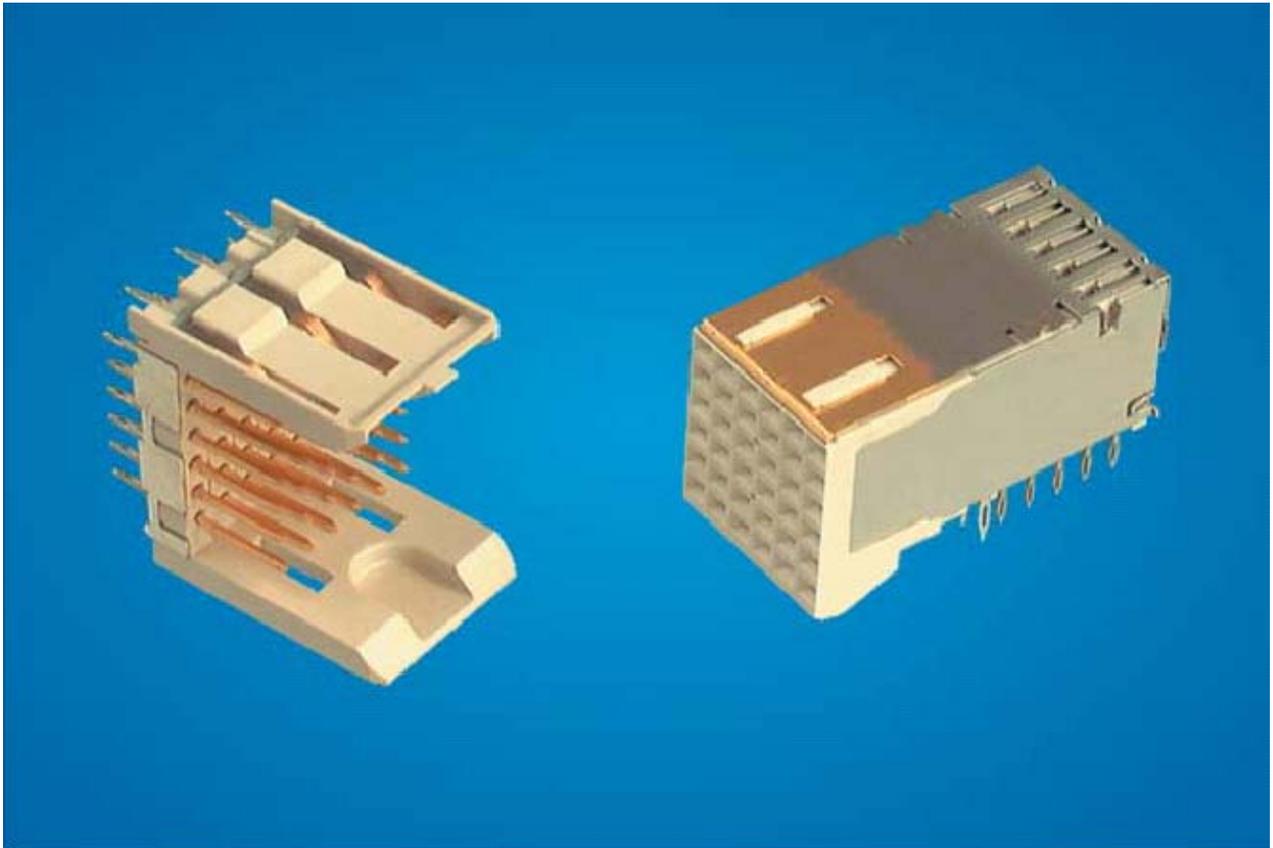
Figure 4.8 – Connector Rendering

Note: Dim B Mating Pin Length
Row C column 1, 3 & 5 pin length is 7.25 mm
Row C column 6 pin length is 6.5 mm
All other pins in header have a pin length of 5.75 mm
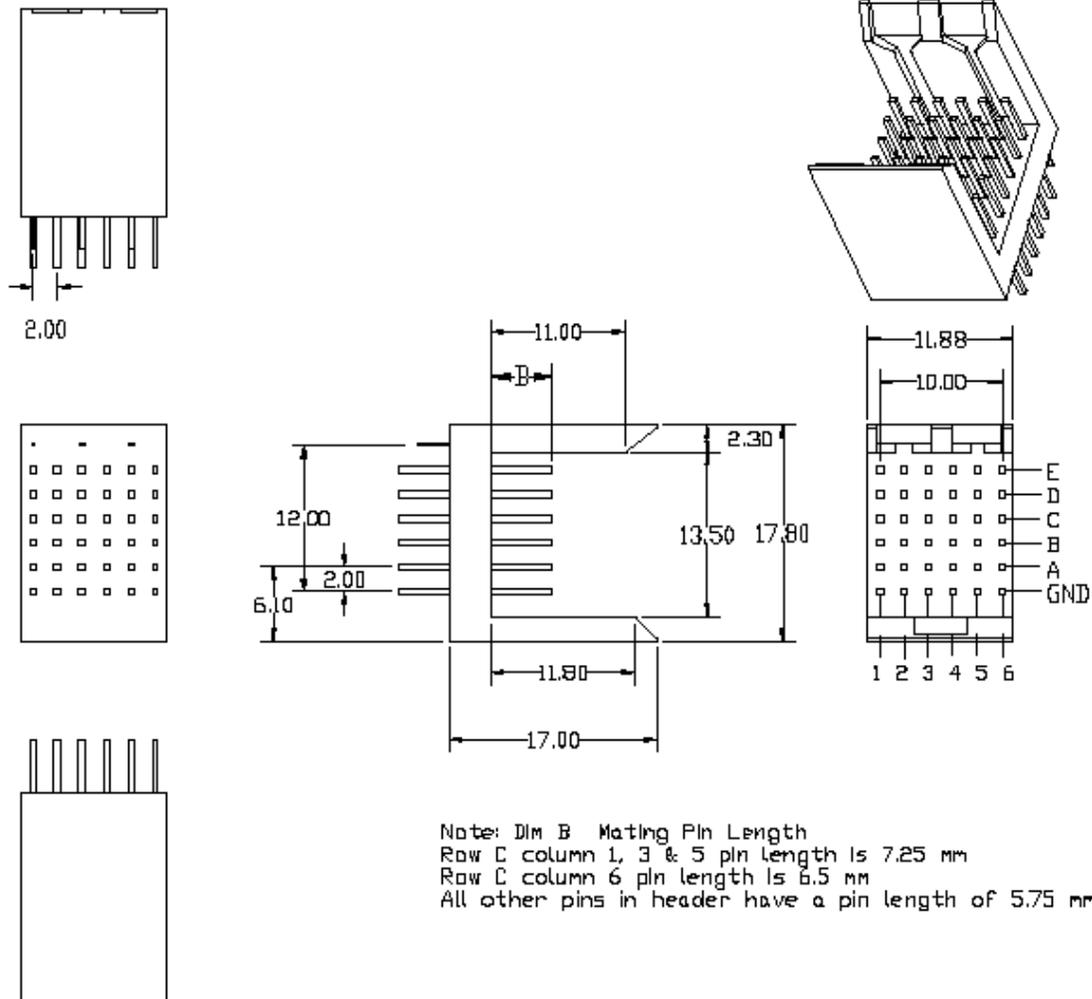
Figure 4.9 – Connector Pin Layout and Pin Lengths
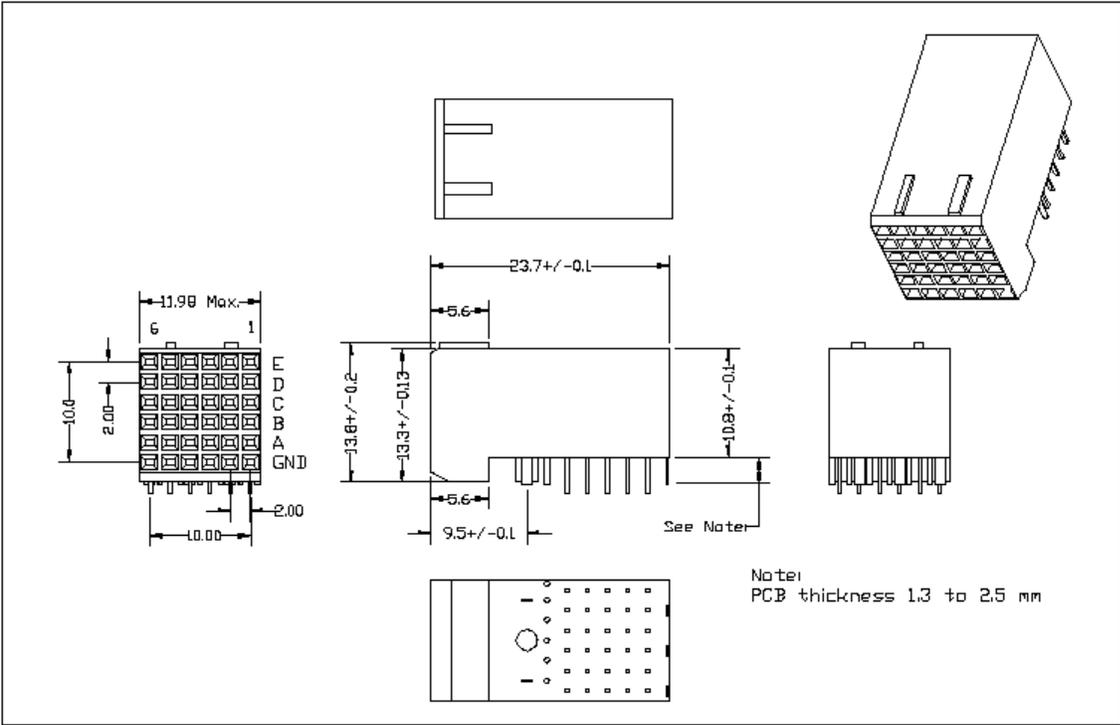
Figure 4.10 – Backplane Connector Receptacle Engineering Drawing
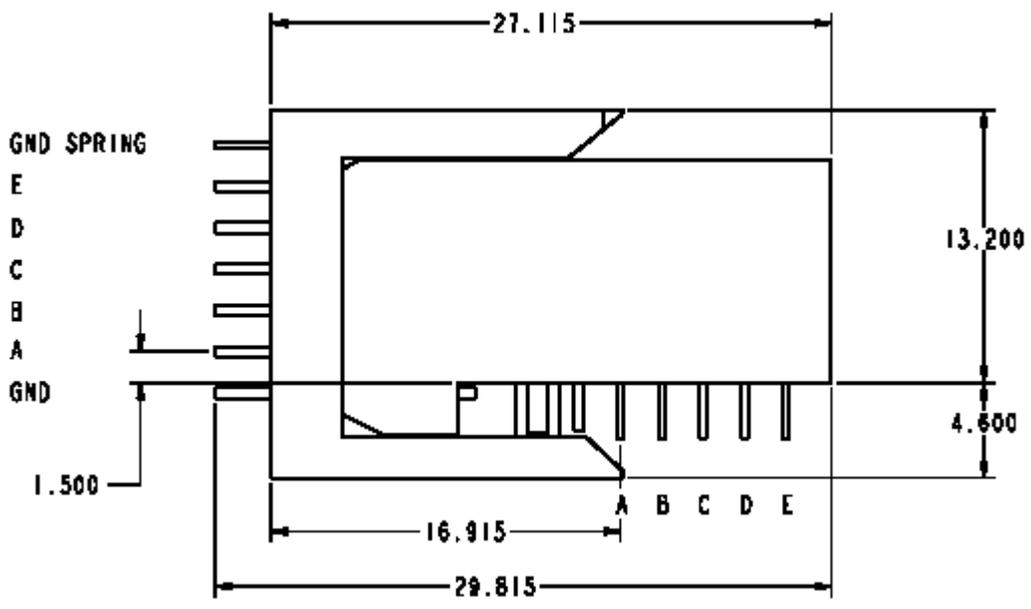
Figure 4.11 – Side View of Connector

4.6. Backplane Connector Locations

4.6.1.   Purpose

This section defines the mating connector locations and connector alignment between I/O modules from one manufacturer and backplanes from a different manufacturer. This is an optional feature of the Serial ATA specification; however I/O controllers and Serial ATA backplanes in support of this industry normal Serial ATA I/O Controller-to-Backplane interface definition <u>shall</u> adhere to this specified connector placement, and connector pinout.
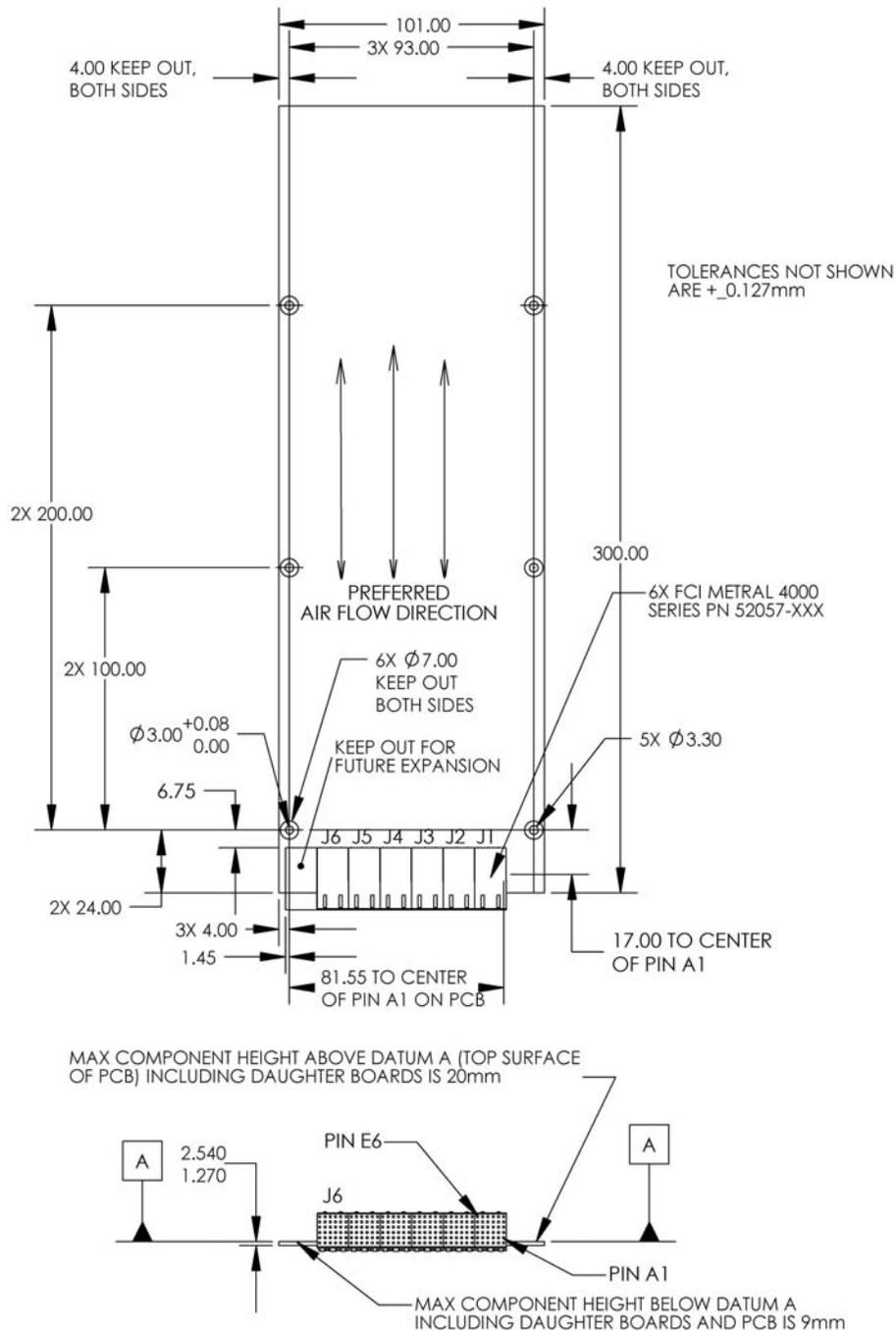
Figure 4.12 – Backplane Connector Locations on 1xWide I/O module
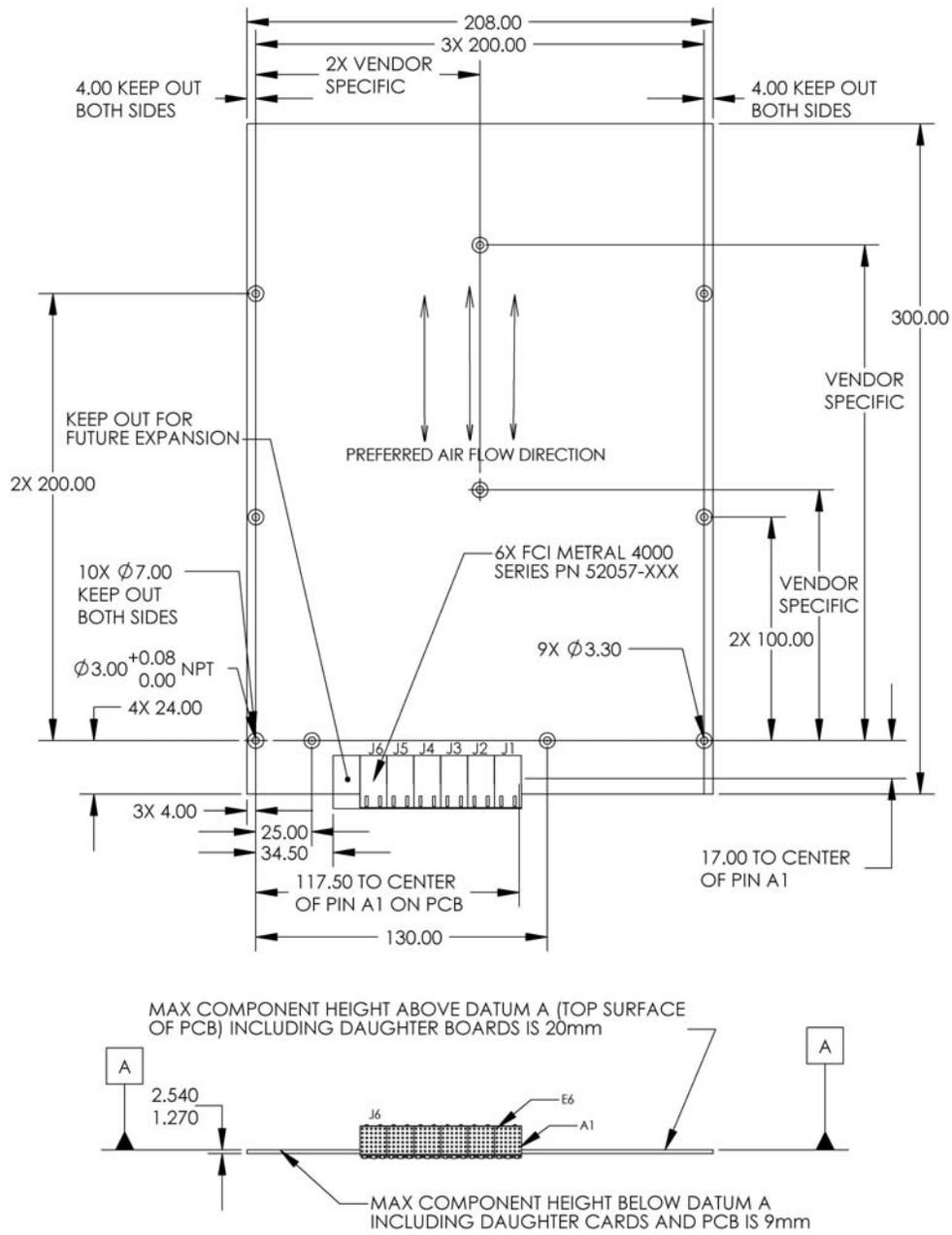
Figure 4.13 – Backplane Connector Locations on 2xWide I/O Module

4.7. Pinout Listing

These tables show the pin listing for the Metral 4000 connector system.
Note that there are grounded shields between each connector row and signal, which are not shown in this matrix to aid clarity.

Table 4.1 - J1, J2, J3 Pin Assignments

J1	Row E	Row D	Row C	Row B	Row A	Ground
1	DR0_TO_IO+	DR0_TO_IO-	Ground	IO_TO_DR0+	IO_TO_DR0-	Shield
2	ACT_LED_DR0_L	MUX_DR0_L	5V	5V	IO_SLOT_0_L	Shield
3	DR1_TO_IO+	DR1_TO_IO-	Ground	IO_TO_DR1+	IO_TO_DR1-	Shield
4	ACT_LED_DR1_L	MUX_DR1_L	5V	5V	OTHER_IO_PRESENT_L	Shield
5	DR2_TO_IO+	DR2_TO_IO-	Ground	IO_TO_DR2+	IO_TO_DR2-	Shield
6	ACT_LED_DR2_L	MUX_DR2_L	5V PRECHARGE	ENC_PROC_SDA	ENC_PROC_SCL	Shield

J2	Row E	Row D	Row C	Row B	Row A	Ground
1	DR3_TO_IO+	DR3_TO_IO-	Ground	IO_TO_DR3+	IO_TO_DR3-	Shield
2	ACT_LED_DR3_L	MUX_DR3_L	5V	5V	BOX_ID_BIT_0	Shield
3	DR4_TO_IO+	DR4_TO_IO-	Ground	IO_TO_DR4+	IO_TO_DR4-	Shield
4	ACT_LED_DR4_L	MUX_DR4_L	5V	5V	BOX_ID_BIT_1	Shield
5	DR5_TO_IO+	DR5_TO_IO-	Ground	IO_TO_DR5+	IO_TO_DR5-	Shield
6	ACT_LED_DR5_L	MUX_DR5_L	5V PRECHARGE	FRU_ID_SDA	FRU_ID_SCL	Shield

J3	Row E	Row D	Row C	Row B	Row A	Ground
1	DR6_TO_IO+	DR6_TO_IO-	Ground	IO_TO_DR6+	IO_TO_DR6-	Shield
2	ACT_LED_DR6_L	MUX_DR6_L	5V	5V	BATT_CHARGE	Shield
3	DR7_TO_IO+	DR7_TO_IO-	Ground	IO_TO_DR7+	IO_TO_DR7-	Shield
4	ACT_LED_DR7_L	MUX_DR7_L	5V	THIS_IO_PRESENT_L	BATT_DISCHARGE	Shield
5	DR8_TO_IO+	DR8_TO_IO-	Ground	IO_TO_DR8+	IO_TO_DR8-	Shield
6	ACT_LED_DR8_L	MUX_DR8_L	12V PRECHARGE	12V	12V	Shield

Table 4.2 - J4, J5, J6 Pin Assignments

J4	Row E	Row D	Row C	Row B	Row A	Ground
1	DR9_TO_IO+	DR9_TO_IO-	Ground	IO_TO_DR9+	IO_TO_DR9-	Shield
2	ACT_LED_DR9_L	MUX_DR9_L	5V	12V	BATT_RETURN	Shield
3	DR10_TO_IO+	DR10_TO_IO-	Ground	IO_TO_DR10+	IO_TO_DR10-	Shield
4	ACT_LED_DR10_L	MUX_DR10_L	5V	THIS_IO_OK_L	BATT_TEMP	Shield
5	DR11_TO_IO+	DR11_TO_IO-	Ground	IO_TO_DR11+	IO_TO_DR11-	Shield
6	ACT_LED_DR11_L	MUX_DR11_L	Reserved (3_3V PRECHARGE)	Reserved (3_3V)	BOX_ID_BIT_2	Shield
J5	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**	**Ground**
1	DR12_TO_IO+	DR12_TO_IO-	Ground	IO_TO_DR12+	IO_TO_DR12-	Shield
2	ACT_LED_DR12_L	MUX_DR12_L	5V	LOW_FREQ_RX_2	LOW_FREQ_TX_2	Shield
3	DR13_TO_IO+	DR13_TO_IO-	Ground	IO_TO_DR13+	IO_TO_DR13-	Shield
4	ACT_LED_DR13_L	MUX_DR13_L	5V	ACT_LED_HOST0	ACT_LED_HOST1	Shield
5	DR14_TO_IO+	DR14_TO_IO-	Ground	IO_TO_DR14+	IO_TO_DR14-	Shield
6	ACT_LED_DR14_L	MUX_DR14_L	Reserved (3_3V PRECHARGE)	Reserved	Reserved	Shield
J6	**Row E**	**Row D**	**Row C**	**Row B**	**Row A**	**Ground**
1	DR15_TO_IO+	DR15_TO_IO-	Ground	IO_TO_DR15+	IO_TO_DR15-	Shield
2	ACT_LED_DR15_L	MUX_DR15_L	5V	5V	OTHER_IO_RESET_L	Shield
3	HS_CHAN_TX(0)+	HS_CHAN_TX(0)-	Ground	HS_CHAN_RX(0)+	HS_CHAN_RX(0)-	Shield
4	LOW_FREQ_RX_1	LOW_FREQ_TX_1	5V	IMIO_0	IMIO_1	Shield
5	HS_CHAN_TX(1)+	HS_CHAN_TX(1)-	Ground	HS_CHAN_RX(1)+	HS_CHAN_RX(1)-	Shield
6	OTHER_IO_OK_L	THIS_IO_RESET_L	5V PRECHARGE	IMIO_2	IMIO_3	Shield

NOTES:

1 Connector as seen from side 1 of backplane. (I.e. Disk Side)

2 Long pins shaded black - Length 7.25 mm

3 Medium pins shaded grey - Length 6.50 mm

4 All other pins short - Length 5.75 mm

4.8. Signal Descriptions

4.8.1. ACT_LED_DR(15:0)_L

Description: Signal is used to drive the activity LED associated with each disk drive. This is an active low signal, i.e. the LED is on when the signal is low. The LEDs are pulled up to +5 Vdc. The LED control circuitry must be capable of sinking 15 mA at 0.4V steady-state.

This signal should be driven by an open-drain output in order to prevent damage should two I/O modules inadvertently attempt to drive the signal at the same time. During RESET the I/O controller output should be set to a high impedance state.

The number of activity LED signals will match the number of SATA ports supported by the controller. It is not mandatory to support 16 ports, any number between 1 and 16 SATA ports can be supported by this specification.

4.8.2. MUX_DR(15:0)_L

Description: Signal is used to control the Serial ATA path through a front-end multiplexer to a disk drive (if implemented). When this signal is low, the multiplexer will select the Serial ATA path to the I/O controller in the option slot 0 identified with IO_Slot_0 connected to GND. This is a standard 3.3 VTTL level signal. This signal should be driven by an open-drain output in order to prevent damage should two I/O modules inadvertently attempt to drive the signal at the same time.

Serial ATA is a point-to-point, controller to disk drive, single initiator interface. Current Serial ATA drives do not support dual Serial ATA ports, therefore, no native capability exists to implement I/O controller failover (Active-Active or Active-Passive). An alternative method to provide a dual I/O controller access to the same disk drive is to implement a front-end multiplexer between the I/O controller and disk drive. This multiplexer will allow only one I/O controller to own the complete access to the disk drive and implement an Active-Passive failover.

This signal will not be implemented in single I/O controller enclosures, as all Serial ATA signals will be directly connected to the single slot. The I/O controller needs to ensure it can operate in a single I/O controller configuration without the presence of these signals.

The MUX_DRx_L controls on the I/O controller must be capable of being reset to an OPEN or high impedance state using the I/O controller RESET signal. This is to allow the failover I/O controller to have direct RESET capability over the MUX_DRx_L controls in the event of the I/O controller failure.

The number of activity MUX_DR signals will match the number of SATA ports supported by the controller. It is not mandatory to support 16 ports, any number between 1 and 16 SATA ports can be supported by this specification.

4.8.3. IO_SATA_Tx(15:0)±

Description: Differential SATA signal pair that originates at the I/O controller (Tx) and is received by the SATA disk drive (Rx). It is not mandatory to support 16 ports, any number between 1 and 16 SATA ports can be supported by this specification.

These signals must be 100 ohms differential characteristic impedance as per the Serial-ATA 1.0 specification.

4.8.4. IO_SATA_Rx(15:0)±

Description: Differential SATA signal pair that originates at the SATA disk drive (Tx) and is received by the I/O controller (Rx). It is not mandatory to support 16 ports, any number between 1 and 16 SATA ports can be supported by this specification.

These signals must be 100 ohms differential characteristic impedance. As per the Serial-ATA 1.0 specification.

4.8.5. IO_Slot_0_L

Description: Active low signal that identifies the I/O controller location, 0 or 1. This signal will be pulled low (GND) on the backplane for IO Slot 0 and high (3.3 Vdc through a 10kΩ resistor) for IO Slot 1.

In a single I/O controller enclosure, this signal shall be connected to GND. In a dual controller configuration, the I/O controller should sense this line to determine in which slot it is located.

4.8.6. Ground

Description: Signal and power ground of the I/O module.

4.8.7.   5V PRECHARGE

Description: +5 Vdc power that is available on the extended pins. This is used for pre-charging the I/O module.

The enclosure must provide for a current limit of 4.5 Amps peak on each 5V pre-charge pin (R=1.1Ω).

4.8.8.   5V

Description: +5 Vdc power that is available on standard length pins.

The enclosure must be capable to supplying 10 Amps of 5V current per I/O module.

4.8.9.   3V3 PRECHARGE

Description: +3.3 Vdc power that is available on the extended pin. This is used for pre-charging the I/O controller 3.3V circuitry. The enclosure must provide for a current limit of 0.75 Amps on each 3.3V pre-charge pin (R=4.4 Ω).

4.8.10.   3V3

Description: +3.3 Vdc power that is available on standard length pins.

The enclosure must be capable to supplying 0.75 Amps of 3.3V current per I/O module.

4.8.11.   12V PRECHARGE

Description: +12 Vdc power that is available on the extended pins. This is used for pre-charging the 12V circuitry in the I/O Option slot module.

The enclosure must be capable of supplying 2.4 Amps peak on each 12V pre-charge pin (R=5Ω).

4.8.12.   12V

Description: +12 Vdc power that is available on standard length pins.

The enclosure must be capable of supplying 1.0 Amp of current per I/O module.

4.8.13.   FRU_ID_SCL

Description: Clock signal of the FRU Identification 2-wire, serial bus. The backplane has a 1.1 kΩ resistor pulled up to 3.3 Volts on this signal. The devices on this bus shall have open collector outputs. This 2-wire serial bus is used by the enclosure processor to gather information from all the FRUs located within the enclosure.

4.8.14.   FRU_ID_SDA

Description: Data signal of the FRU Identification 2-wire, serial bus. The backplane has a 1.1 kΩ resistor pulled up to 3.3 Volts on this signal. The devices on this bus shall have open collector outputs. This 2-wire serial bus is used by the enclosure processor to gather information from all the FRUs located within the enclosure.

4.8.15.   ENC_PROC_SCL

Description: Clock signal of the SES processor 2-wire, serial bus. The SES processor has a 1.1 kΩ resistor pulled up to 3.3 Volts on this signal. The devices on this bus shall have open collector outputs. This 2-wire serial bus is used by the I/O controller to talk to the enclosure processor.

4.8.16.   ENC_PROC_SDA

Description: Data signal of the SES processor 2-wire, serial bus. The SES processor has a 1.1 kΩ resistor pulled up to 3.3 Volts on this signal. The devices on this bus shall have open collector outputs. This 2-wire serial bus is used by the I/O controller to talk to the enclosure processor.

4.8.17. HS_CHAN_Tx(1:0)

Description: Differential transmit pair that can connect the I/O controller to either the other I/O controller or an I/O connector receive pair. Details of the uses of these signals are provided in Figures 4.4 and 4.51. It is recommended that these signals should be 100 ohms differential characteristic impedance.

4.8.18. HS_CHAN_Rx(1:0)

Description: Differential receive pair that can connect the I/O controller to either the other I/O controller or an I/O connector transmit pair. Details of the uses of these signals are provided in Figures 4.4 and 4.51. It is recommended that these signals should be 100 ohms differential characteristic impedance.

4.8.19. ACT_LED_HOST_L

Description: Host link activity LED control signal from the I/O controller for front panel mounted LED. Each port will have a separate LED for the intended use of indication which controller port is active. Exact functionality may be defined by the vendor.

4.8.20. BATT_CHARGE

Description: Signal is used to charge a battery back-up unit (BBU). The backplane must support a maximum of 2 amps on this trace.

4.8.21. BATT_DISCHARGE

Description: Signal is used to discharge a BBU. The backplane supports a maximum of 2 amps on this trace.

4.8.22. BATT_TEMP

Description: Signal is used to report an analog voltage level which corresponds to a temperature level within a BBU. The backplane supports a maximum of 100 mA on this trace.

4.8.23. BATT_RETURN

Description: Signal is used as the return (ground) path for a BBU. The backplane supports a maximum of 2 amps on this trace.

4.8.24. THIS_IO_OK_L

Description: Active low signal is used to determine if the I/O Option slot module is performing within specification. This signal is driven by the I/O controller. The I/O Option Slot module must provide a pull-up for this line when it is inactive. The backplane should support a maximum of 100 mA on this trace.

4.8.25. OTHER_IO_OK_L

Description: Active low signal is used to determine if the other I/O Option slot module in a dual controller configuration is performing within specification. This signal is an input to the I/O controller. The backplane should support a maximum of 100 mA on this trace.

4.8.26. OTHER_IO_RESET_L

Description: Active low output signal which is used to reset the other I/O Option slot module in a dual controller system, located in the opposite slot. The backplane must provide a pull-up for this line when it is inactive. This signal is cross-wired with the THIS_IO_RESET_L signal on dual controller backplanes. The backplane should support a maximum of 100 mA on this trace.

4.8.27. THIS_IO_RESET_L

Description: Active low input signal which is used to reset the I/O Option slot module located in this slot. This signal is cross-wired with the OTHER_IO_RESET_L signal on dual controller backplanes. The backplane should support a maximum of 100 mA on this trace.

4.8.28.   LOW_FREQ_RX_(1:0)

Description: Signal line used for intermodule, 2-wire communications. This signal is cross-wired with the LOW_FREQ_TX signal on dual controller backplanes as shown in Figure 4.6. This is a low-speed signal line. Maximum frequency is 500 kHz. The actual implementation of this signal is to be decided by the I/O controller vendor. The backplane should support a maximum of 100 mA on this trace.

4.8.29.   LOW_FREQ_TX_(1:0)

Description: Signal line used for intermodule, 2-wire communications. This signal is cross-wired with the LOW_FREQ_RX signal on dual controller backplanes as shown in Figure 4.6.. This is a low-speed signal line. Maximum frequency is 500 kHz. The actual implementation of this signal is to be decided by the I/O controller vendor. The backplane should support a maximum of 100 mA on this trace.

4.8.30.   OTHER_IO_PRESENT_L

Description: Active low signal is used to denote the presence of an option slot module in the opposite I/O option slot module. The I/O controller must provide a pull-up for this line when it is inactive. This signal is cross-wired with the THIS_IO_PRESENT_L signal on the dual backplane only. This is a low-speed signal line. The actual implementation of this signal is to be decided by the I/O controller vendor. The backplane should support a maximum of 100 mA on this trace.

4.8.31.   THIS_IO_PRESENT_L

Description: Active low signal is used to denote the presence of an option slot module in the local I/O option slot module. The I/O controller must provide a pull-up for this line when it is inactive. This signal is cross-wired with the OTHER_IO_PRESENT_L signal on the dual backplane only. This is a low-speed signal line. The actual implementation of this signal is to be decided by the I/O controller vendor. The backplane should support a maximum of 100 mA on this trace.

4.8.32.   IMIO_(3:0)

Description: These are direct connecting signals used for intermodule communication. The backplane should support a maximum of 100 mA on these traces. See Figure 4.7 for details.

4.8.33.   BOX_ID_BIT_(2:0)

Description: Signal is used to determine the ID of the enclosure in which it is installed.

4.8.34.   Reserved (2 pins)

Description: Two undefined pins J5 Row A pin 6, and J5 Row B pin 6, which are not available for use at this time. No signals should be connected to these signals on either the backplane or the I/O Option Slot Module.

Please refer to Serial ATA Backplane Design Guide available on http://www.serialata.org/ for additional information.