SCSI signal modeling study group (SSM)   99-329r1
December 01, 1999
Rochester, MN, CA
Subject: Approved minutes for the SSM study group on October 28, 1999

This was the next meeting to address the general subject of modeling for
parallel SCSI. Dean Wallace of QLogic led the meeting. Bill Ham of
Compaq took these minutes. There was a good attendance from a broad
spectrum of the industry. Qlogic (Dean Wallace) hosted the meeting.

Last approved minutes: 99-287r1.

1. Introduction

Dean Wallace opened the meeting and conducted the introductions and
reviewed the meeting purpose.

2. Attendance

The following folks were present:

Dean Wallace, Qlogic, d_wallace@qlc.com
Martin Ogbuokiri, Molex, mogbuokiri@molex.com
Larry Barnes, LSI Logic, larry.barnes@lsil.com
Jonathan Fasig, Western Digital, jonathan.L.Fasig@wdc.com
Tariq Abou-Jeyab, Adaptec, tajeyab@corp.adaptec.com
Bill Ham, Compaq, bill_ham@ix.netcom.com
Andrew Bishop, Quantum, andrew.bishop@quantum.com
Matt Schumacher, Compaq, Matt.Schumacher@compaq.com
Jeff Walden, Foxconn, jwalden@ieee.org
Dave Chapman, Amphenol, dave.chapman@aipc.fabrik.com
Jie Fan, Madison cable, jfan@tycoelectronics.com
Greg Vaupotic, Amphenol, gerg.vaupotic@snet.net
Donald Getty, Unitrode-TI, donald_getty@ti.com
Paul Navarrez, FCI, pnavarrez@fciconnect.com
Amy Barton, Circuit Assembly, amyb@circuitassembly.com

3. Agenda development

The agenda shown was that used.

4. Approval of previous minutes

The minutes of the August meeting (99-287r0) were approved (ham moved / Dean Wallace Bishop seconded) with slight modifications and Ham will post them with the corrections. This will be document 99-287r1.

5. Presentation policy

After some discussion the following policy relating to making presentations at SSM was developed:

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

6. SSM Project proposal - Ham

The project proposal was changed by the SCSI working group to a technical report. The revised proposal cast in a Technical report

format was created and posted to the T10 web site. Since the document did not meet the two week rule it was not voted on at the last plenary. The document is on the web site 99-243r1.pdf.

7. Presentations

7.1 Andrew Bishop / Jie Fan SPICE cable modeling results)

This presentation is or will be available on the T10 web site.

7.2 Simulation study questions (Schumacher)

Matt Schumacher presented a collection of questions intended to help intended to bound the work of the simulation working group:

What degree of accuracy is expected from simulation
      Are worst case limits a requirement of simulation?
            If so, will the require transistor level / SPICE models?
            If so, we will also require input from cross talk – this implies multilevel models

      On the other hand, is it sufficient to use simulation for "topology improvement"?
            If so, few can get along w/o multilevel models and SPICE xcvr's

What types of models are required to achieve worst case accuracy
      Multiline connector models will be required
      Correlated xcvr's (SPICE?)
      What else?

Can the average company / engineer obtain the required models?
      Multilevel models will be difficult
      SPICE transceivers may be unobtainable

Verification?
Optimization?

This presentation further underscored the need to develop a comprehensive set of definitions as a core starting point.

7.3 Document framework (Barnes)

Larry Barnes, editor of the SSM document, reviewed the present state and organization of the document. Following is the result of this discussion cast in the form of a table of contents with owners assigned. The numbering may not be accurate in the list below.

1 Scope and Purpose (Larry Barnes)
1.1 Scope

1.2 Purpose

2 References (Jonathan Fasig)
2.1 Tools (TBD)

3 Definitions, Acronyms, Keywords, and Conventions   group

4 Overview (Bill Ham)

6 Models
6.1 General Recommendations (Larry Barnes)
6.1.1 Supporting Documentation

6.2 Cables
6.2.2 Cable media (bulk cable) (Jie Fan)
6.2.3 Transition region (Bob Gannon?)

6.3 Connectors (Martin O.)
6.3.1 Cable Connectors
6.3.2 Non-Cable Connectors
6.3.2.1 RGL transmission line matrix

6.4 PCB's (Matt S. / Tariq A.)
6.4.1 Traces
6.4.1.1 Microstrip
6.4.1.2 Stripline
6.4.1.3 Broad Coupled Stripline
6.4.1.4 Offset Broad Coupled Stripline
6.4.2 Discontinuities
6.4.2.1 Vias
6.4.2.2 Pads

6.5 Terminators (Paul Aloisi / Don Getty)

6.6 Transceivers (Dean Wallace)

6.7 Chip packages (Dean Wallace)

7 Standard Model Constructions
7.1 Host bus adapter / target board model (Tariq / Matt S.)
7.2 Point to point / multidrop (TBD)
7.3 Cable assemblies (TBD)
7.2 System Model (TBD)
7.4 Backplane (Larry Barnes)

8 Measurement and Validation
8.2 Physical measurement points (Greg V.)
8.1 Access to Measurement Points
8.3 Behavioral
8.4 Circuit

9 Simulation integration strategy (Dean Wallace)
9.1 System configurations
9.2 Data patterns
9.3 Data rate

Section owners are to create basic material and submit to Larry Barnes
by November 19, 1999.

7.4 Model database strategy (Wallace)

Dean proposed a specific summary of the present plans for the web based database:

Web Site for models

- List of companies with existing models.
- What type of models are they. Connector media, transceiver etc.
- Description / intended use
- Path to the model, is an nda required for the model.
- What type of model, SPICE, IBIS, HDL.
- Revision history on site.

7.5 IBIS issues (Wallace)

Dean reported that new thoughts concerning IBIS and other tools may be in order. Following is his presentation:

Simulation Tools

1) Choices are primarily SPICE, IBIS, or some type of HDL such as VHDL-AMS.
2) Idealized digital models are not suitable for SI simulations.
3) Analog simulators generally support SPICE models and SPICE netlist formats.
4) SI simulators support IBIS.
5) Mixed mode simulators support VHDL-AMS.

6) SPICE
-Has some serious drawbacks for SI simulations, the simulations run very slow due to the modeling of transistors in full detail.

-Many simulators lack support for coupled transmission lines or lossy lines.

-Accuracy can be questionable for SI due to the interaction between
time-step algorithms and delay characteristics of transmission lines.
Might have to trade off accuracy for reasonable run time.

6) IBIS

- Formal standard IBIS 3.2 standard is currently in balloting.
- Driven by SI design.
- No IP is included with the models.
- IBIS describes I/O pin characteristics using tables of I/V and V/T
  data.
- Table based models simulate much faster (sometimes up to 100 times
  faster than SPICE).
- IBIS models can be as accurate as SPICE models if care is taken in
  measurement and model validation.

7) VHDL-AMS

- New standard IEEE 1076.1.
- Equation based model.
- Mixed analog and digital

The main missing item on the IBIS agenda was the multilevel properties.
Larry Barnes has initiated the work with the IBIS committee on a
multilevel output / ISI compensation capability for IBIS. It appears
likely that an IBIS scheme to deal with theses issues will be
forthcoming thru the IBIS committee at some point in the future.

Taken together, it appears that IBIS may be the vehicle to use for parts
of the system where SPICE is not available or is unsuitable for one
reason or another.

Dean noted that part of the resistance to using IBIS has been that it
takes some work to make the models good. This is the case with any tool
and IBIS may have been getting an unfair negative image in the SSM
group.

7.6 Scrambling (Wallace)

Dean noted that scrambling really is a subset of the data pattern issues
and that this will not be further discussed

8. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This
matrix is a concise description of the methodology to be used for the
respective areas of the point to point SCSI bus segment. Several of the
areas were significantly modified at this meeting. Note that the
multidrop areas have not yet been identified.

8.1 Transceiver chips: owner, Dean Wallace

Interface is at packaging pins
Model types: Spice, IBIS, HDL, table spice – details TBD
Data patterns: TBD
ISI compensation: required but not presently believed compatible with
IBIS capability – this means that IBIS will have to be enhanced and that
only SPICE models will be effective until the new IBIS techniques are
available.
Single line required - cross talk from non SCSI sources not considered
in the model, SCSI line cross talk is not significant within the
transceiver. Therefore multiline models are not required for
transceivers.

8.2 Bus segment termination: owner, Paul Aloisi / Don Getty

Interface is at package pins
Model types: Spice, IBIS details TBD
Terminator type: multimode
Single line only

8.3 Transceiver board: owners, Tariq Abou-Jeyab and Matt Schumacher

Interface is at transceiver board connectors, transceiver chip pins,
terminator chip pins
Model types: Spice
PCB construction: edge, broadside, dielectric type / thickness, vias,
pads, discontinuities
Single line, multiline

Further detail was provided by Matt in this area as transcribed below:

Listed are some key datapoints to consider for HSPICE simulation of a
simple LVD SCSI PCB. Initial simulations will be used to optimize PCB
routing topologies. Simulating worst case scenarios will be discussed
in a later document, as it will require SPICE model correlation, process
corners, multiline SPICE models for cross talk etc.

Request SPICE models:

        check for a driver and a receiver model
        Ask for single line models and multiline models of connectors.
Multiline models may take much longer to arrive if you can get them at
all. If single line models are used, signal integrity investigation
will not include crosstalk.
        Are models for unmated connectors necessary?
        Required models must work for various edge rates (slow, typ, fast)
        Keep the models in a centralized/secure location. Vendors usually
distribute them under NDA.
        Some correlation of the models is recommended (compare simulation
and lab data)
        Request models well in advance of need

Obtain transmission line geometries from PCB data / design requirements

        These parameters are required: trace width, copper weight of trace
and planes, dielectric constants, dielectric spacing within the

differential pair, dielectric spacing to the planes and trace lengths of
the nets to be simulated.

Generate RLGC matrices for transmission line segments(cline):

Using a field solver, obtain the RLGC matrices for the
transmission line geometries.
/compare the field solver impedance with the TDR measurement of
the coupon.
Note: the coupon will provide a controlled environment with
minimal discontinuities for accurate trace characterization.

Draft a trace topology from the known trace segments and components:

Draft the transmission line topology
the drawing below is an example of a simple transceiver board in
host bus adapter

Build a spice netlist for the trace topology:

Do not forget the process variations.

Simulate and review data:

Time domain simulation is sufficient for optimizing topologies.

W's are SPICE element numbers. All other numbers are node locations.
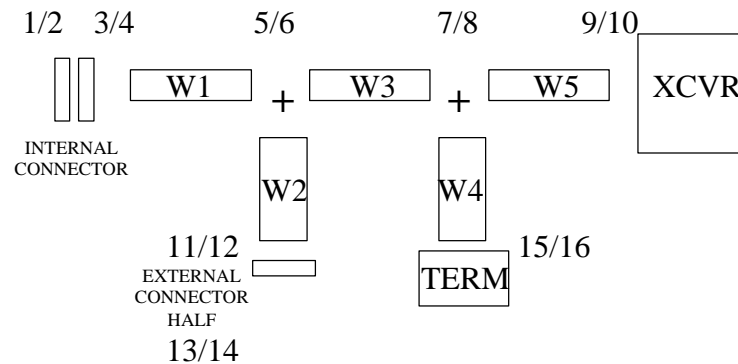
Figure 1 - Architecture of a transceiver board model (no unused
connectors)

8.4 Mated connectors: owner, Martin Ogbuokiri

Interface is at transceiver board and the cable assembly transition
region
Model types: Spice
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,
single line, multiline

8.5 Cable assembly transition region: owner, Bob Gannon

Interfaces are at the connector termination and the uniform media
Model types: Spice same as connector
Construction types: twisted flat, round fanout, laminated round, IDC
flat?
Single line multiline

8.6 Uniform cable media: owner, Jie Fan

Interfaces are at the beginning of the cable assembly transition region
on either end.
Model types: Spice
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

8.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted
components,
Model types: SPICE
PCB construction: edge, broadside, dielectric type / thickness, vias,
pads, discontinuities
Single line, multiline

9. SFF backplane

This item will be dropped from future agendas.

10. Simulation integration strategy

Further discussion pending progress on the component level simulation
work. This will be addressed at the next meeting.

11. System configurations

Not discussed but reaffirmed as needed for the document

12. Data patterns

Not discussed but reaffirmed as needed for the document

13. Data rate

Not discussed, but reaffirmed as needed for the document

14. Definitions:

The following terms were suggested as candidates for definition in the
document:

SPICE, IBIS, model, validation, cable assembly, transition region,
verification, accuracy, HDL, VHDL, ASM, ASCM, Veriloq, PCB, backplane,
microstrip, stripline, via, discontinuity, cline, lossy, lossless,
uniform, attenuation, gain, differential, planar, skin effect,
dielectric constant, dielectric loss, loss tangent, conductivity,
resistivity, convergence, phase velocity, group velocity, group delay,
phase delay, multiline, single line, SLM, MLM, single ended, balanced,
unbalanced, mode, element, RLGC, netlist, admittance, transmittance,
coupling(K), matrix, S parameters, scattering matrix, ABCD, Y
parameters, two-port parameters, and others to be suggested later.

15. Tools:

This topic refers to identification and properties of specific modeling
tools. It was not discussed at this meeting.

16. Next meetings

Dec 01, 1999 Rochester, MN
Future requested meetings:
Jan 31, 2000 Huntington Beach, CA (Qlogic) 1PM to 8PM
Mar 01, 2000 Manchester,NH (Hitachi)

17. Action Items:

17.1 Action items from previous meetings

Status as of the October 28, 1999 meeting is shown.

Martin O. to supply an RGL transmission line matrix (circuit type of
specification) for VHDCI, SCA-2,and HD68 connectors.

Status: carried over, models now exist but not delivered, HD connectors still needed

Dean to provide a target board model.
Status: transferred to transceiver board effort - done

Larry Barnes to create a document framework.
Status: done

Larry Barnes to do an overview presentation of the IBIS transceiver model specification.
Status: carried over - handouts provided but presentation still needed

Ham to post the draft minutes of the September 30 meeting after review by Dean
Status: done

Jim Broomall to provide electronic copy of his presentation on component modeling methods.
Status: done document number 99-289r0

Larry Barnes to propose a multilevel output capability for IBIS to allow for ISI compensation.
Status: ongoing

Andrew Bishop and Dean Wallace to help Jie to develop a cable media model.
Status: done

17.2 New action items from present meeting

Jonathan Fasig to draft a proposal for model requirements for passive interconnects.
Status: new

All matrix element (document section) owners to provide draft input for the respective sections to Larry Barnes by November 19, 1999. (Provide input in Word 6/7 format) send to larry.barnes@lsil.com
Status: new

Dean Wallace to contact Bob Gannon to determine how he wishes to proceed with the cable assembly transition region.
Status: new

Ham to post the draft minutes of the October 28 meeting after review by Dean
Status: new