Accredited Standards Committee*
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Reply to:	John Lohmeyer

To: T10 Membership
From: John Lohmeyer
Subject: SPI-3 Working Group Meeting -- May 22, 1998
Chicago, IL

Agenda

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Results of Meeting

1. Opening Remarks

John Lohmeyer, the T10 Chair, called the meeting to order at 9:00 a.m., Monday May 22, 1998. He thanked Gene Milligan of Seagate for hosting the meeting and providing lunch.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated. John noted that standards are not permitted to contain known patented material unless the patent holder agrees to comply with the ANSI patent policy.

2. Approval of Agenda

The draft agenda was approved with the following additions and changes:

Item '4.6 IUTR Negotiation' was changed to '4.6 Parallel Protocol Request Negotiation'

The following agenda items were added during the course of the meeting:

4.1 Phase Naming

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for T10 membership. Working group meetings are open to any person or organization directly and materially affected by T10's scope of work. The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Lawrence J. Lamers	P	Adaptec, Inc.	ljlamers@ix.netcom.com
Mr. Vincent Bastiani	A#	Adaptec, Inc.	bastiani@corp.adaptec.com
Mr. Robert C. Elliott	P	Compaq Computer Corp.	Robert.Elliott@compaq.com
Mr. Don Vohar	A	Fujitsu (FCPA)	dvohar@fcpa.fujitsu.com
Mr. George Penokie	P	IBM Corp.	gop@us.ibm.com
Mr. Alan Littlewood	P	LSI Logic Corp.	alanl@lsil.com
Mr. Frank Samela	A	Methode Electronics, Inc.	franksam@methode.com
Mr. Skip Jones	P	QLogic Corp.	sk_jones@qlc.com
Mr. Ting Li Chan	A	QLogic Corp.	t_chan@qlc.com
Mr. Chuck Micalizzi	V	QLogic Corp.	c_micalizzi@qlc.com
Mr. James McGrath	A#	Quantum Corp.	JMCGRATH@QNTM.COM
Mr. Bruce Leshay	V	Quantum Corp.	bleshay@tdh.qntm.com
Mr. Richard Uber	V	Quantum Corp.	duber@tdh.qntm.com
Mr. Duncan Penman	V	Quantum Corp.	duncan.penman@qntm.com
Mr. Gene Milligan	P	Seagate Technology	Gene_Milligan@notes.seagate.com
Mr. Daniel (Dan) F. Smith	O	Seagate Technology	daniel_f_smith@notes.seagate.com
Mr. Mayank R. Patel	V	Seagate Technology	patel@cdg.stsv.seagate.com
Mr. John Lohmeyer	P	Symbios, Inc.	lohmeyer@ix.netcom.com
Mr. Tracy Spitler	V	Symbios, Inc.	tracy.spitler@symbios.com
Mr. Andrew Brown	V	Symbios, Inc.	andrew.brown@symbios.com
Mr. David Steele	V	Symbios, Inc.	david.steele@symbios.com
Mr. Dave Wehrman	O	UNISYS Corporation	dave.wehrman2@unisys.com
Mr. Paul D. Aloisi	P	Unitrode Corporation	aloisi@unitrode.com
Mr. Jeffrey L. Williams	P	Western Digital Corporation	Jeffrey.L.Williams@wdc.com
Mr. Gregory Kapraun	A	Western Digital Corporation	Gregory.D.Kapraun@wdc.com
Mr. Bob Warren	V	Western Digital Corporation	robert.w.warren@wdc.com

26 People Present

Status Key:
- P - Principal
- A,A# - Alternate
- O - Observer
- L - Liaison
- V - Visitor

4. SPI-3 Topics

4.1 Phase Naming

George Penokie discussed what to call the two new phases that had previously been unused. The consensus was:

Existing Data In phase:	Single Transition Data In
Existing Data Out phase:	Single Transition Data Out
New Data In phase:	Double Transition Data In
New Data Out phase:	Double Transition Data Out

Where it does not matter whether the clocking is done with single transitions or double transitions, the terms Data In phase and Data Out phase will be used.

4.2 CRC Proposals

Jim McGrath presented 98-177r0, 'Proposal for Parallel SCSI: Increase Transfer Rate and Improve Error Detection'. A number of terminology changes were made, including the naming changes from the above agenda item. Also, the term 'frame' was changed to 'CRC group'.

It was noted that there is no double-transition asynchronous protocol defined.

George Penokie proposed that the double-transition data phases be limited to 16-bit wide buses only. Besides simplifying the design somewhat (particularly in the area of pad bytes), it would mean that the P1 signal could be available for an unspecified purpose. The group did not close on this idea, preferring that it get wider exposure before making a decision.

There was a discussion of whether the pad bytes should be transferred before or after the CRC. Jim's current proposal has the pad bytes transferred after the CRC. Several people argued that the pad bytes should occur first and be included in the CRC. The consensus was that the pad bytes will be before the CRC and the CRC will include both data and the pad bytes. On an 8-bit bus, there will be 0, 1, 2, or 3 pad bytes. On a 16-bit bus, there will be 0 or 1 pad words. 32-bit buses are treated exactly the same as two 16-bit buses, each with their own REQ and ACK signals (REQQ and ACKQ) and each with their own CRC generator/checking logic.

The above rules also simplified the CRC generator since the input will always be a multiple of 32 bits.

There are some boundary cases that needed clarification:

1. A Data Phase with no REQ transitions. (This by definition is not actually a Data Phase.)
2. A Data Phase containing only a CRC without any data. (Unusual, but allowed.)
3. A Data Phase containing data followed by CRC. (This is the normal case.)
4. A Data Phase containing a CRC followed immediately by another CRC. (Unusual, but allowed.)
5. A Data Phase containing data, then CRC followed immediately by another CRC. (Unusual, but allowed.)

It was noticed that there may be some ambiguities regarding entering and leaving packetized mode. It appeared that there is a rule in SPI-3 Rev 0 that prevents the initiator from re-negotiating out of packetized mode: currently, the target will go to Bus Free phase if the initiator selects it with ATN while in packetized mode.

There was a discussion about whether the extra setup time on the CRC_Valid signal is necessary, whether the pad bytes should be inverted, and whether the extra setup time should be 12.5 ns or some other value. It was decided that no changes from Jim's current proposal are necessary (keep the extra 12.5 ns of setup time and do not invert the pad bytes).

4.3 Learn Mode (Domain Validation)

Jim McGrath presented 98-176r1, Proposal for Parallel SCSI: Domain Validation. Several improvements were suggested:

- Both a starting and ending message should be defined.
- The testing sequence can occur at any time.

- The testing sequence occurs at the currently negotiated speed/width/clocking mode.

Jim plans to revise the proposal for next time.

4.4 Expander Communication

Jim McGrath reported that he does not intend to do any more work on his 98-158 document and it should be dropped from future agenda.

4.5 QAS

This topic was not covered.

4.6 Parallel Protocol Request Negotiation

This item was re-named from IUTR since it includes several new items. George Penokie plans to put a proposal on the reflector for consideration at the June 19th meeting.

4.7 Fast-80

Gene Milligan presented 98-153r1. He noted that the paper copies he passed out are actually pre-revision 1. The correct Rev 1 document is on the T10 web/ftp site.

The C1, C2, and C3 capacitance values in Table 6 were changed from 20, 20, 10 pF to 15, 15, 8 pF. There was some concern that these values may be difficult to achieve especially if multimode drivers are required. Jim McGrath suggested that larger values would be acceptable if the device spacing was also increased.

Gene noted that the System Deskew Delay description may need some work. This time may be used incorrectly in the synchronous data transfer description and/or its value may need adjustment.

Symbios plans to bring in a proposal that would change the voltage values in Figure 22 from 1.8 to 1.4 volts. This is based on the desire to support 2.5-volt chips.

There was some discussion on how the Table 10 voltages were selected although these had not changed since SPI-2. There was particular concern over the 3.0 volt specification for Vmin on SE/LVD terminators. Paul Aloisi pointed out that single-ended termination does not need to pull up to 2.85 volts; 2.5 volts is all that is required.

Dan Smith presented 98-182r0, Ultra-3 Cable Tests. Vince Bastiani presented 98-181r0, Fast-80 Eye Pattern Testing. Vince made several suggestions for ways to increase data rates still higher than Fast-80 including ISI compensation, increased drive levels, cancellation of bias at the receiver, cable skew cancellation, regular clock periods, and data encoding.

5. Meeting Schedule

The next meetings of SPI-3 Working Group will be:

- Friday, June 19, 1998 from 9 am to 5 pm in Huntington Beach, CA at the Hilton Waterfront Hotel (714-960-7873), hosted by QLogic
- **Tuesday**, July 14, 1998 from 9 am to 6 pm in Portland, ME at the Holiday Inn By the Bay (207-775-2311), hosted by Digital Equipment Corp.

6. Adjournment

The meeting was adjourned at 5:00 p.m. on Friday May 22, 1998.