Accredited Standards Committee*
National Committee for Information Technology Standards (NCITS)

Doc. No.:	T10/98-146r0
Date:	May 12, 1998
Reply to:	John Lohmeyer

To: T10 Membership
From: Ralph Weber / John Lohmeyer
Subject: SPI-3 Working Group Meeting -- May 4, 1998
Colorado Springs, CO

Agenda

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   - 4.2 Load Compensation (97-281) [Novak]
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   - 4.13 Analysis of Fast-80 (98-160r0, 98-161r0, 98-162r0) [Smith]
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   - 4.16 New Expander Proposal (98-158r0) [McGrath]
5. Meeting Schedule
6. Adjournment

Results of Meeting

1. Opening Remarks

John Lohmeyer, the T10 Chair, called the meeting to order at 9:05 a.m., Monday May 4, 1998. He thanked Symbios for allowing him to host the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated. John noted that standards cannot contain known patented material unless the patent holder agrees to comply with the ANSI patent policy.

2. Approval of Agenda

The draft agenda was approved with the following additions and changes:

4.7 Hot Swap Technical Issues (98-155r0) [Uber]
4.11 Simplified Parallel SCSI CRC Proposal (98-150r0) [Gardner]
4.12 Proposal for Fast-80 (98-152r0, 98-153r0) [Milligan]
4.14 CRC Proposal (98-154r0) [Leshay]
4.15 Old Expander Proposal (98-157r0) [McGrath]
4.16 New Expander Proposal (98-158r0) [McGrath]

The following agenda items were added during the course of the meeting:

4.13 Analysis of Fast-80 (98-160r0, 98-161r0, 98-162r0) [Smith]

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for T10 membership. Working group meetings are open to any person or organization directly and materially affected by T10's scope of work. The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Lawrence J. Lamers	P	Adaptec, Inc.	ljlamers@ix.netcom.com
Mr. Vincent Bastiani	A#	Adaptec, Inc.	bastiani@corp.adaptec.com
Mr. Wally Bridgewater	A#	Adaptec, Inc.	wally@eng.adaptec.com
Mr. Mark Delsman	A#	Adaptec, Inc.	mdelsman@corp.adaptec.com
Mr. Steven P. Ego	O	Aeronics Inc.	
Mr. Jeffrey Crockett	V	Aeronics Inc.	jeffreycrockett@worldnet.att.net
Mr. Scott Lindstrom	O	AMP, Inc.	slindstr@amp.com
Mr. Ron Roberts	A	Apple Computer	rkroberts@aol.com
Mr. Robert C. Elliott	P	Compaq Computer Corp.	Robert.Elliott@compaq.com
Mr. Bill Galloway	A	Compaq Computer Corp.	Bill.Galloway@compaq.com
Mr. Charles Tashbook	P	Dallas Semiconductor	charles.tashbook@dalsemi.com
Mr. Greg McSorley	P	Data General / Clariion	greg_mcsorley@dg.com
Dr. William Ham	A#	Digital Equipment Corp.	bill.ham@digital.com
Mr. Don Vohar	A	Fujitsu (FCPA)	dvohar@fcpa.fujitsu.com
Mr. George Penokie	P	IBM Corp.	gop@us.ibm.com
Mr. Dan Colegrove	A#	IBM Corp.	colegrov@us.ibm.com
Mr. Dean Wallace	P	Linfinity Micro	75671.3443@compuserve.com
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Mr. Pete McLean	P	Maxtor Corp.	pete_mclean@maxtor.com
Mr. Jay Neer	A	Molex Inc.	jneer@molex.com
Mr. Chris Millsaps	V	Mylex Corp.	chrism@mylex.com
Mr. Edward A. Gardner	P	Ophidian Designs	eag@ophidian.com
Mr. Skip Jones	P	QLogic Corp.	sk_jones@qlc.com
Mr. Ting Li Chan	A	QLogic Corp.	t_chan@qlc.com
Mr. Chuck Micalizzi	V	QLogic Corp.	c_micalizzi@qlc.com
Mr. James McGrath	A#	Quantum Corp.	JMCGRATH@QNTM.COM
Mr. Bruce Leshay	V	Quantum Corp.	bleshay@tdh.qntm.com
Mr. Richard Uber	V	Quantum Corp.	duber@tdh.qntm.com
Mr. Gene Milligan	P	Seagate Technology	Gene_Milligan@notes.

			seagate.com
Mr. Gerald Houlder	A	Seagate Technology	Gerry_Houlder@notes.seagate.com
Mr. Daniel (Dan) F. Smith	O	Seagate Technology	daniel_f_smith@notes.seagate.com
Mr. Mayank R. Patel	V	Seagate Technology	Masiewicz@notes.seagate.com
Mr. Dave Guss	P	Silicon Systems, Inc.	dave.guss@tus.ssi1.com
Mr. Robert N. Snively	P	Sun Microsystems Computer Co	bob.snively@sun.com
Mr. John Lohmeyer	P	Symbios, Inc.	lohmeyer@ix.netcom.com
Mr. Ralph O. Weber	A	Symbios, Inc.	roweber@acm.org
Mr. Graeme Weston-Lewis	A#	Symbios, Inc.	gwl@symbios.com
Mr. Kevin Bruno	V	Symbios, Inc.	kevin.bruno@symbios.com
Mr. Frank Gasparik	V	Symbios, Inc.	frank.gasparik@symbios.com
Mr. Tracy Spitler	V	Symbios, Inc.	tracy.spitler@symbios.com
Ms. Joy Godbee	V	Symbios, Inc.	joy.godbee@symbios.com
Ms. Kathleen Perkins	V	Symbios, Inc.	kathleen.perkins@symbios.com
Mr. Bill Schmitz	V	Symbios, Inc.	bill.schmitz@symbios.com
Mr. David Steele	V	Symbios, Inc.	david.steele@symbios.com
Mr. Pete Tobias	A#	Tandem, a Compaq Company	tobias_pete@tandem.com
Mr. Paul D. Aloisi	P	Unitrode Corporation	aloisi@unitrode.com
Mr. Jeffrey L. Williams	P	Western Digital Corporation	Jeffrey.L.Williams@wdc.com

47 People Present

Status Key:
- P - Principal
- A,A# - Alternate
- O - Observer
- L - Liaison
- V - Visitor_

4. SPI-3 Topics

4.1 Staged Contact Resistance (98-174) [Herrmann]

In the absence of Hank Herrmann, discussion of this topic was deferred to the July meeting.

4.2 Load Compensation (97-281) [Novak]

Vit Novak was not available to discuss this topic. Questions were raised about whether additional discussion was necessary on this topic. A review of the last meeting minutes indicated that a discussion of where to put the information in SPI-3 should be discussed. Conversely, it was noted that Vit expressed a belief that his presentations were only informational. The group took no action on locating the information found in Vit's presentations in any committee draft document(s).

4.3 Universal Backplane Annex (98-101) [Wallace]

Dean Wallace expressed concerns about the size of the universal backplane annex, 12 pages. George Penokie, Jim McGrath and several others reassured Dean that 12 pages is not too big. Dean repeated his concerns about

the size and asked that discussion be postponed to the next meeting so that he might have a chance to distill the current material. George asked that Dean not distill useful information out of the annex.

4.4 Bias Reduction Proposal (98-156) [Bridgewater]

Wally Bridgewater presented a discussion of how the bias might be moved from the terminator to the transmitter and receiver, considering the timing issues involved. He also described the value of removing the bias during high-speed data transfer phases.

Wally also proposed scheduled reductions in driver strengths, or cutbacks, to address ISI (InterSymbol Interference) problems. The group discussed the “cutback” proposal with attention to how much cutback should occur in any step and how many symbol repetitions before a cutback step would occur.

4.5 Dual Clocking Proposal (97-208) [Bastiani]

Vince Bastiani requested that this item be deferred to the next meeting.

4.6 Test results on dual edge signals (98-113r0) [Bastiani]

Vince Bastiani requested that this item be deferred to the next meeting.

4.7 Hot Swap Technical Issues (98-155r0) [Uber]

Dick Uber presented a discussion of the sequences for pin mating during hot plugging and then showed traces from a sampling oscilloscope. Dick summarized his presentation as follows:

- Hot insertion events DO NOT cause problems during bus free times.
- Hot insertion events DO NOT cause reversals of bus polarity during data transfers.
- Glitches that are superimposed on either asserting or negating transitions have the potential to shift the transition in time. This would cut into the setup and hold time margins.
- Because of the huge time delay between the mating of the contacts for a differential signal pair, the bus may have to operate for an extended time with a load half connected. The imbalance causes a signal distortion, which can affect setup and hold time margins.
- No problems with Hot Swap Case 4 were found during this testing. However, please note that the drives used for this testing measured well under the allowed 20pF capacitance limit.

Dick provided the following conclusions:

- Case-4 Hot Swap has been demonstrated to work satisfactorily.
- Testing has not been exhaustive, and has been limited to one backplane construction and one vendor’s disk drives.

Dan Smith noted that Seagate has observed similar results in their testing.

The SPI-2 description of case 4 hot-plugging was reviewed. Gene Milligan closed the discussion by noting that it is hard to say you will not get errors and difficult to say you will never get undetectable errors. Gene concluded that everything points to the importance of adding CRC when the transfer rates are increased.

4.8 QAS review (97-199r8) [Moore/Lamers]

Larry Lamers presented the latest revision of the QAS proposal (97-199r8). Questions were raised regarding statements in section 3.4 (Mixed Bus Blocking Relief). George Penokie agreed to review section 3.4 carefully and provide comments to Larry.

The need for showing QAS capability in the Inquiry data surfaced, and Larry reminded the group that a proposal on that topic has been waiting for resolution of the 97-199 issues and will be brought to the next meeting. Based on other discussion issues concerning section 3.4, Larry agreed to propose adding a bit to the control mode page to control the fairness algorithm as part of the Inquiry data (SPC-2) proposal.

Bruce Leshay repeated his concerns about snooping the bus for a 55h as a message byte value. Several cases were discussed and none produced the problems that Bruce could show to be fatal.

Larry presented a timing comparison showing some QAS features (98-159). The group asked that the presentation be enhanced to compare QAS and non-QAS timings. Larry agreed to revise the charts for the July meeting.

4.9 CRC on existing SCSI parallel protocol (98-144r1) [Penokie]

George Penokie provided a quick overview of his CRC proposal. One issue raised concerned the potential requirement that the initiator crack the data returned for commands such as Inquiry that may return less data than requested. George requested that rather than dealing with the outstanding problems of his proposal, he would rather hear the other CRC proposals (see items 4.11 and 4.14). After all three proposals are heard, the group can begin resolving issues.

4.10 Terminator Power voltage level [Wallace]

Dean Wallace asked that this item be removed from future agenda.

4.11 Simplified Parallel SCSI CRC Proposal (98-150r0) [Gardner]

Ed Gardner presented a proposal using a specifically encoded new bus phase, a CRC phase (actually specific instances of the Data Out and Data In bus phases). Ed noted that the weakness of the proposal is the extra time required turn the bus around from input to output or vice versa. The CRC discussion continued with Bruce Leshay's presentation (see item 4.14).

4.12 Proposal for Fast-80 (98-152r0, 98-153r0) [Milligan]

Gene Milligan presented 98-152r0, an overview of a Fast-80 proposal (called Fast 80ish in the presentation), and distributed a proposal (98-153r0) containing specific changes and additions to SPI-3 to support double-clocking Fast-80. Questions were raised about the relative values of the proposed Transmit Hold Time and Transmit Assertion Period. It was agreed that the two 8 ns numbers in the proposed Table 1 should be 10.55 ns.

Noting that time would be required to read the specific changes proposal, the group requested two special ad hoc meetings to discuss Fast-80 issues. The agreement on ad hoc meetings is reflected in item 5.

4.13 Analysis of Fast-80 (98-160r0, 98-161r0, 98-162r0) [Smith]

Dan Smith presented three sets of test data supporting the proposed Fast-80 timings (98-160r0, 98-161r0 and 98-162r0). Dan noted that his measurements differed from those shown earlier by Wally Bridgewater. The test methodology was reviewed and Dan received some suggestions for improved future tests.

4.14 CRC Proposal (98-154r0) [Leshay]

Bruce presented a proposal that the Parity signal be reused as a CRC_Valid signal for transfers where double-edge clocking is used. He described the reasoning that concluded with the proposal to reuse the Parity signal. Concerns were raised about the use of the Parity (CRC_Valid) signal during Data Out phase, as that use would require the signal to be driven in the opposite direction from the data.

At the conclusion of all the CRC proposal presentations, George suggested that his proposal (98-144r1) be set aside. Questions were raised about possible patents on the Bruce Leshay and Ed Gardner proposals. Ed say that he would not be applying for a patent and the Quantum representatives said that any patents covering the 98-154 proposal would be licensed at no cost.

The group reduced the description of the choices to a choice between a high performance CRC implementation that breaks existing bus expanders and lower performance CRC implementation that does not break existing bus expanders. With that realization, the group moved to discussion of the new expander proposal (98-158r0, see 4.16).

4.15 Old Expander Proposal (98-157r0) [McGrath]

Jim McGrath started by saying that any change in the SCSI protocols “might” break existing bus expanders. The essence of Jim’s proposal was an effort to test the operation of a newly negotiated set of transfer parameters, particularly double-edge clocking. Jim described a testing method that would rely on exchanging commands between the target and initiator, which met resistance from the group.

Jim’s preferred testing method used Data In and Data Out (what might be called unsolicited Data In and Data Out, because they are not the result of a command). Data received by the initiator during a Data In phase would be automatically repeated back to the target during the immediately subsequent Data Out phase. The group discussed the mechanics of the Data I/O method.

One addition to the proposal was requiring that the Data I/O testing be bracketed by messages clearly showing when the testing starts and end. The number of bytes to be transferred during the Data I/O testing was discussed, with options such as the REQ/ACK offset value or some other explicit value. Jim agreed to prepare a specific proposal for the July meeting.

4.16 New Expander Proposal (98-158r0) [McGrath]

Jim presented a proposal that a new message byte precede the Identify message. The new message would be distinguishable from the Identify because bit 7 would be zero. The low order nibble of the proposed new message would describe the transfer properties of the I_T nexus that follows. The information communicated by the new message could be snooped by expanders to determine the transfer properties of the I_T nexus, thus eliminating some amount of state knowledge required in the bus expander. The intent of the proposal was providing bus expanders information about the transfer parameters of the data phase(s) to follow in the current connection.

Concerns were raised about the new message breaking long-standing rules about Identify messages coming first. Alternatives were raised but not found acceptable. Questions were raised about the need for the capability, to which Bill Galloway and Dave Steele answered that the capability definitely would be required to identify the use of double-edge clocking. The expander cannot dynamically determine that double-edge clocking is being used and modify its handling of the data signals fast enough.

The consensus was that a new message be defined to provide the results of a transfer parameters negotiations to bus expanders. Jim asked the group to consider the consensus idea overnight and bring thoughts to the EPI portion of the SCSI Working Group. Based on the results of the SCSI Working Group, Jim agreed to take responsibility for writing a new proposal reflecting the opinions expressed the next day.

Chair’s note: Later in the week other proposals were presented for communicating the use of double-clocking to bus expanders that seemed to have better consensus. See items 4.2 and 7.2 in 98-147.

5. Meeting Schedule

The next meetings of SPI-3 Working Group will be:

- May 22, 1998 from 9 am to 5 pm hosted by Seagate in Chicago, IL at the O'Hare Hilton (773-686-8000),
- June 19, 1998 from 9 am to 5 pm in Huntington Beach, CA hosted by QLogic at the Hilton Waterfront Hotel (714-960-7873), and
- July 13, 1998 from 9 am to 8 pm in Portland, ME hosted by Digital Equipment Corp. at the Holiday Inn By the Bay (207-775-2311).

6. Adjournment

The meeting was adjourned at 6:44 p.m. on Monday May 4, 1998.