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Reply to: John Lohmeyer

To: Membership of T10

From: John Lohmeyer, Chair T10

Subject: Minutes of SPI-3 Physical Study Group
January 21, 1998 -- Irvine, CA

Agenda

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Results of Meeting

1. Opening Remarks

John Lohmeyer, the T10 Chair, called the meeting to order at 9:00 a.m., Wednesday January 21, 1998. He thanked Skip Jones of QLogic for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated.

2. Approval of Agenda

The agenda was approved. Vince Bastiani asked that items 4.4 be deferred until March. Bob Atkinson (AMP) did not know why item 4.1 was added and asked that it be deferred until March.

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for T10 membership. Working group meetings are open to any person or organization directly and materially affected by T10's scope of work. The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Vincent Bastiani	A#	Adaptec, Inc.	bastiani@corp.adaptec.com
Mr. Tak Asami	V	Adaptec, Inc.	asami@itc.adaptec.com
Mr. Wally Bridgewater	V	Adaptec, Inc.	wally@eng.adaptec.com
Mr. Richard Moore	V	Adaptec, Inc.	richard_moore@corp.adaptec.com
Mr. Scott Lindstrom	V	AMP Incorporated	slindstr@amp.com
Mr. Bob Atkinson	O	AMP, Inc.	rdatkins@amp.com
Dr. William Ham	A#	Digital Equipment Corp.	bill.ham@digital.com
Mr. Mike Fitzpatrick	V	Fujitsu CPA	mfitzpatrick@fcpa.fujitsu.com
Mr. Sam Ray	V	IBM	str@almaden.ibm.com
Mr. George Penokie	P	IBM Corp.	gop@us.ibm.com
Mr. Jay Neer	A	Molex Inc.	jneer@molex.com
Mr. Skip Jones	P	QLogic Corp.	sk_jones@qlc.com
Mr. Ting Li Chan	A	QLogic Corp.	t_chan@qlc.com
Mr. Chuck Micalizzi	V	QLogic Corp.	c_micalizzi@qlc.com
Mr. Fardad Siavoshi	V	QLogic Corp.	f_siavoshi@qlc.com
Mr. Patrick McGarrah	P	Quantum Corp.	pmcgarra@tdh.qntm.com
Mr. Richard Uber	V	Quantum Corp.	duber@tdh.qntm.com
Mr. Daniel (Dan) F. Smith	O	Seagate Technology	daniel_f_smith@notes.seagate.com
Mr. John Lohmeyer	P	Symbios, Inc.	john.lohmeyer@symbios.com
Ms Yang Jiao	V	TEAC	yjiao@teac.com
Mr. Peter Baril	V	Temp-Flex Cable Inc.	pbaril@worldnet.att.net
Mr. William McMaken	V	Trimm Technologies	bmcmaken@trimm.com
Mr. Darryl Froman	V	UNISYS Corporation	
Mr. Paul D. Aloisi	P	Unitrode Corporation	aloisi@unitrode.com
Mr. Doug Piper	P	Woven Electronics	doug.piper@internetmci.com

25 People Present

Status Key:
- P - Principal
- A,A# - Alternate
- O - Observer
- L - Liaison
- V - Visitor

4. Old Business

4.1 Low-Attenuation Cables (97-213, 97-228) [Rogers, Bellino]

Since no one has been present to address these proposals for several meetings, this agenda item will be dropped.

4.2 Staged Contact Resistance [Amp]

John Lohmeyer briefly reviewed the idea of a staged contact design previously disclosed by Bill Ham of Digital and documented in the minutes of a previous working group meeting. It includes a non-metallic lead-in section

that absorbs the electrical transitions slowly and the mated metallic section of the contact is low-impedance for in service use. The idea is that the high-impedance section charges the contact to the actual bus voltage minimizing the effects of hot plugging. Bob Atkinson noted that AMP is investigating such a connector, but he was not prepared to discuss it now. He asked to defer the topic until March.

4.3 Bias Reduction Proposal (97-214) [Bridgewater]

Wally Bridgewater asked that this topic be deferred until March.

4.4 Dual Clocking Proposal (97-208) [Bastiani]

Vince Bastiani asked that this topic be deferred until March.

5. New Business

5.1 Initial test results on dual clock signals (98-113r0) [Bastiani]

Vince Bastiani presented 98-113r0 on initial test results with dual-edge clocks. As usual, there were a number of questions about the test setup and why particular values were selected. The data supports the idea that dual-edge clocking is feasible, but more testing is needed and planned.

Several of the test setups involved a relatively long cable from the driver to a series of closely spaced receivers. The signals were generally confirmed previous data where the worst signals were seen at the first receiver and much-improved signals at the second and subsequent receivers. Bill Ham noted that the idea of a signal "breakwater" ahead of the first real device was a valid approach that could be realized by adding a simple lumped capacitor.

It was noted that the clock signal used for the test was very regular. In the real world, it will not be as regular.

Vince said that he expects to have a test chip before the March meeting.

5.2 Discussion on using eye pattern for specification (98-113r0) [Bastiani]

Vince Bastiani noted that eye patterns might not be entirely relevant to testing parallel buses because of signal skew. Bill Ham pointed out that people who use eye patterns do so because they are forced to use sampling techniques due to very fast signals. SCSI does not have this problem since the signals are still within analog scope ranges and does not need to resort to using eye patterns. Using color grade type plots can be valuable for non-correlated signals to quickly determine the extremes of the waveforms. This can look like an eye and could be valuable.

There was some discussion about the term 'cable skew' on page 18 of Vince's presentation. It perhaps should include other skews beyond just the cable skew.

Briefly, the idea of skew compensation was discussed. Most people believed that Fast-80 will not require skew compensation, but we may want to lay the groundwork for future generations of SCSI. Skew compensation will require some protocol changes to provide training patterns.

5.3 Need for error detection on dual-edge clocks (98-144r0) [Gintz]

Bill Gintz gave a presentation (98-114r0) on the need for more robust error detection mechanisms when hot plugging with dual-edge clocking. Bill Ham said that the glitches that Bill Gintz showed were very similar to those he had previously measured and presented in March 1997.

There was discussion regarding the probability that the glitches would introduce any undetected errors. Bill Gintz was concerned that a plugging glitch on REQ or ACK could move the clocking point for all the data lines. This could introduce multiple-bit errors and overwhelm the parity mechanism, which only reliably detects single-bit errors.

Staged resistance connector contacts is one solution to the plugging glitches. It works by spreading out the energy of the plugging event. Adding a CRC to SCSI is another solution. It doesn't prevent the glitches, but it would more reliably detect the errors.

It was noted that there are other mechanisms (e.g., firmware errors, ESD) that are more likely to produce undetected errors. Adding a more robust error detection scheme would help with some of these mechanisms, but not others. John Lohmeyer noted that adding CRC would impact development costs, but should have little or no impact on product costs; a staged contact would likely add cost to each connector.

Bill Gintz said he had a test setup that allows him to inject a short pulse anywhere within a data pattern provided he has control of the system clock. This is quite useful in testing for worst-case timing shifts due to plugging events.

Bill Ham noted that some rather unexpected mechanisms might be present during plugging events. He has observed some data that might be explained by high current densities melting the contact point. He mentioned an article he had written in the *Digital Technical Journal*, December 1997 issue, on this topic. Bill plans to bring copies of the article to the March meeting.

5.4 Hot plugging concerns [Gintz]

See 5.3, above.

6. Meeting Schedule

The next meeting of SPI-3 Working Group will be March 16, 1998, in San Diego, CA at the Hyatt Islandia Hotel (619-224-1234), hosted by QLogic.

7. Adjournment

The meeting was adjourned at 11:55 a.m. on Wednesday January 21, 1998.