Accredited Standards Committee*
X3, Information Technology

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Reply to: John Lohmeyer

To: Membership of X3T10

From: Ralph Weber, X3T10 Secretary
Bill Ham, SPI-2 Technical Editor
Larry Lamers, Vice Chair X3T10

Subject: Minutes of SPI-2 LVD Working Group Meeting
San Diego, CA -- March 11, 1996

Agenda

1. Opening Remarks

2. Approval of Agenda

3. Attendance and Membership

4. Test Data (96-141) [Ham]

5. Transmission Line Model (96-123 & -124) [Gingerich]

6. Timing Budget [Ham]

7. SPI-2 Document Review (X3T10/1142D) [Ham]

8. Releasing Bus from Active Negation [Uber]
   8.1 Digital Filtering of Negation Release Glitches [Lohmeyer]

9. Standing Waves [Bridgewater]

10. Termination Balance [Ham]

11. Glitch Filtering [Ham]

12. Drive Currents [Moore]

13. Meeting Schedule

14. Adjournment

Results of Meeting

1. Opening Remarks

Larry Lamers, the X3T10 Vice-Chair, called the meeting to order at 9:00 a.m., Monday March 11, 1996. He thanked Skip Jones of QLogic for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated.

2. Approval of Agenda

The agenda was approved with the following additions:

10. Termination Balance [Ham]
11. Glitch Filtering [Ham]
12. Drive Currents [Moore]

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work. The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Norm Harris	P	Adaptec, Inc.	nharris@eng.adaptec.com
Mr. Lawrence J. Lamers	A	Adaptec, Inc.	ljlamers@aol.com
Mr. Tak Asami	A#	Adaptec, Inc.	asami@dt.wdc.com
Mr. Wally Bridgewater	V	Adaptec, Inc.	wally@eng.adaptec.com
Mr. Richard Moore	V	Adaptec, Inc.	richard_moore@corp.adaptec.com
Mr. Edward Fong	P	Amdahl Corp.	esf10@amail.amdahl.com
Mr. Ron Roberts	A	Apple Computer	rkroberts@aol.com
Dr. Benjamin Monderer	V	Box Hill Systems Corp.	ben@boxhill.com
Mr. Clifford E. Strang Jr.	P	BusLogic	skip@buslogic.com
Mr. Louis Grantham	P	Dallas Semiconductor	grantham@dalsemi.com
Mr. Siegfried Schmalz	V	Dallas Semiconductor	schmalz@dalsemi.com
Mr. Ken Jeffries	V	Dell Computer Corporation	ken@volente.us.dell.com
Dr. William Ham	A#	Digital Equipment Corp.	ham@subsys.enet.dec.com
Mr. Roger Cummings	O	Distributed Processing Tech.	cummings_roger@dpt.com
Mr. Ralph O. Weber	P	ENDL Associate	roweber@acm.org
Mr. Mike Chennery	A#	Fujitsu	mchenery@fcpa.fujitsu.com
Mr. Andy Chen	A	Fujitsu Computer Prods Amer	achen@fcpa.fujitsu.com
Mr. Dan Colegrove	A#	IBM Corp.	colegrove@vnet.ibm.com
Mr. Dan Strevey	V	Intellistor, Inc.	dstrevey@intellistor.com
Mr. Dean Wallace	P	Linfinity Micro	75671.3443@compuserve.com
Mr. Wayne E. Werner	O	Lucent Technologies	wew@alupo.att.com
Mr. Ting Li Chan	A	QLogic Corp.	t_chan@qlc.com
Mr. John A. Fobel	O	Rancho Technology, Inc.	scsi@trancho.com

Mr. Gene Milligan	P	Seagate Technology	Gene_Milligan@notes.seagate.com
Mr. Gerald Houlder	A	Seagate Technology	Gerry_Houlder@notes.seagate.com
Mr. Brian N. Davis	A#	Seagate Technology	brian_davis@notes.seagate.com
Mr. Dave Guss	P	Silicon Systems, Inc.	dave.guss@tus.ssi1.com
Mr. Daniel E. Moczarny	V	Silicon Systems, Inc.	dan.moczarny@tus.ssi1.com
Mr. Robert N. Snively	P	Sun Microsystems Computer Co	bob.snively@eng.sun.com
Mr. John Lohmeyer	P	Symbios Logic Inc.	john.lohmeyer@symbios.com
Mr. Pete Tobias	A	Tandem Computers	tobias_pete@tandem.com
Mr. Kevin Gingerich	V	Texas Instruments	4307725@mcimail.com
Mr. Tokuyuki Totani	P	Toshiba America	totani@tix.netcom.com
Mr. Kenneth J. Hallam	P	UNISYS Corporation	ken.hallam@mv.unisys.com
Mr. Paul D. Aloisi	P	Unitrode Integrated Circuits	Aloisi@uicc.com

35 People Present

Status Key: P - Principal
A,A# - Alternate
O - Observer
L - Liaison
V - Visitor

4. Test Data (96-141) [Ham]

Bill Ham presented test data that was so hot off of the oscilloscope that he had not fully analyzed it. The data was based on a controlled load board, a tool that allows the placement of a known load on a SCSI bus. In the discussion, Bill noted that the tests used a symmetrical driver, because he has been unable to build an asymmetrical driver from discrete components.

One significant conclusion Bill reached based on the testing was that a glitch filter is needed. This is caused by reflections from clustered loads much as in the single ended case defined in SPI-2. The glitch filter would operate by ignoring the signal state for between 5 ns and 7 ns after a transition is recognized. It was noted that this does not mean that a 5 to 7 ns low pass analog filter be used. Digital filtering was recommended.

Bill's test configuration usually involved several loads placed near one terminator with a long (often 26 m) run of unloaded cable to the driver and other terminator. In several cases, Bill showed that 20 pF loads cause unacceptable signal degradation in this configuration. He also showed that a lower per-node capacitance budget, such as 10 pF, produced a much better signal to the point where adequate margin was seen. This result is highly dependent on the bus length and other physical configuration parameters. The worst case occurred when a long string of one bits was followed by a single zero bit (or vice versa). The first changed bit signal had the lowest margin. It was noted that this effect is precisely what causes the need for d.c. balance in a manner similar to 8b-10b.

5. Transmission Line Model (96-123 & -124) [Gingerich]

Bill Ham had incorporated the model in Annex B of the SPI-2 revision 5. As part of the SPI-2 review, Kevin Gingerich walked the group through the Annex B. One of the first steps was to remove all references to EIA/TIA documents. A complete set of tests and limits are now in place for the LVD SCSI transceivers.

6. Timing Budget [Ham]

Rev 05 contained a proposal for a specific method for defining the timing parameters: assertion period, negation period, set up time, and hold time. This proposal followed the Fast-20 model. This turned out to be one of the most useful parts of the meeting because it forced real consideration of the receiver thresholds.

The issue identified was the behavior of real receivers with respect to the idea that they have a 30 mV sensitivity. This 30 mV level was the d. c. level or the level to be used if the differential signal for assertion is approximately the same as the differential signal for the negation. However, when the differential signal for the assertion is large (as with a long series of "1's" and the negation signal is small (as with a short "0") the actual receiver threshold must be larger for the negation detection (if the same timing values are to be met). This is caused by "precharging" within the receiver circuitry with the long assertion that must be discharged and recharged by the short negation. This observation is critical in determining what an acceptable signal really is and will significantly affect the configurations that are possible.

The present thinking is that one should use a negation threshold that is 0.25 times the assertion voltage level prior to the negation. This allows a very deterministic way of evaluating signals for their acceptability.

The above discussion also applies to the complementary transitions from negation to assertion.

This impact of this on the acceptability of different configurations is not presently known.

7. SPI-2 Document Review (X3T10/1142D) [Ham]

Bill distributed revision 5 of the SPI-2 proposed working draft, dated March 11, 1996. See other sections of these minutes for the details of this review.

8. Releasing Bus from Active Negation [Uber]

Richard Uber was not present. Discussion of this topic was deferred to the next meeting. It was decided at the last meeting that it would be required for devices to ignore glitches for a bus settle delay after release from active negation. It is not clear that this item needs further discussion.

8.1 Digital Filtering of Negation Release Glitches [Lohmeyer]

Discussion of this topic was deferred to the next meeting.

9. Standing Waves [Bridgewater]

This subject was not addressed at this meeting but still needs review. Continue to keep this item active.

10. Termination Balance [Ham]

The group discussed the termination balance test as part of the proposed working draft document review. This subject was addressed as a result of reflector traffic that pointed out that the specification in rev 04 was not possible to meet. After a lot of good discussion it was decided to adopt the proposed wording in rev 05 but to remove the hard limits on delta Vmin and delta V max. This test is still viewed as a balance test for the LVD SCSI terminators and will remain in the standard.

11. Glitch Filtering [Ham]

During the presentation of his test data, Bill noted the need for a digital glitch filter on all signals. The glitch filter Bill described would ignore all signal activity for between 5 ns and 7 ns after a transition has been recognized.

12. Drive Currents [Moore]

Due to lack of time this item was not addressed at this meeting.

13. Summary of Results

The group agreed that development of the SPI-2 standard is not yet complete. A major area of concern was the impact of the revised view of the receiver threshold on the allowed configurations. The group agreed to a target of stabilizing the LVD SCSI portions of SPI-2 at the May meeting.

14. Meeting Schedule

Pending approval by X3T10, the next meeting of SPI-2 Working Group will be Monday-Tuesday April 22-23, 1996, in San Jose, CA at the Sheraton Inn Milpitas, CA (408-943-0600) hosted by Adaptec. Another SPI-2 Working Group meeting will be held May 6, 1996 in Fort Lauderdale, FL.

15. Adjournment

The meeting was adjourned at 5:09 p.m. on Monday March 11, 1996.