Accredited Standards Committee*
X3, Information Technology

To: Membership of X3T10

From: Ralph Weber, Secretary X3T10
              John Lohmeyer,Chair X3T10
              Bill Ham, SPI-2 Technical Editor

Subject: Minutes of X3T10 SPI-2 LVDS Working Group Meeting
              Dallas, TX -- January 8, 1996

Agenda

1. Opening Remarks

2. Approval of Agenda

3. Attendance and Membership

4. SPI-2 Document Review (X3T10/1142D) [Ham]

5. Releasing Bus from Active Negation [Uber]

6. Voltage Mode Drivers [Bridgewater]

7. Meeting Schedule

8. Adjournment

Results of Meeting

1.   Opening Remarks

John Lohmeyer, the X3T10 Chair, called the meeting to order at 9:03 a.m., Monday January 8, 1996. He thanked Jim McGrath of Quantum for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated.

2.   Approval of Agenda

Bill Ham noted that the draft agenda is very general and that details would be needed. But, he agreed to handle the details under the appropriate general headings. The draft agenda was approved without changes.

3.   Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work. The following people attended the meeting:

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        Name            S       Organization        Electronic Mail Address
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Mr. Norm Harris         P  Adaptec, Inc.            nharris@eng.adaptec.com
Mr. Lawrence J. Lamers A#  Adaptec, Inc.            ljlamers@aol.com
Mr. Wally Bridgewater   V  Adaptec, Inc.            wally@eng.adaptec.com
Mr. Richard Moore       V  Adaptec, Inc.            richard_moore@corp.adapte
                                                    c.com
Mr. Richard B. Rauch    V  APCON, Inc.              rbr@apcon.com
Mr. Dennis R. Haynes    O  Burr-Brown Corp.         haynes_dennis@bbrown.com
Mr. Justin McEldowney   V  Burr-Brown Corp.         mceldowney_justin@bbrown.
                                                    com
Mr. Jaff Lin            A  BusLogic                 jaffl@buslogic.com
Mr. Lyle Conn           V  Conner Peripherals       lyle.conn@conner.com
Mr. Louis Grantham      P  Dallas Semiconductor     grantham@dalsemi.com
Dr. William Ham        A#  Digital Equipment Corp.  ham@subsys.enet.dec.com
Mr. Ralph O. Weber      P  ENDL Associate           roweber@acm.org
Ms. Nancy Cheng        A#  Hitachi Computer Products n_cheng@hitachi.com
Mr. George Penokie      P  IBM Corp.                gop@rchvmp3.vnet.ibm.com
Mr. Dan Colegrove      A#  IBM Corp.                colegrove@vnet.ibm.com
Mr. Dean Wallace        P  Linfinity Micro          75671.3443@compuserve.com
Mr. Frank Samela        A  Methode
Mr. Edward A. Gardner   V  Ophidian Designs         gardner@acm.org
Dr. Akira James Miura   A  Panasonic Technologies,  miura@tadw.research.panas
                           Inc                      onic.com
Mr. Skip Jones          P  QLogic Corp.             sk_jones@qlc.com
Mr. Ting Li Chan        A  QLogic Corp.             t_chan@qlc.com
Mr. Mark Evans          A  Quantum Corp.            mevans@qntm.com
Mr. Richard Uber        V  Quantum Corp.            duber@tdh.qntm.com
Mr. Gene Milligan       P  Seagate Technology       Gene_Milligan@notes.seaga
                                                    te.com
Mr. Gerald Houlder      A  Seagate Technology       Gerry_Houlder@notes.seaga
                                                    te.com
Mr. Dave Guss           A  Silicon Systems, Inc.    dave.guss@tus.ssi1.com
Mr. Daniel E. Moczarny  V  Silicon Systems, Inc.    dan.moczarny@tus.ssi1.com
Mr. Robert N. Snively   P  Sun Microsystems Computer bob.snively@eng.sun.com
                           Co
Mr. John Lohmeyer       P  Symbios Logic Inc.       john.lohmeyer@symbios.com
Mr. Frank Gasparik      V  Symbios Logic Inc.       frank.gasparik@symbios.co
                                                    m
Mr. Kevin Gingerich     V  Texas Instruments        4307725@mcimail.com
Mr. John Wilson         V  Texas Instruments        jwilson@asic.sc.ti.com
Mr. Paul D. Aloisi      P  Unitrode Integrated      Aloisi@uicc.com
                           Circuits
Mr. Matthew Thomas      A  Unitrode Integrated      thomasm@uicc.com
                           Circuits
Mr. Tak Asami           A  Western Digital          asami@dt.wdc.com
                           Corporation
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35 People Present

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Status Key:  P    -  Principal
             A,A# -  Alternate
             O    -  Observer
             L    -  Liaison
             V    -  Visitor
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4.   SPI-2 Document Review (X3T10/1142D) [Ham]

Bill Ham expressed concern about signal glitches after bus settle delay. John Lohmeyer said that his discussion have indicated that it will not be a problem. Dave Guss said that the glitches would not be problems for targets but could represent problems for hosts, because they are required to detect levels set by the targets. John (representing hosts) became less certain about glitch problems.

Bill Ham approached the day's work with the goal of writing improved wording about required behavior after release from negation. Almost every topic discussed for the remainder of the day was cast in terms of its effect on reducing the glitch problem. In this regard, it was noted that glitches when the bus is released normally are the most common problem, but glitches during unexpected bus free may produce the most difficult to predict problems.

Kevin Gingerich presented a detailed model representing a differential bus in both DC and AC terms. He described all aspects of the model and suggested that the group would benefit from adopting the model (or one like it) as a development tool for examining bus properties.

Bill presented a new diagram for representing the capacitance loading restrictions to be placed on device. The group decided that the diagram was confusing and returned to a tabular representation for the data.

Stub length (previously set at 0.2m) was discussed. It was agreed to reduce the total stub length to 0.1m and splitting the 0.1 equally between inside and outside the device.   Bill noted that the draft document will be changed but that future discussions probably will revisit the stub length issue.

Limits on the differences between stub line lengths for several signals were discussed. Bill described the need for restricting differences in stub line lengths as being skew management. The need was generally agreed. But, several problems were raised regarding the details of the specification. Very strict limits on differences in stub lengths were discussed. However, the very strict limits were dismissed because they might prevent the usage of BGA chip technologies.

Kevin Gingerich and Bill Ham led a discussion of test circuits. Several complexities were raised and reviewed. Bill concluded that the group had reached the point where the meeting discussion should end and people should return to their offices to develop experimental circuits and collect test data.

By the end of the meeting, Bill had developed the following list of agreed assumptions:

    A device load of 20 pF +/- 1 pF

    A stub length of 0.1 m

    30 mV receivers

    110-135 Ohms cable impedance
    110-115 Ohms terminators

    Requiring cable to have a capacitance/length of 15-50 pF/ft

A major result of the discussions was an agreement that the electrical circuits will be specified in ways that eliminate glitch problems when releasing the bus. At this time, using different assertion and negation levels seems to be the best (or only) solution for the problem.

5.   Releasing Bus from Active Negation [Uber]

Richard Uber presented a circuit that he felt would be immune to glitches as the target goes bus free. Wally Bridgewater described an electrical problem with the proposal, part of which was related to higher power consumption.

6.   Voltage Mode Drivers [Bridgewater]

Wally Bridgewater presented a revised proposal for voltage mode drivers. He stated that, after further consideration, the only difference between current mode drivers and voltage mode drivers is where the resisters are located. Also, the voltage mode dissipates less power on the chip, but more power overall.

Bill's conclusion was that the goal of the standard should be to tell people what to do not how to build the circuits to do it.

7.   Meeting Schedule

The next meeting of SPI-2 Study Group will be Monday March 11, 1996, in San Diego, CA at the Hyatt Islandia (619) 22401234, hosted by Quantum Corp. Another SPI-2 Study Group meeting is scheduled for February 5, 1996 in Denver, CO hosted by Symbios Logic -- It appears that the February 5 meeting will be re-scheduled due to a conflict with an FC-0 meeting and the need for a two-day meeting to meeting the March '95 stability deadline. Tentatively, the meeting will be moved to January 29-30, 1996 still in Denver, CO.

8.   Adjournment

The meeting was adjourned at 5:29 p.m. on Monday January 8, 1996.