Accredited Standards Committee*
X3, Information Technology

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Reply to: John Lohmeyer

To: Membership of X3T10

From: John Lohmeyer, Chair X3T10
Bill Ham, SPI-2Technical Editor

Subject: Minutes of X3T10 SPI-2 LVDS Working Group Meeting
Milpitas, CA -- December 15, 1995

Agenda

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Results of Meeting

1. Opening Remarks

John Lohmeyer, the X3T10 Chair, called the meeting to order at 9:30 a.m., Friday December 15, 1995. He thanked Jim McGrath of Quantum for hosting the meeting.

As is customary, the people attending introduced themselves and a copy of the attendance list was circulated.

2. Approval of Agenda

The agenda was developed at the meeting.

3. Attendance and Membership

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or organization directly and materially affected by X3T10's scope of work. The following people attended the meeting:

Name	S	Organization	Electronic Mail Address
Mr. Norm Harris	P	Adaptec, Inc.	nharris@eng.adaptec.com
Mr. Wally Bridgewater	V	Adaptec, Inc.	wally@eng.adaptec.com
Mr. Richard Moore	V	Adaptec, Inc.	richard_moore@corp.adaptec.com
Mr. Simon Ngo Sy	V	Adaptec, Inc.	simonn@eng.adaptec.com
Mr. Chris Burns	V	Adaptec, Inc.	chrisb@eng.adaptec.com
Mr. Dennis R. Haynes	O	Burr-Brown Corp.	haynes_dennis@bbrown.com
Mr. Richard Kulavik	V	Burr-Brown Corp.	kulavik_Richard@bbrown.com
Mr. Jaff Lin	V	BusLogic	jaffl@buslogic.com
Mr. Joe Chen	P	Cirrus Logic Inc.	chen@cirrus.com
Dr. William Ham	A#	Digital Equipment Corp.	ham@subsys.enet.dec.com
Ms. Nancy Cheng	A#	Hitachi Computer Products	n_cheng@hitachi.com
Mr. Dan Colegrove	A#	IBM Corp.	colegrove@vnet.ibm.com
Mr. Richard Greenberg	V	IBM Corp.	richg@vnet.ibm.com
Mr. Dean Wallace	P	Linfinity Micro	75671.3443@compuserve.com
Mr. Ting Li Chan	A	QLogic Corp.	t_chan@qlc.com
Mr. Richard Uber	V	Quantum Corp.	duber@tdh.qntm.com
Mr. Farrokh Mottahedin	V	Quantum Corp.	fmottahe@qntm.com
Mr. Brian N. Davis	A#	Seagate Technology	brian_davis@notes.seagate.com
Mr. Dave Guss	A	Silicon Systems, Inc.	dave.guss@tus.ssi1.com
Mr. Bob Masterson	V	Sonoran Tech.	rwmast@aol.com
Mr. Vit Novak	A	Sun Microsystems, Inc.	vit.novak@sun.com
Mr. John Lohmeyer	P	Symbios Logic Inc.	john.lohmeyer@symbios.com
Mr. Mark Jander	V	Symbios Logic Inc.	mark.jander@symbios.com
Mr. Pete Tobias	A	Tandem Computers	tobias_pete@tandem.com
Mr. Kevin Gingerich	V	Texas Instruments	4307725@mcimail.com
Mr. Paul D. Aloisi	P	Unitrode Integrated Circuits	Aloisi@uicc.com

26 People Present

Status Key:
- P - Principal
- A,A# - Alternate
- O - Observer
- L - Liaison
- V - Visitor

4. SPI-2 Document Review (X3T10/1142D) [Ham]

Terminator specification:

Bill Ham discussed the changes to the LVDS terminator specification.

The first area of discussion was the differential impedance requirement. The new test circuit developed at the last working group was discussed. The method of specifying this performance requirement was accepted but the

actual values of the resistance were questioned. Based on earlier inputs from Unitrode that the sign of the reflections should always be such that the terminator is lower impedance than a loaded bus a set of lower numbers for the terminator were included in the draft standard. These lower numbers decrease the signal amplitude and were not accepted. Further it was noted (see below) that the leakage current from devices could have a significant effect on the terminator bias. This was noted and placed on a list of concerns. The issue was not resolved in this meeting. It was noted that a more sensitive receiver would be very beneficial here.

A value of slightly over 100 ohms was deemed to be optimal for the nominal terminator resistance.

Output leakage current:

After some discussion, the output pin off current was specified at +/- 20 uA. This level is required to accommodate 2.5 V IC processes that have higher leakage than % or 3.3V processes. This raised the question of what happens on a fully-loaded bus when all the devices are leaking at the same extreme of this specification (15 * +/- 20 uA = +/- 300 uA total leakage current).

Terminator common-mode impedance test circuit:

See Table 3 and Figure 3. Kevin Gingerich suggested that the specification should include AC characteristics over the range of DC to 300 MHz. Eventually, we settled on a range of DC to 1 MHz since only the common mode noise needs to be accommodated -- not the SCSI signals. This test was accepted as valid with the addition of the frequency requirements.

Terminator balance test:

This test measures the balance of the terminator between the two sides. Any curve within the box (Vmin to Vmax and delta Vmin to delta Vmax) is legal. A 10 mV imbalance was allowed. Specified frequency range is DC to 1 MHz. This test was accepted as valid with the addition of the frequency requirements.

Driver current requirements:

Late in the afternoon, we re-visited the signal budget again. Bill developed a model of the driver and receivers, including crosstalk, leakage current, unbalanced termination, and the receiver sensitivity of 70 mV. We do not have much margin for cable loading or attenuation with a 5 mA current mode driver and the present common mode range. It appears that we need to increase the driver current again, perhaps to around 7 or 8 mA. Or we need to increase the receiver sensitivity and reduce the terminator bias voltage. Limiting the common mode range is another possibility. There are other ways to keep the chip power dissipation down that can be applied. Stay tuned.

5. Setup Time Budget (96-103) [Bridgewater]

Wally Bridgewater presented a Proposed Change for Setup Time Budget (96-103). It contains a justification for changing the setup time for Fast-40 from 5 ns to 9 ns at the driver and from 1 ns to 5 ns at the receiver, adding 4 ns to each number. Wally said the additional 4 ns is needed because the received data voltage levels are asymmetric due to the bias currents in the terminators.

Kevin Gingerich suggested that the receiver design could compensate for the offset voltages.

Bill Ham suggested that the setup time be increased by 2 ns to 7 ns transmit and 3 ns receive. He was concerned that increasing the budgets any higher would create problems with the Fast-80 budgets. Wally countered that the Fast-20 Differential budget had 4 ns of time for the external drivers that could be shifted to the transmit setup time. After a little more haggling, we ended up with agreement on adding 3.5 ns to get 8.5 ns transmit setup time and 4.5 ns receive setup time.

Fast-80 transmit setup and hold times were each changed to 5.75 ns and the Fast-80 receive setup and hold times were each changed to 1.75 ns. Bill suggested that, with these changes, still higher speeds beyond Fast-80 could not be achieved without protocol changes or going to a more tightly specified interconnect.

6. Releasing Bus from Active Negation [Uber]

Richard Uber bought up an issue regarding spurious glitches on LVDS lines caused when the driver goes from the active negation to the released states. The lines may appear to be true for up to a round-trip trip (approximately a BUS SETTLE DELAY). The major time of concern was the transition from MESSAGE IN phase to BUS FREE phase. Bill Ham asked the protocol chip vendors to look at their chips to see whether such glitches would have any adverse affects on their operation.

7. DIFFSENSE Specification [Uber]

Richard Uber presented a foil pointing out several deficiencies in the DIFFSENSE specification. The present document shows this information as a circuit example rather than as a performance specification. Having lobbed the grenade, Richard sat down and Bill Ham picked up foils and markers; he spent over an hour developing a new specification for DIFFSENSE (see SPI-2 Rev 4). These changes do not materially affect real designs underway but will improve the way the DIFFSENS is specified in the standard.

8. Voltage Mode Drivers [Bridgewater]

Wally Bridgewater presented the idea of using voltage-mode drivers with a separate 1 volt supply. The advantage is that the transistors would have a very low voltage drop (~0.1 volts) so the on-chip power dissipation would be quite low. The disadvantage is that external voltage regulators would be required.

There was some concern about how large of a common mode voltage range can be supported; Wally thought the transistors could operate somewhat outside the rails. Another concern was the effect of the low-impedance driver on the transmission line. Wally plans to do more investigation for the Dallas meeting.

It was generally agreed that the specifications for the drivers in the present draft depend too strongly on a current source method of implementation. By forcing a current source and a set of compliance voltages one boxes in a power dissipation in the chip. As there is nothing intrinsic about the use of current mode drivers with LVDS Kevin Gingrich and Bill Ham both called for removing the required use of current mode drivers. At the January meeting we will develop performance specifications that do not preclude the use of voltage mode drivers. This will open up new ways to manage the chip power dissipation and leave the implementation details to the suppliers.

9. Meeting Summary [Ham]

Generally, this meeting explored several second order facets of the low voltage differential transmission schemes. While there were some new points raised these were all of a tweaking nature. No show stoppers have been found yet.

At the request of the newly-formed SCSI Trade Association, a goal of acheiving technical stability by the March ‘96 meeting was set.

10. Meeting Schedule

The next meeting of SPI-2 Study Group will be Monday January 8, 1996, in Dallas, TX at the Doubletree Hotel at Park West (214-869-4300), hosted by Quantum Corp. Another SPI-2 Study Group meeting is scheduled for February 5, 1996 in Denver, CO hosted by Symbios Logic -- It appears that the February 5 meeting will be re-scheduled due to a conflict with an FC-0 meeting and the need for a two-day meeting to meeting the March '95 stability deadline. Tentatively, the meeting will be moved to January 29-30, 1996 still in Denver, CO.

11. Adjournment

The meeting was adjourned at 5:25 p.m. on Friday December 15, 1995.