To: X3T10 Membership X3T10/95-122r0

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Subject: Proposed 22 MByte/Sec ATA Timing Extension For ATA-3

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The following document contains modified sections from the ATA-2 Specification 948D Revision 2j Draft on ATA Timing Extensions. These sections have been enhanced to include the higher 22 MByte/Sec bandwidth modes.

## 1. New Timing Modes

In order to achieve higher data transfer rates new timing modes are defined: one for Multiword DMA data transfers and one for PIO data transfers.

## 2 New Multiword DMA Transfer Mode

New Multiword DMA Transfer Mode is defined and identified as Mode 3. The timing parameters associated with Multiword DMA Transfer Mode 3 are defined in Table 1. Peripherals reporting support for Multiword DMA Transfer Mode 3 must also support Multiword DMA Transfer Mode 0, Mode 1 and Mode 2. The timing parameters shown in Table 1 is directly related to the timing chart in the ATA-2 document 948D revision 2j Figure 12 on page 114

The minimum value of t0 is specified by the device in word 65 of the Identify Drive information. Refer to section 7.1.6 for a description of word 65.

**TABLE 1: New Multiword DMA Timing Parameters (Mode 2 and below are defined in ATA-2)**

| | Multiword DMA timing parameters | Mode 2 nsec | | Mode 3 nsec | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| t0 | Cycle time | 120 | | 90 | |
| tC | DMACK- to DMREQ delay | | --- | | --- |
| tD | DIOR-/DIOW- 16-bit | 70 | | 50 | |
| tE | DIOR- data access | | --- | | 30 |
| tF | DIOR- data hold | 5 | | 5 | |
| tF | DIOR- data hold | 20 | n/a | | n/a |
| tG | DIOW- data setup | 20 | | 20 | |
| tH | DIOW- data hold | 10 | | 10 | |
| tI | DMACK to DIOR-/DIOW- setup | 0 | | 0 | |
| tJ | DIOR-/DIOW- to DMACK hold | 5 | | 5 | |
| tKr | DIOR- negated pulse width | 25 | | 25 | |
| tKw | DIOW- negated pulse width | 25 | | 25 | |
| tLr | DIOR- to DMREQ delay | | 35 | | 30 |
| tLw | DIOW- to DMREQ delay | | 35 | | 30 |
| tZ | DMACK- to tristate | | 25 | | 25 |

## 3. New PIO Transfer Mode

New PIO Transfer Mode is defined and identified as Mode 5. The timing parameters associated with PIO Transfer Mode 5 are defined in Table 2. Peripherals reporting support for PIO Transfer Mode 5 must power up in a PIO Transfer Mode compatible with the existing ATA standard. The timing parameters shown in Table 2 is directly reflected in the timing chart in the ATA-2 document 948D revision 2j Figure 10 on page 110.

The minimum value of t0 is specified by the device in word 68 of the Identify Drive information. Refer to Identify Device Command section for a description of word 68.

**TABLE 2: New PIO Timing Parameters (Mode 4 and below are defined in ATA-2)**

| | PIO timing parameters | | Mode 4 nsec | Mode 5 nsec |
|---|---|---|---|---|
| t0 | Cycle time | (min) | 120 | 90 |
| t1 | Address valid to DIOR-/DIOW- setup | (min) | 25 | 20 |
| t2 | DIOR-/DIOW- 16-bit | (min) | 70 | 50 |
| | Pulse width 8-bit | (min) | 70 | 50 |
| t2i | DIOR-/DIOW- recovery time | (min) | 25 | 25 |
| t3 | DIOW- data setup | (min) | 20 | 20 |
| t4 | DIOW- data hold | (min) | 10 | 5 |
| t5 | DIOR- data setup | (min) | 20 | 20 |
| t6 | DIOR- data hold | (min) | 5 | 5 |
| t6Z | DIOR- data tristate | (max) | 30 | 30 |
| t7 | Addr valid to IOCS16- assertion | (max) | n/a | n/a |
| t8 | Addr valid to IOCS16- negation | (max) | n/a | n/a |
| t9 | DIOR-/DIOW- to address valid hold | (min) | 10 | 5 |
| tRd | Read Data Valid to IORDY active | (min) | 0 | 0 |
| | (if IORDY initially low after tA) | | | |
| tA | IORDY Setup time | | 35 | 30 |
| tB | IORDY Pulse Width | (max) | 1250 | 1250 |

## 4. Command and Parameter Changes

In order to achieve the desired improvement in data transfer rates, changes are made to the parameters associated with two existing commands: the Identify Drive command and the Set Feature command. Changes are made to follow the existing data structure in Identify Device and Set Feature commands with added timing and mode parameters.