Accredited Standards Committee^{*} X3, Information Processing Systems

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To: Membership of X3T10

From: Lamers/Milligan

Subject: Minutes of X3T10 ATA -3 Working Group #1 October 19, 1994

Agenda

1. Openning Remarks	2
2. Attendance and Membership, Introductions	
3. Approval of Agenda	2
4. Document Distribution	2
5. Old Business	3
5.1 ATA-3 Project Plan	3
5.2 ATA Suspended Issues List	3
5.3 ATA Command Queuing Proposals	4
5.4 ATA Multi-threading	4
5.5 Data prefetching across the ATA interface	5
5.6 Device 1 only on ATA	5
5.7 20 MB/s and greater ATA transfer rates	6
6. New Business	6
7. Call for Patents	6
8. Liaison Reports	6
9. Action Items	6
10. Meeting Schedule	
11. Adjournment	

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1. Openning Remarks

Gene Milligan convened the meeting at 9:30 am. He thanked Jim McGrath of Quantum for hosting the meeting. He also requested that Larry Lamers take the minutes and thanked him for accepting the request.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by X3T10 and would be conducted under the X3 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the X3T10 task group. The voting rules for the meeting are those of the parent committee, X3T10. For the ad hoc, other than straw votes, the voing rules are: one vote per participating company.

The minutes of this meeting will be posted to the X3T10 BBS and the ATA Reflector and will be included in the next X3T10 committee mailing.

2. Attendance and Membership, Introductions

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

The following people attended the meeting.

Name	_Company	Email Address
Hale Landis	Consultant	landis@sugs.tware.com
John Packer	Adaptec	packer@eng.adaptec.com
Lawrence J. Lamers	Adaptec	ljlamers@aol.com
Richard Kalish	Adaptec	rkalish@corp.adaptec.com
Kevin James	AMD	kevin.james@amd.com
Nicos Syrimis	Cirrus Logic	
Mark Gurkowski	Conner	mark.gurkowski@conner.com
Bill Willette	Dell Computer	bill_willette@us1.dell1.com
Dal Allan	ENDL	
Jeff Epstein	Future Domain	jeffe@fdc.mhs.compuserve.com
Dan Colegrove	IBM	colegrove@vnet.ibm.com
Pete McLean	Maxtor	pete_mclean@maxtor.com
Ron Roberts	Maxtor	rkroberts@aol.com
Tom Newman	Mission Peak Designs	71246.1573@compuserve.com
Robbie Shergill	National Semiconductor	rss@berlioz.nsc.com
Peter Brown	Oak Technology	peterb@corp.oaktech.com
Wang Mai	Oak Technology	
Chi-Chen Wu	Promise Technology	chiwu@promise.com
Ron Lin	Promise Technology	ronlin@promise.com
Farbod Falakfarsa	Quantum	-
James McGrath	Quantum	jmcgrath@qntm.com
John Brooks	Quantum	jbrooks@asic.qntm.com
Gene Milligan	Seagate	gene_milligan@notes.seagate.com
John Masiewicz	Seagate Technology	masiewicz@notes.seagate.com
Stephen Finch	Silicon Systems	5723283@mcimail.com
Devon Worrell	Western Digital	worrell@dt.wdc.com
Tom Hanan	Western Digital	t_hanan@dt.wdc.com

3. Approval of Agenda

Item 7 was changed to 'ATA-3 Command Goals & Requirements. The agenda was approved as amended.

4. Document Distribution

Conner ATA Tagged Command Queuing 10/18/94

Minutes of ATA Ad-hoc Working Group - Aug. 1994

Quantum ATA Command Queuing 10/13/94 James McGrath Western Digital Enhanced IDE Design Guidelines - Revision 1.0 - 10/18/94 - Hanan Suggested Multi-thread & Queing Process - Hanan

5. Old Business

5.1 ATA-3 Project Plan

Gene Milligan noted that ATA-3 is supposed to be delivered within 14 months. He requested an analysis of the work items be done so as to insure that we will meet that goal.

Tom Hanan presented a list of goals for ATA-3.

lower cost plug and play compatibility with existing systems highest performance at cost point for single disk work station internal peripherals Non-disk peripherals ATAPI CD-ROM & Tape PCI Bus Master DMA Command/device vs command/channel multi-thread Commands/device vs. command/device command queuing

Jim McGrath asked if ATA-3 could address issues above the interface, ala CAM for SCSI. Gene Milligan responded that there was ample precedence for such work as exemplified by the SCSI CAM projects and the FDDI Network layer (subsequently dropped due the availability of existing solutions for FDDI). However if the committee decides such work is desirable an additional project would be required and consideration for IEEE projects in related areas should be considered.

The term multi-thread was changed to overlapped commands. The multi-thread term generally refers to the software driver feature not a peripherial. Command queuing is yet another feature of a device.

There was considerable discussion over whether overlapped commands and command queuing are two separate issues or part of the same issue.

The ATA-3 Study Group agreed to recommend that key elements of the project plan should be: Proposal "cut off" January 1995 (later items slated for ATA-4) Preliminary description of proposed items by 11/10/94 Concensus on approach and acceptance of a working document by March 1995. Solidify the dpANS by July 1995. Final edit by September 1995. Initiate Letter Ballot for forwarding by November 1995.

5.2 ATA Suspended Issues List

The following list was supplied by Steve Finch:

a) Data reliability - CRC and Parity proposals - Adpatec, Cirrus, . All interested parties should update their proposals. (X3T10/94-027r2)

b) Major clean-up/re-write of the ATA document. - Deleted in view of the ATA-2 accomplishments.

c) Inclusion of ATAPI and CD-ROM support. - To be considered as items are developed by the ATAPI project activity with this item being principally liaison.

d) 20 MB/s transfer rates - tied in with termination issues. It was agreed that higer transfer rates should be DMA and not PIO.

Minutes of ATA Ad-hoc Working Group - Aug. 1994

Hale Landis suggested that the addition of a DMA mode IDENTIFY DRIVE command could eliminate the need for PIO mode commands for systems that wanted to implement just one set of command types. He urged that optimizing on DMA only hardware would simplify the drive and adapter silicon

- e) Reset Pulse Width (X3T10/94-053r2) need to resolve over the internet.
- f) Secure Mode (for removable devices) (X3T10/94-087r0) comments are requested.
- g) Format Issues. Resovled in ATA-2.
- h) Termintation issues tied in with item d).
- i) Check Power Mode additional capability (X3T10/94-154r0) comments if any are requested.
- j) Multi-threading. (Command overlap and command queuing) see further agenda items.

All prior proposals for ATA-3 that the proposer wishes to champion for inclusion in this project are requested to re-posted on the ATA reflector to insure that all participants have an opportunity to review nad comment on the latest version.

The study group recommended that all proposals for consideration ahead of ATA-4 need to be submitted by January 12, 1995.

The ATA-2 document will serve as the basis for the ATA-3 document.

5.3 ATA Command Queuing Proposals

See item 5.4.

5.4 ATA Multi-threading

Tom Hanan discussed the slides noted under document distribution. Is compatibility with with existing adapters required for overlapped commands? ... for queuing? Most of the group felt that a good solid performance solution should be the objective and if there are compatibility issues these are of secondary importance for queueing. Not requiring host intervention in DMA data transfers is a goal.

Key items:

interrupts during data transfers master/slave vs SCSI architecture register for command tag overlapped vs queuing support

List of topics to discuss:

overlapped commands arbitrated TF (DRQ, IRQ) command queuing interrupts during DMA data transfer register for command queueing master/slave vs peer architecture identify host hardware changes required electrical (buffer, cable, drivers) error reporting & management degree of CPU involvment effect of resets & aborts sharing interrupt line command by comand enabling of queing and arbitration atapi disk power mangement allow only simple que tags

Does the group want to proceed with an ATA command queueing and overlapped commands? 9 in favor, 6 opposed. Larry Lamers noted his negative was due to the fact that the ATA-3 project proposal does not specifically specify that ATA-3 will include command queuing.

Minutes of ATA Ad-hoc Working Group - Aug. 1994

Exception management in the queued environment. Jim McGrath expounded his view. Only simple queue tags should be allowed. Sending a command with the same tag value aborts both commands. Error reporting is the same as in ATA-2. Soft resets do not abort the queue. An error does not stop processing of the queue. Does the group favor using only simple queue tags? 13-0 Does the group favor having the queue cleared on error or reset? 13-0 Does the group favor having no provision to abort commands? 14-2 Does the group favor having a hardware reset put the device in non-queue mode? 12-1 (note - a software reset does not) Power mangement: Does the group favor fixing the sleep mode? 13-0 Does the group favor eliminating the sleep mode? 1-12 Queue tag register location: There are four ways to do this. a) redefine task file (e.g., error register) issues-problems with a command that completes in error and in multiple driver environments b) use non-disk register (e.g., 3f3) issues-may be in use by other folks c) use reserved hard disk bits issues-historical uses make this difficult to predict their use d) use word access method (e.g., use upper half of 3f6) issues-how does the drive know it is in word mode? also 16-bit access in PCMCIA may be a problem. Without opposition items b) and c) were dropped from consideration. Does the group favor redefining a task file for the queue tag (similar to Conner proposal)? 4-8-8 Does the group favor using word access for the queue tag? 9-4-8 Does the group favor not making a decision at this time? 13-2-3 Enabling queuing on a command by command basis. Should the mixed driver environment be addressed? If so, how should we do this?

Should all drivers know ATA-3? 8-4 Should a mix of drivers for ATA-2 and ATA-3 be allowed? 6-8

Does the group favor requiring ATA-3 accept queued and non-queued commands? 7-6-3

Does the group favor arbitration?

Are the devices autonomous relying on the host to resolve contention or is there a mechanism for the devices to resolve bus usage (i.e., arbitration)?

John Masciewicz suggested that each company that wants to make a proposal for queuing develop one and bring it back to the next meeting and be allowed one-hour to present that proposal and its merits. There was general agreement to follow this path.

Steve suggested that the slave drive use PDIAG for interrupt. This works if a bridge chip handles the interrupts. Can a bridge chip handle a two signal interrupt? Defining this as a functional requirement has compatibility issues.

Agree that if it is host based that it must be simple enough for a bridge to do it.

5.5 Data prefetching across the ATA interface

Prefetching can be a problem with ATAPI devices because they are not a fixed length transfers. Handle in ATAPI.

5.6 Device 1 only on ATA

Desired by ATAPI to allow only one device as device 1 so that timeout need not be waited for and for applications where it is desired to keep the ATAPI and Disk Device on a separate bus. Should the registers be shadowed for the non-existent devices? This will be looked at in the ATA-2 working group as part of Hale Landis's comments.

5.7 20 MB/s and greater ATA transfer rates

DMA only was agreed to.

6. New Business

None.

7. Call for Patents

Gene Milligan requested that anyone aware of andy patents required fort the proposals be disclosed early in accordance with the ANSI patent policy.

The Secure Mode proposal involves patents pointed out by Pete McLean and he stated that a letter has been submitted by Maxtor. He also mentioned an IBM patent and Dan Colgrove agreed to pursue that possibility.

8. Liaison Reports

8.1 ATA-2

Review of the document is continueing. A two day working group meeting is set for Thursday and Friday. The target is to attempt a forwarding at the January X3T10 plenary.

8.2 ATAPI

Tom Hanan reported that an ATAPI meeting is planned for 11/29/94 to deal with command queuing and SFF-8020 issues. Tom plans to not submit ATAPI to X3T10 until the project proposal is approved.

9. Action Items

1) Gene Milligan to investigate the appropriateness of command queuing in the ATA-3 project proposal.

2) Larry lamers to get document numbers for later inclusion in next minutes.

3) All participants are requested to post existing proposals for ATA-3 on the ATA reflector.

4) All partcipants to submit ATA-3 proposals for consideration in preliminary concept form by 11/10 and final form by January 12, 1995.

10. Meeting Schedule

November 10, 1994 at Palm Springs, CA. Host: Western Digital. November 30, 1994 at Irvine, CA. Host: Western Digital.

11. Adjournment

The meeting adjourned at 5:00 PM on October 19, 1994.