Accredited Standards Committee*
X3, Information Processing Systems

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Date: Sept. 8, 1994
Project:
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Reply to: S. Finch

To: Membership of X3T10

From: Shergill/Finch

Subject: Minutes of X3T10 ATA Ad-hoc Working Group #9 Aug 31-Sep 1, 1994

Agenda

1. Opening Remarks
2. Attendance and Membership, Introductions
3. Approval of Agenda
4. Document Distribution
5. Old Business
    - 5.1 Termination Issues (Hanan)
    - 5.2 ATA-2 Technical Review
6. New Business
    - 6.1 Multi-threading (Hanan)
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8. Adjournment

Results of Meeting

1. Opening Remarks

Steve Finch convened the meeting at 9:00 am. Steve thanked Ray Heineman of Maxtor for hosting the meeting.

As is customary, the people attending introduced themselves. A copy of the attendance list was circulated for attendance and corrections.

It was stated that the meeting had been authorized by X3T10 and would be conducted under the X3 rules. Ad hoc meetings take no final actions, but prepare recommendations for approval by the X3T10 task group. The voting rules for the meeting are those of the parent committee, X3T10. These rules are: one vote per company; and any participating company member may vote.

The minutes of this meeting will be posted to the X3T10 BBS and the ATA Reflector and will be included in the next X3T10 committee mailing.

2. Attendance and Membership, Introductions

Attendance at working group meetings does not count toward minimum attendance requirements for X3T10 membership. Working group meetings are open to any person or company to attend and to express their opinion on the subjects being discussed.

The following people attended the meeting.

Name	Company	Email Address
Norm Harris	Adaptec	
Richard Kalish	Adaptec	rkalish@aol.com
Lawrence J. Lamers	Adaptec	ljlamers@aol.com
Joseph Chen	Cirrus Logic	chen@cirrus.com
Nicos Syrimis	Cirrus Logic	
Lane Lee	Conner Peripherals	
Jeff Epstein	Future Domain	
Mark Raymond	Future Domain	
Dan Colegrove	IBM	colegrove@vnet.ibm.com
Tony Pione	IBM	
Ray Heineman	Maxtor	ray_heineman@maxtor.com
Ron Roberts	Maxtor	
Tom Newman	Mission Peak Designs	
Robert Griffith	National Semiconductor	
Robbie Shergill	National Semiconductor	rss@berlioz.nsc.com
Curt Allred	Nexcom Tech.	
Karl Schuh	Nexcom Tech.	
Peter Brown	Oak Technology	
Phil Verinski	Oak Technology	
Charles Yang	Panasonic	
Mike Carpenter	Qlogic	M.carpenter@qlc.com
Farbod Falakfarsa	Quantum	
James McGrath	Quantum	
Don Powlison	Quantum	
John Masiewicz	Seagate Technology	masiewicz@notes.seagate.com
Hale Landis		
Stephen Finch	Silicon Systems	5723283@mcimail.com
Yas Hashimoto	Toshiba America	
Devon Worrell	Western Digital	
Tom Hanan	Western Digital	t_hanan@dt.wdc.com

(Note: Not all attendees were present for both days).

3. Approval of Agenda

Item 5.1 was struck because Hanan did not put his proposal on the Reflector at least two weeks prior to this meeting as was agreed to at the last meeting. Tom was asked by Steve to bring this in as an ATA-3 item.

Item 6.1 was added for the second day, if time permits.

The agenda was approved as amended.

4. Document Distribution

ATA-2 Working Draft, Rev 2f - Finch, SSI.
Re: Items for ATA agenda - McGrath, Quantum.
Re: WD Command Queuing Proposal - McGrath, Quantum.
Hale Landis's Comments - Landis.

5. Old Business

5.1 Item removed from agenda.

5.2 ATA-2 Technical Review:

The working draft revision 2f was reviewed in a section-by-section manner. Rest of this section is intended to be a complete list of changes agreed upon. Please refer to the Working Draft revision 2g for a complete and accurate description of the changes.

Revision Page will be deleted when the document is finalized (was a comment by Gene Milligan)

Throughout the document, Steve will explicitly say "bit xxx" instead of "xxx".

Throughout the document, Steve will change 'x' to 'r' for all reserved bits.

Section 3:
Added glossary item - Command acceptance: a command is considered accepted whenever the host writes to the cmd reg. and the device currently selected has its BSY bit set to 0. An exception exists for the execute diagnostics cmd. (see description of execute diag cmd).

Added glossary Item - Drive Selection: a drive is selected when the DEV bit in the Drive/Head register is equal to the device number assigned to the device by means of a dev0/dev1 jumper or switch or use of the CSEL signal.
(moved here from section 6.1.1)

Section 3.2.5
Tom Newman said that the byte ordering appears reversed - others didn't agree.
Tom Hanan wanted a note added - this is not the order in the PC. All agreed, Hanan wrote the note and it was added. Tom Newman was asked to check the actual byte ordering on a disk drive.
On Day-2: Tom Newman reported back. His results showed that the byte ordering is reverse of what the document currently contains. Confusion was due to the difference in byte-ordering between the actual data transfers at the interface and the way Identify Data is represented. Agreed to change this section to address only the byte ordering for 8 and 16-bit data transfers - not the byte-ordering related to fields in Identify Device data. Also worked out an advisory note saying that some systems will swap bytes.
Voted on the note's inclusion: For: 13, Against: 4. The note was accepted.

Changed "n from 2 to 512" to "n starting at 2"

Paragraph 2: changed "will" to "shall" and also stressed "on the interface" again.

Sections 4.2 and 4.3
Editor will soften the language to say that the connector shown here is one example of several connectors. Agreed that we will completely define the connection schemes in ATA-3.

Section 4.5
Table 3, second line, description, changed "Rise" to "Fall".

Section 5.2.4 DASP-
Third paragraph, second sentence: deleted.

Added back the language from rev 2d concerning the requirement for the host to current limit on the LED load. (John Masiewicz comment).

Sections 5.2.6 and 5.2.7
Added after the last sentence "The device shall not act on the data until after it is latched". (Tony Pione and Devon Worrell had pointed out this problem).

5.2.10 INTRQ
Joe Chen wanted to add back the option of clearing INTRQ automatically at the end of the data block transfer - except for the last block transfer. Hale didn't like this option because it means that interlocking is lost. Tom Newman pointed out that there are other ways to interlock. Jim mcGrath pointed out that the hardware implementation of today require a dead-time to be inserted in order to ensure interlock. The group voted on the concept behind Joe's proposal - 3 in favor, 14 against. Joe was asked to bring this issue to the plenary meeting if he wants to pursue this further.

5.2.11 IOCS16-
Fourth bullet point:
Jim McGrath: should it be "not valid" or "not asserted"? He wanted it to be "not asserted".
Others disagreed. The group agreed unanimously to change "is not valid" to "shall not be used by the host".
Another isssue raised was whether an editor's note should be added stating that IOCS16's switching at mode 3 or higher speeds is not recommended. Vote - 5 for, 6 against. Not accepted.

5.2.15 second para, last sentence: changed "made by...." to "vendor specific".

5.2.15.2 CSEL
Tom Hanan brought up the issue that some people want to use CSEL to select the devices electronically - so we should specify that the csel should be used only at the time of reset.
Added the sentence: "host shall maintain CSEL at a stable level for at least 31 seconds after the deassertion of Reset-". Also changed the terms "grounded" and "open" to "negated" and "asserted" in the two bullets.

6.1 changed the title to Device Addressing Considerations and combined with subsection 6.1.1.

Paragraph 3, first sentence: deleted everything after Device/Head Register (see clause 6.2.8) because the other methods are configuration, not selection.
Robbie Shergill asked that the last sentence of para 3 should be deleted because it is not consistant with figure 1. This opened up the issue of whether a single drive can exist as drive 1. Tom Hanan claimed that some people are implementing systems with a slave drive only. Steve Finch asserted that this cannot be done without violating the spec. This issue was not resolved and the sentence in question was left intact.

Fourth paragraph was moved to glossary.

6.2 table 7: Issue was raised whether "not used" be changed to "reserved"? After a lengthy discussion the group decided not to do so. The Device Address register entry was replaced with a note saying that only bit 7 has to be kept high impedance and the rest of the bits are obseleted.

6.2.3/6.2.4/6.2.8/6.2.12
mcgrath asked that Cyl/Head/Sector Number updating requirement be removed because the auto-increment circuitry is costly and the updating serves no real purpose. Hale and Hanan agreed with this. Changed the wording to state that the updating is only required for media access cmds that end in an error. Added an editor's note stating that all commands ended with the CSH updated prior to this spec, but this spec doesn't require that.

6.2.5 Data Register
Changed wording as suggested by Hale in his document.

6.2.6 Device Control Register
Made bits 7-3 reserved. Voted on making bit 3 reserved: 12 in favor, 1 opposed.

6.2.7 Device Address Register

Eliminated this section. Added a note to table 7 instead.

6.2.8 Device/Head Register
Removed second sentence.
Made bits 7 and 5 reserved.
Removed the "binary encoded" term.
Changed the name of the L bit to sector address mode select
Changed the name of the DEV bit to device address

6.2.9 Error register
BBK bit: Ray Heineman wanted to eliminate this bit because Format Track has been made vendor specific and it is the only command that uses this bit.
Hale wanted to retain it because he may need to use it for commands other than format track.
Voted: make it reserved? For: 10, opposed: 4.

MC and MCR bits: Hale wanted to remove the description only and say that these are for removable media and the implementation is vendor-specific. Joe Chen disagreed - these bits have been in ATA-1 and some people are using them.
Voted - in favor of Hale's alternate wording: 12, against:1.

6.2.11 Sector Count register
Accepted Hale's alternate description which says essentially that just because SCNT=0 doesn't mean that the command completed successfully.

Deleted the reference to Format Track cmd.

6.2.12 Sector Number register
Accepted Hale's alternate description.

6.2.13 Status register
Joe Chen proposed making bits 2, 4 and 5 vendor-specific.
CORR bit: McGrath wanted to make it "reserved" altogether. Colegrove wanted to retain it because his users monitor this bit to keep track of media degradation. Shergill asserted that it is the definition of "correcatble error" that varies from vendor to vendor so just make this vendor specific. This was agreed to.

DWF bit: Hale doesn't mind making this vendor specific, but wants to retain the portion that this bit should stay set 'till the status is read. Voted to accept Hale's wording. 13 for, 3 against.

DSC bit: Agreed to accept Hale's recommendation and make it equal to DRDY bit because BIOSes generally look for this state in the Status register. McGrath asked for, and all agreed, that a note should be added that in ATA-3 this bit will be reclaimed.
Additionally, this bit's name was changed to Bit4.

Next, Hale's introductory statements for this register were amended and accepted.

Gene Milligan had commented that the clearing of error bits is not clearly defined and this causes the hosts to never know what to believe. Hanan agreed and suggested that the ERR bit and the Error register should be required to hold their state until the next command. All agreed on the following language:

"Once this bit is set, the device shall not clear this bit or change the contents of the command block registers, except the data reg and the vendor specific bits in the Status register, until a new command is accepted by the device, the SRST bit is set to one, or RESET- is asserted."

Another of Gene's comments was also accepted - it should be noted that the BSY=1 state can be very short so the host sw should not rely on detecting this state.

The group next considered Hale's proposals pertaining to the Status register. Hale recommends that DRQ, ERR and CORR bits be changed only while BSY=1. chen suggested that just BSY and DRQ's relationship should be covered here and ERR and CORR bits should not be covered. Finch asserted that the better way to specify this is that there are only certain registers or bits that the device can change while BSY=0. These bits are: DRDY, DWF, bit 4, CORR, IDX in the status register and the Data register. This change was accepted.

A lengthy discussion took place on the issue of BSY's state during data transfers. In the end, the group agreed to Hale's five conditions for when BSY must be set but changed the language. Sum total of it all is that from 400ns max after command acceptance and until command completion, if DRQ is not set then BSY must be. The list has been made a set of requiremnts for the events when the device must set BSY. Robbie Shergill raised the point that the device should also not be allowed to set BSY at any other times - which was the original intention of this list in ATA-1. This was agreed to and Steve will add a sentence at the end.

DRDY bit: accepted Hale's re-wording with few changes: deleted the requirement that it stays stable 'till status is read. A discussion took place concerning whether DRDY=1 means that the device is ready to ACCEPT a command - given our new definition of command acceptance. This issue was not resolved.

ERR bit: Dan Colegrove rewrote the paragraph in response to Gene's comment of this morning. It specified the list of bits and regs that must not change once ERR bit is set and until the next command.

6. New Business

No new business items were addressed as the technical review was not completed within the allocated time.

7. Meeting Schedule

9/15: Houston, TX. Host: Compaq.
9/27-28: Milpitas, CA. Host: Quantum (was previously scheduled to be held at Longmont).
11/10: Palm Springs, CA. Host: Western Digital

8. Adjournment

The meeting adjourned at approximately 4:00 PM on Sept 1, 1994.