Doc No: X3T10/94-055r0

Subj: ATA Extensions SSWG Minutes - Feb 94
Date: March 11, 1994

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Minutes of the ATA-Extensions Special Working Group Meeting
Held February 23, 1994, in Milpitas, CA, at Crown Sterling Suites Hotel.

Chaired by: Steve Finch, SSI.
Hosted by: Jim McGrath, Quantum Corp.
Minutes recorded by: Robbie Shergill, National Semiconductor.

Following documents were distributed in this meeting:

- 94-052r0: Proposed change of Mode 4 T0... (T. Hanan, WD)
- 94-051r0: Comments on ATA-2 rev 2 (J. Masiewicz, Seagate)
- 94-047r0: Minutes of the January SSWG meeting (R. Shergill, National)
- 94-027r1: Data CRC (R. Kalish, Adaptec)
- _____: Low Power Modes (T. Hanan, WD)

1. Steve Finch opened the meeting at 9:30AM by thanking the host and stating the purpose of the meeting and some pertinent ANSI mechanisms. He asked each attendee to introduce themselves and also sign the attendees list.

2. Agenda for this meeting was circulated by Steve Finch. It was modified and accepted.

1. Opening remarks, introductions and welcome

2. Approval of agenda

3. Attendance and membership

4. Time and place of next meeting

5. Old Business
    5.1 16.6 MB/s
    5.2 Data CRC

6. New Business
    6.1 Seagate Comments and Driver Specs (Masiewicz)
    6.2 Rise/fall times
    6.3 Issues from ATA-2 editors meeting
    6.4 Minimum reset pulse width
    6.5 DRQ deassertion after the last byte is transfered
    6.6 Miscellaneous

7. Adjournment

3. Attendance List

NAME	COMPANY	PHONE

Al Pham	Adaptec	408-945-2560
Richard Kalish	Adaptec	408-957-7169
John Geldman	Cirrus Logic	510-226-2101
Dave Weber	Cirrus Logic	510-226-2367
Mark Gurkowski	Conner Peripherals	303-682-8317
Dan Colegrove	IBM	507-289-0922
Larry Lamers	Adaptec	408-945-8600
Robbie Shergill	National Semi.	408-721-7959
Charles Yang	Panasonic	408-262-2200
Jim McGrath	Quantum	408-894-4504
Jim Wilshire	Quantum	408-894-5245
Mike Carpenter	Q-Logic	714-668-5366
Hank Davenport	Samsung	408-434-5427
John Masiewicz	Seagate	408-439-2152
Steve Finch	Silicon Systems	714-573-6808
Tom Hanan	Western Digital	714-832-7472

4. Time and Place for the Next Meeting:

Mar 14: Newport Beach (as part of X3T9.10, 2-8 PM)
Mar 30: TBD (possibly Western Digital, Irvine)

(Next Editors' Meeting is on March 13 at Newport Beach).

5. Old Business

5.1 16.6 MB/s:
Tom Hanan presented revised Mode 4/Mode 2 timings that are contained in his document. The group reviewed the proposed timing values. Although Tom is pointing out the system design difficulty with 25ns recovery time, he is not recommending that this time should be reduced to 20ns.
The group decided to change t4 back to 10ns so that it would be the same in PIO and DMA modes.

The note concerning IOCS16- was debated. John Geldman's suggestion of removing the note and putting in a recommendation was agreed to.

John Masiewicz suggested that DIOR- setup time be reduced by 5ns. This was not agreed to.

John Geldman suggested that IOCS16- "negation" should be changed to "release". Agreed.

Mark Gurkowski asked again that Note 4 of the table make it clear that the minimum t0 time supported is returned in the ID data. This was agreed to.

Robbie Shergill raised the point that t0 now doesn't apply to assert edge-to-assert edge cycle. After a brief discussion it was decided that this is true and it is allowed.

It was decided that the DMA diagram will be changed back to show that data lines can be kept enabled during burst transfers.

John Geldman pointed out that the "xx"s on read data have been dropped - these should begin when DIOR- is asserted. Tom Hanan wanted the "xx"s to start from DMACK- assertion. Significant discussion took place, a vote was taken and Tom's proposal was denied.

Dan Colegrove asked if a drive is required to set mode 3 bit also if mode 4

bit is set. It was clarified that you don't have to; you only have to always meet mode 0. However, the low-level timings guarantee that if you can make mode 4, you can make mode3 also.

5.2 DATA CRC:
Since Richard Kalish was not at the last meeting, he wanted to revisit this issue. It was clarified that at the last meeting it was decided that this issue should be debated on the reflector under the broader heading of data integrity. If necessary, a separate SSWG can be started on this topic. No further discussion took place.

6. NEW BUSINESS:

6.1 SEAGATE COMMENTS ON ATA-2:

John Masiewicz went over his document and each item was discussed in order.

The issue of 3v and 5v drive power was discussed. John Masiewicz just doesn't want to endorse the plugging of 3v drives into 5v systems.

Steve Finch proposed that we eliminate support the 3v option from the power connector. After further discussion, a vote was taken on this proposal and it passed unanimously. Steve will take this recomendation to X3T10 next month.

Tom Hanan propsed that since we don't adequately address 3v operation, we should take out all references to 3v operation. This was also agreed to unanimously.

John Masiewicz feels that his proposed electrical specs have been put into ATA-2 in such a way that the true intent is lost - thus the new proposal. John wanted to know if we want to include the ATA-1 info in ATA-2 spec? Tom answered yes, because ATA-2 replaces ATA-1.

Jim McGrath brought up the issue of mixing ATA-2 and ATA-1 drives/systems. Tom felt that we have to have a way to alter the driver characteristics based on the mode we're running in. McGrath said that this would be difficult because most systems don't even want to do a Set Features.

Robbie Shergill said that it sounds like we need to do mode selection in hardware - such as using the IOCS16- (grounded means ATA-2) for this purpose. Tom Hanan agreed with the desirability of hardware selection, but not at the cost of an interface signal.

As far as electrical specifications are concerned, John Masiewicz asserted that his proposal of using thevenin equivalent loads covers both ATA-1 and ATA-2 for all signals except IOCS16-. He will look at this issue more and revise the load circuit if needed.

Based on Masiewicz's comments, a number of other corrections were also agreed to. John will revise his document and Steve Finch will edit the ATA-2 document appropriately.

Al Pham (Adaptec) suggested that INTRQ signal's enabling/disabling times should be specified. Concern is that the signal may drift up to a logical-high level when one drive is deselected and another is selected. The group agreed that something like 50ns max time should be spec'd from drive selection to INTRQ enabled. Tom Hanan will write a proposal.

6.2 RISE AND FALL TIMES:

The issue of rise and fall time specification was debated extensively. Jim Wilshire (Quantum) wanted to change to 10 and 90 percent points, but John Masiewicz said that there is difficulty with this method in determining what the full amplitude should be. Tom Hanan and Jim Wilshire said that their driver design slews at different rates during different portions of the transition; but Mark Gurkowski asserted that a spec shouldn't tell people how to implement. Finally, there was some agreement that perhaps specifying dv/dt for a given load is the best way to go.

No final resolution was reached. It was agreed that we all will bring our specific preference to the next meeting in Newport Beach.

6.3 ISSUES FROM EDITORS' MEETING:

Steve Finch asked if we should drop the alternate connector descriptions from the annexes?
Tom Hanan wants to either do a complete job or drop it altogether.
Steve will leave them in for now. Further discussion defered to the editors' meeting.

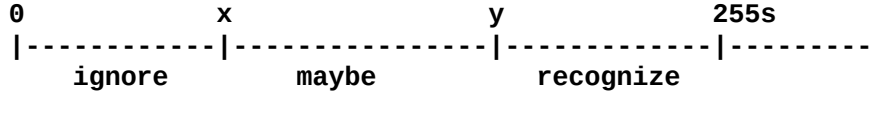
6.4 RESET MIN TIME:

Adaptec raised this issue again: at what point does a reset pulse become narrow enough to be called a glitch and, therefore, is ignored?

John Masiewicz doesn't want a new spec that will obselete existing hardware. He also believes that the safest thing for the system is that the drive goes ahead and resets anytime it sees a reset pulse of any duration. Tom Hanan doesn't agree with this philosophy.

Steve Finch stated that as it stands today, under 255s the drive's behavior is undefined as per ATA spec. The drive spec may say that below n ns it will definitely ignore, but the ATA spec doesn't have to address it.

Jim McGrath said that in reality a few nano-seconds wide pulse has to be filtered. It was decided that we should take this discussion to the Reflector. Everyone should give their input on x and y as defined below and as their silicon does it today:



6.5 DRQ CLEARING AFTER LAST TRANSFER:

Tom Hanan reported that one of his customers, who is a system manufacturer, is saying that they have a fast BIOS that is having a problem where, on more than one drive, they see that just after the last data word transfer the DRQ bit is still set and the BUSY bit is still not set. The BIOS then thinks that the drive wants to transfer the next sector and it just proceeds with that. Tom's customer is not blaming the drive for doing this, but in order to avoid this he wants the ATA-2 spec to add a required minimum time delay between the data phase and the status phase that the BIOS wil have to observe. They recommended 55s, but the group thinks that 55s is too long. All agreed to put a limit of 1 5s. Tom will write a proposal.

6.6 MISCELLANEOUS:
Steve Finch informed everyone that the ATA-3 project proposals will be voted upon in the March Plenary. So, make sure your rep is ready to vote.

John Masiewicz asked if we can safely say now that 16MB/s mode will be included in ATA-2. Steve Finch said that he intends to show 16MB/s to the Plenary this March and then give them two months so in May they can vote on it.

7. The meeting was adjourned at 3:00 PM.

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