Minutes of SAS PHY Working Group conference call February 1, 2007 T10/07-062r0

Attendance:

Mr. Bernhard Laschinsky	Agere Systems
Mr. Kevin Marks	Dell, Inc.
Mr. Mickey Felton	EMC
Mr. Ramez Rizk	Emulex
Mr. Douglas Wagner	FCI
Mr. Mike Fitzpatrick	Fujitsu
Mr. Rob Elliott	Hewlett Packard Co.
Mr. Dan Colegrove	HGST
Mr. George O. Penokie	IBM Corp.
Mr. Harvey Newman	Infineon Technologies
Mr. Schelto van Doorn	Intel Corp.
Dr. Mark Seidel	Intel Corp.
Mr. Pankaj Kumar	Intel Corp.
Mr. Michael Jenkins	LSI Logic Corp.
Mr. Gabriel Romero	LSI Logic Corp.
Mr. Paul Wassenberg	Marvell Semiconductor, Inc.
Mr. Galen Fromm	Molex Inc.
Mr. Hock Seow	NEC Electronics America, Inc.
Mr. Tim Symons	PMC-Sierra
Mr. Rick Hernandez	PMC-Sierra
Mr. Alvin Cox	Seagate Technology
Mr. Benoit Mercier	STMicroelectonics
Mr. Stephen Finch	STMicroelectronics
Mr. Adrian Robinson	Vitesse Semiconductor
Mr. Kevin Witt	Vitesse Semiconductor
Mr. Mahbubul Bari	Vitesse Semiconductor
Mr. Larry McMillan	WDC

27 in attendance

Agenda:

1.) 10/07-058r0 SAS-2 OOB and SSC [Finch]
http://www.t10.org/ftp/t10/document.07/07-058r1.pdf

Steve to update per discussion, change 2300 to 2400, and add line in table73 for if SSC is supported along with appropriate wording. These changes are included in the r1 link above.

Seagate complained that they thought they had an issue with the timing change. Alvin indicated that the response he was working from was somewhat confusing and that he would verify and post a position to the reflector. Since the call, Alvin has clarified that the issue is not with the OOB area (just SNW1 and SNW2 if SSC is applied), so the objection is now removed. A memo concerning this has been sent to the reflector.

2.) New items.
Rob indicated a need to propose wording for attenuation of jitter paragraph. Alvin indicated that this is required for measurement of jitter if SSC is applied to the signal and does not affect SAS 1.1. Seagate plans to propose a description based on lab measurements they have made.

3.) Review of PHY specification proposal.
Alvin will post the initial proposal the afternoon of 2/2.
http://www.t10.org/ftp/t10/document.07/07-063r0.pdf

It is very preliminary and nowhere near complete, but rather a basis to leverage the final PHY proposal from rather than a PowerPoint format.

Discussion items:

Rob doesn't like "transmitter device" and "receiver device" because "device" has so many meanings. I have left them in place until a viable alternative is proposed.

Use "transmitter device equalization" instead of "de-emphasis".

Transmitter equalization needs to be informative rather than normative because of emphasis schemes and desire by large OEM's to have custom settings. A default transmitter equalization value of 3 dB is currently the recommended value. In some extraordinary cases, additional equalization is beneficial. The discussion regarding what value of transmitter equalization for the reference transmitter device resulted in no consensus. On one side, a low value gives the worst case simulation for high-loss channels while a high value give the worst case for short channels.

1. Is it that hard to run both simulations?
2. Since the channel characteristics are known via s-parameter measurements, if both extremes are not used in simulations, can't an engineering judgment be made to

Discussed the method of measuring transmitter equalization. The diagnostic 2 DWORD test pattern of D30.3 (Table 215 in SAS 2 rev 8) [4/3/3/4] or possibly CJTPAT could be used. CJTPAT is available from all PHY's so it has this advantage. Text and figures will be updated based on the pattern chosen, amount of equalization, and final methodology. Comments encouraged.

Jitter:
All indications are that the present measurement method using a type 1 filter with a corner frequency of fbaud/1667 will not allow measurement with SSC. Probably needs a type 2 filter, but details need to be determined. Seagate will provide an initial description.

There are some factors at the far end that will complicate the receiver jitter tolerance specification. Since the receiver is expected to have an equalization function, a mathematical equalization equation will probably be needed to process the received signal at the compliance point to determine the resulting jitter is proper for testing the receiver device.

General:
Values need some amount of description for measurement methodology similar to what was done in SATA.

Next call February 9, 2007

Agenda:
1.) 10/07-058r1 SAS-2 OOB and SSC [Finch]
http://www.t10.org/ftp/t10/document.07/07-058r1.pdf

2.) New items.

3.) Continue discussion of PHY specification proposal.
http://www.t10.org/ftp/t10/document.07/07-063r0.pdf

Weekly teleconferences scheduled for Thursdays at 10 am CST:

PARTICIPANT INFORMATION:

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Webex information:
https://seagate.webex.com/seagate

Topic: SAS-2 PHY WG
Date: Thursday
Time: 10:00 am, Central Standard Time
Meeting number: 826 515 680
Meeting password: 6gbpsSAS

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