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06-496r2 SAS-2 Electrical Specification Proposal

Serial Attached SCSI

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SAS-2 Phy Working Group

11/7/06

YOUR PARTNER FOR SUCCESS

Overview

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- Motivation
  - Multiple SAS-2 Test Chips Have Been Built and Tested, SAS-2 Product Designs are Starting, To Date We Do Not Have a Electrical Specification or Outline of One.
- Propose Initial Transmitter and Receiver Electrical Specifications
  - Definitions & Compliance Points
  - Reference Devices
  - Transmitter Device Signaling
  - Receiver Device Signaling
  - Channel Compliance
  - Open Issues

References

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References:

- 06-419R1 SAS-2 Reference Transmitter and Receiver Specification Proposal
- 06-206R2 SAS-2 Data Eyes vs. De-Emphasis
- 06-053R0 Roadmap to SAS-2 Physical Layer Specification
- 06-052R0 Enhanced SFF-8470, SFF-8086 and SATA Cable at 6Gbps
- 05-204R1 Towards a SAS-2 Physical Layer Specification
- 05-426R0 SAS-2 Cable Reach Objective and Crosstalk
- 05-425R1 SAS-2 Channel Model Simulations
- 05-342R0 SAS-2 Adaptive Equalizer Physical Layer Feasibility
- 05-341R1 Updated Test and Simulation Results in Support of SAS-2
- 05-203R0 SAS-2 6Gbps Test Results

Compliance Points and Devices Should be Consistent with SAS-1

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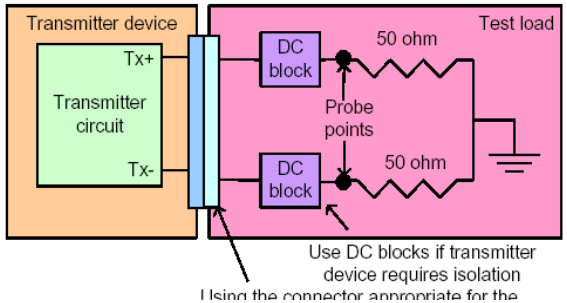
- Compliance Points (SAS1.0 see Section 5)
- Tx Device
- Rx Device
- Zero Length Tx Test Load

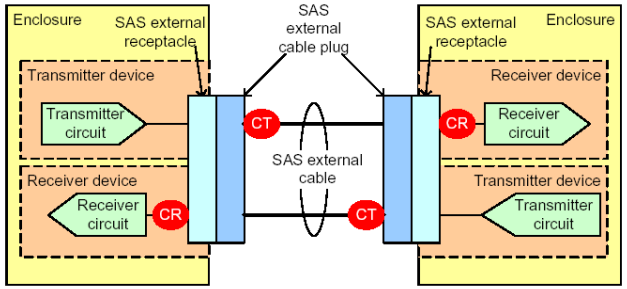
Table 33 — Compliance points

Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device (see 3.1.245), as measured at probe points in a test load attached with an internal connector (e.g., with a SAS plug (see 5.2.3.2.1), SAS internal cable receptacle (see 5.2.3.2.2), SAS internal cable SATA-style signal cable receptacle (see ATA/ATAPI-7 V3), SAS backplane receptacle (see 5.2.3.2.3), SAS internal wide cable receptacle (see 5.2.3.4.2), SAS internal wide plug (see 5.2.3.4.3), SAS internal compact wide cable plug (see 5.2.3.4.5), or SAS internal compact wide receptacle (see 5.2.3.4.6))
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device (see 3.1.152), as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector (e.g., with a SAS external cable plug (see 5.2.3.3.2), a SAS external receptacle (see 5.2.3.3.3), a SAS external compact cable plug (see 5.2.3.3.5), or a SAS external compact receptacle (see 5.2.3.3.6)).
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.

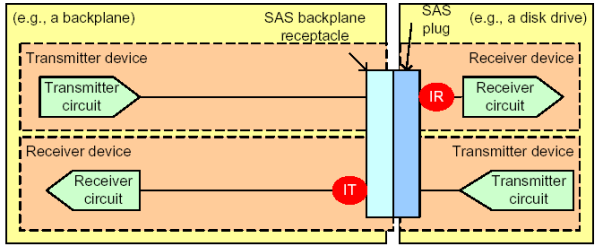


Examples

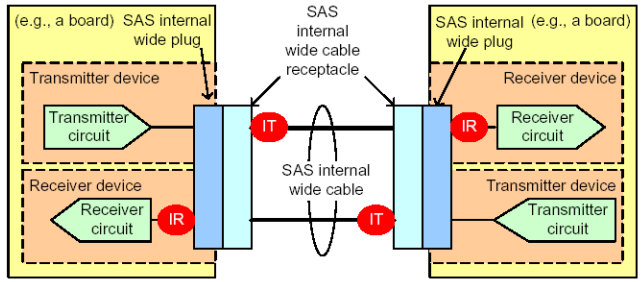
External receptacle/external cable plug



Backplane receptacle/SAS plug



Internal wide cable receptacle/internal wide cable plug



Recommendation Made for Test Load to Test Equipment Insertion Loss Spec. (Update to be added)

Reference Devices

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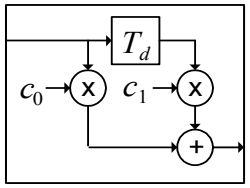
- The Tx and Rx Reference Devices (see T10-419r1)
  - Used for Link Simulation and Channel Compliance
  - Not a Design Guideline, actual Designs must exceed the Performance of these Reference Devices

Reference Transmitter

Reference Transmitter		Units
Ref Tx # Taps De-Emphasis	2	Taps
Ref Tx De-Emphasis	-6	dB
Ref Tx De-Emphasis Tap Spacing	1	UI

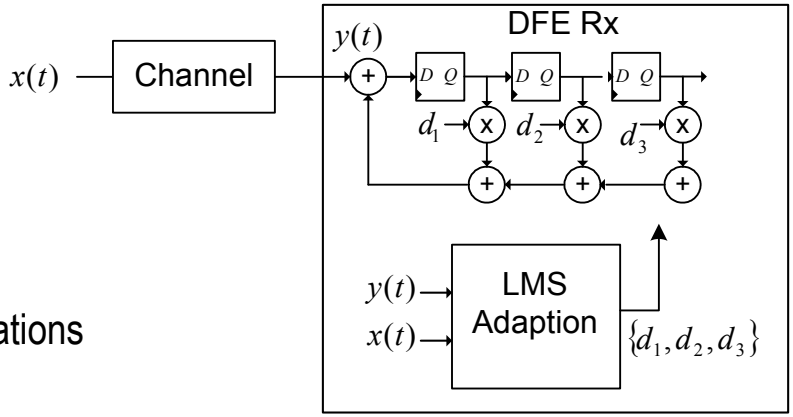


$$DE_{dB} = 20Log_{10}\left(\frac{c_0 + c_1}{c_0 - c_1}\right)$$

$$c_0 = 0.7488 \quad c_1 = -0.2488$$

- Reference Receiver

Receiver		Units
Reference Rx # DFE Taps	3	taps
DFE Tap Spacing	1	UI
Coefficient Adaptation Agorithm	LMS*	



* See Lee and Messerschmitt, Digital Communications

SAS-2 Transmitter Device Proposed Numbers

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Transmitter Device Signal Characteristics

- Measured into a Zero Length Test Load (CT and IT)
- Through a Mated Connector

	SAS-2			
Transmitter	Min	Nominal	Max	Units
Bit Rate		6000		MBps
Differential Voltage (pk-pk) Vpk	800		1200	mV
Transition Time (20%-80%)	0.25 / 41.667		0.45 / 75	UI /ps
Tx De-Emphasis	-5		-7	dB
DC Differential Impedance	60	100	115	ohm
DC Impedance Mismatch			5	ohm
DC Common Mode Impedance	15	25	40	ohm
Differential Return Loss			see Plot	dB
Common Mode Return Loss			see Plot	dB
Max. Intra-Pair Skew			15	ps
Max. Tx Output Imbalance rms(Vp,Vn)			10	%
**Common Mode Generation V Pk-Pk			50	mV
Random Jitter			0.15	UI
Deterministic Jitter			0.15	UI
Total Jitter			0.3	UI
AC Coupling Cap			12	nF

**** Recommendation Made for Common Mode spec in the frequency domain**

Transmitter Device Rise Fall Times

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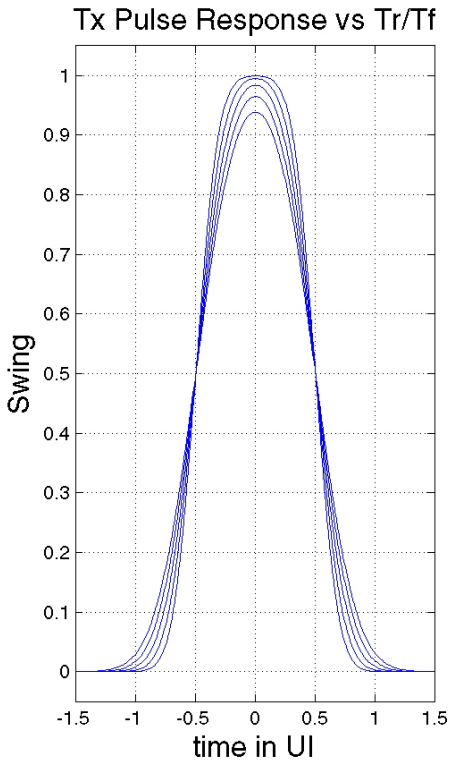
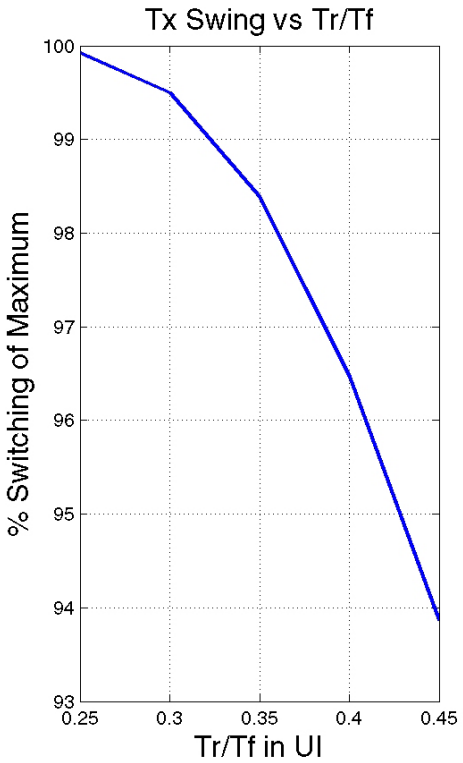
- Propose Tr/Tf = { 0.25 → 0.45 UI } ➔ {41.6667 → 75ps }
- Look at % Switching as a Function of Tr/Tf
- Proposed Range Provides 94% Max Swing and Reasonable Range for Process, Temperature and Voltage Yield





Transmitter Device De-Emphasis Measurement

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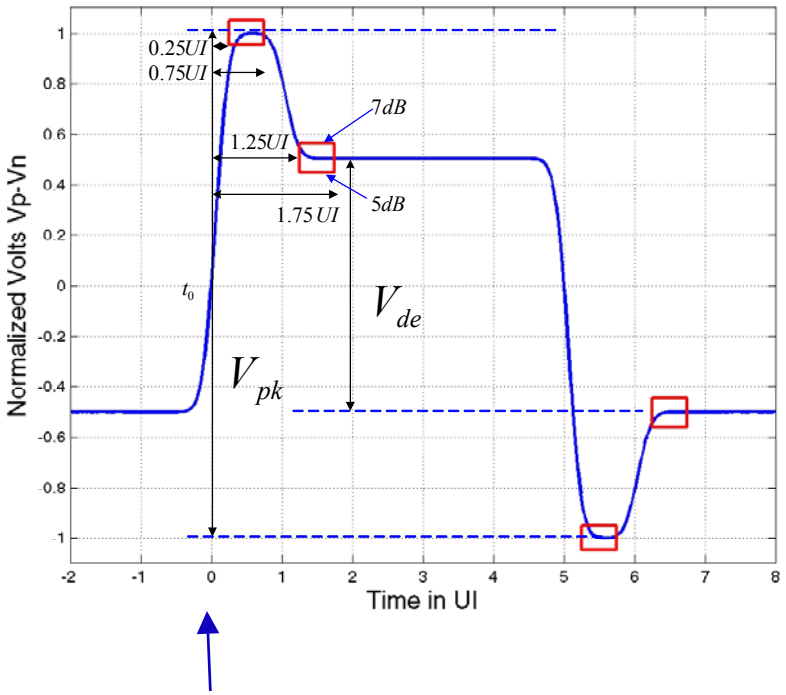
Transmitter De-Emphasis

- Measured into a Zero Length Test Load (CT and IT)
- 6 dB Target 5→7 dB Tolerance
- 23% Tolerance Window

Vpk mV	Vde mV	DE (dB)	CutBack (%)	DE Vtol	DE Vtol %
1200	675	5	44		
1200	601	6	50	139	23%
1200	536	7	55		
800	450	5	44		
800	401	6	50	93	23%
800	357	7	55		

- Modified Proposed Measurement Technique
  - Similar to IEEE 10GBase-KR
  - Define Window for Voltage Measurements



V_{pk} = Maximum Voltage Measured $t_0 + 0.25 \cdot T$ to $t_0 + 0.75 \cdot T$

V_{de} = Minimum Voltage Measured $t_0 + 1.25 \cdot T$ to $t_0 + 1.75 \cdot T$

All Voltage Measurements Referenced to Zero Crossing

$$DE_{dB} = 20Log_{10}\left(\frac{V_{de}}{V_{pk}}\right) \qquad Cutback = \frac{V_{pk} - V_{de}}{V_{pk}}$$

Transmitter Device De-Emphasis Measurement

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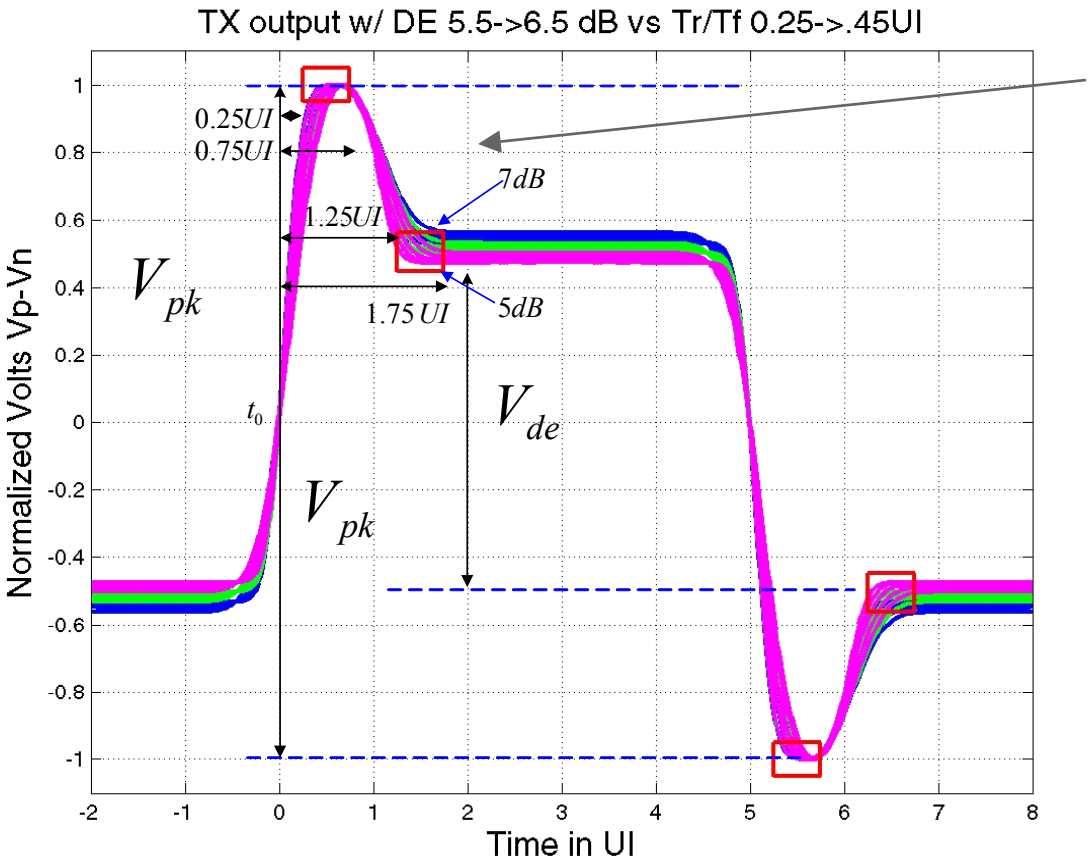
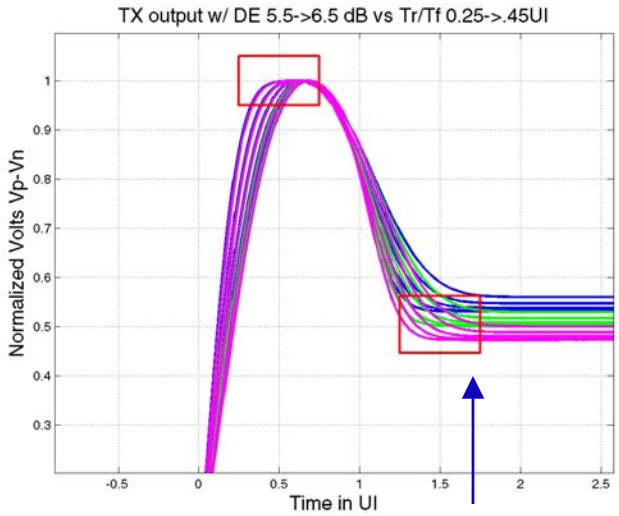
- Transmitter De-Emphasis & Tr/Tf Specifications Are Consistent
  - Sweep Tr/Tf 0.25→0.45 UI
  - Sweep Ideal DE 5.5→6.5 dB
  - All Pass the 5->7 dB Specification



Close Up



5→7dB Specification

Transmitter Device Return Loss Specification

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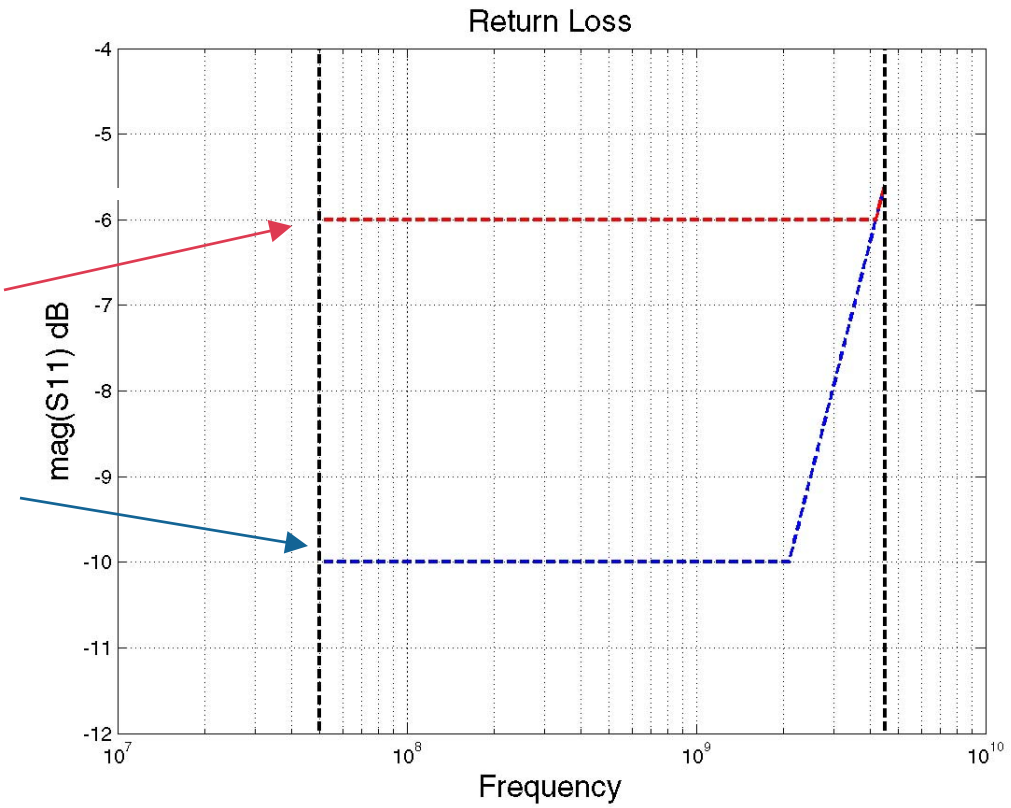
- Based on 8G Fiber Channel (Similar to 10GBase–KR and PCIE 2.0)

for $50MHz < f < 4.5GHz$

$$RL_{cm} = \max\left\{-6, -5.9 + 13.3 * Log_{10}\left(\frac{f}{4.25G}\right)\right\}$$

$$RL_{diff} = \max\left\{-10, -5.9 + 13.3 * Log_{10}\left(\frac{f}{4.25G}\right)\right\}$$



SAS-2 Transmitter Device Proposed Numbers

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Receiver Device Signal Characteristics

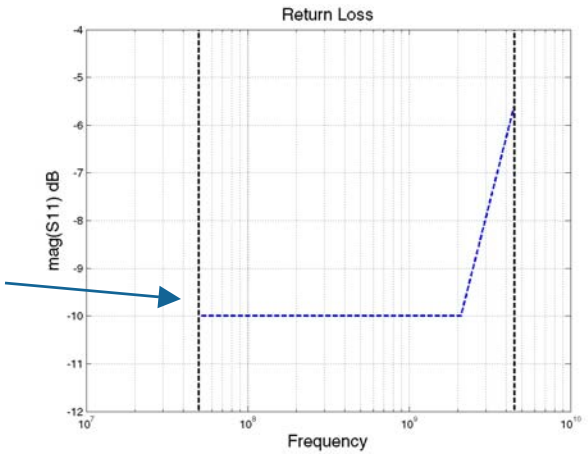
- Measured at (CR and IR)

	SAS-2			
Receiver	Min		Max	Units
DC Differential Impedance		100		ohm
DC Common Mode Impedance	20		40	ohm
Differential Return Loss			See Plot	
Common Mode Return Loss			See Plot	
Common-Mode Tolerance (2-200MHz)	150			mV
Max Operational Input Voltage @ 6GBps	1200			mV
Max Non-Operational Input Voltage	2000			mV

for $50MHz < f < 4.5GHz$

$$RL_{diff} = RL_{cm}$$

$$= \max\left\{-10, -5.9 + 13.3 * Log_{10}\left(\frac{f}{4.25G}\right)\right\}$$



Jitter Tolerance Mask TBD

SAS-2 Channels

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- A Compliant Channel
  - Any Channel Which Will Operated at 1e-15 (1e-12?) With the Given Reference Transmitter and Receiver Device.
  - Operation is Defined as Passing Link Analysis at the TBD Worst Case Corner.
  - Simulation Methodology is up to the User, but is Expected to be Based on Estimated/Measured S-Parameters and Digital Communication Analysis Techniques.
- SAS-2 S-Parameter Models Set Posted to the T10 Serve as Guidance

Incomplete List of Issues

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- SSC Causes Measurement Issues:
  - Tx Jitter Generation
  - Rx Jitter Tolerance
- Tx De-Emphasis Causes DJ Which Needs to be Removed Before Jitter Generation Can Be Estimated?
- Question: Do we Want to Support a Low-Swing Mode for Short / Clean Channels? Just refer to use SATA 2 level for power saving if desired.
  - 400→600mV
  - No De-Emphasis
- Are We Going to Define a Rx Compliance Channel / Test? Yes we need to.
- Are we going to support variable or fixed Tx De-Emphasis?

Summary

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- **Electrical Transmitter and Receiver Device Specifications Provided**
  - **Starting / Discussion Tables Provided for Development**

Additional Information

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- Rx Compliance Test ISI Generator (From 06-053r0)
- LMS Analysis of HP24 w/ and w/ De-Emphasis

SAS-2 Receiver Compliance Test Hardware See 06-053r0

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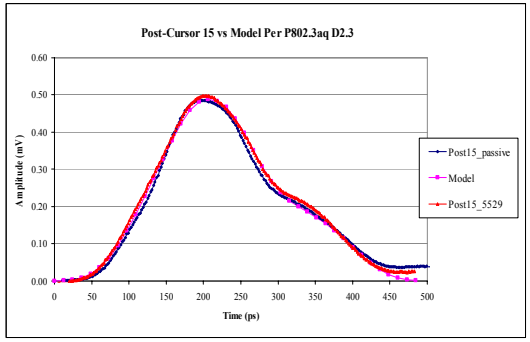
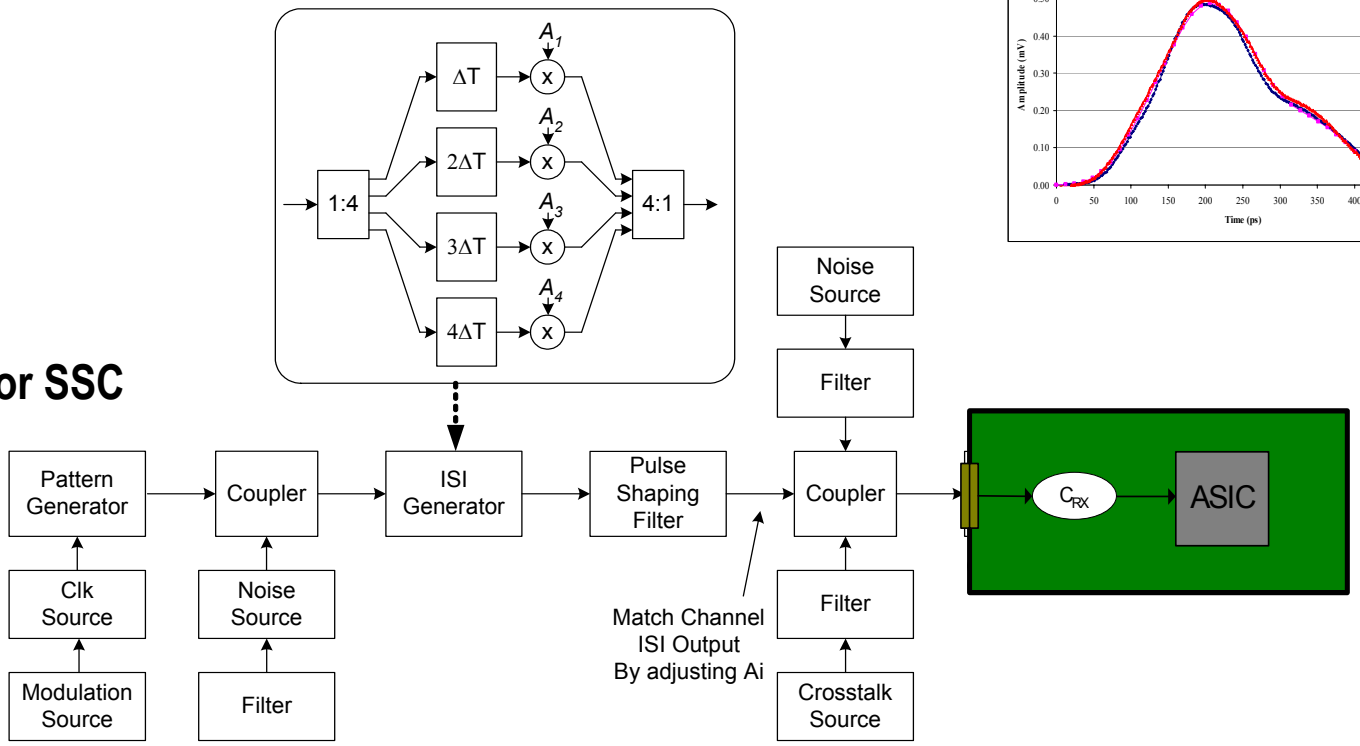
- Receiver Compliance w/ Jitter, Crosstalk and Interference (same as OIF-CEI, & 10GBase-KR)
- Standardize Test Setup based on 10GBase-LRM ISI Generator
  - Generate ISI coefficients for channels of Interest
  - Calibrate and Test Through Mated Connector
  - Emulate Tx DE, C_{TX} & C

10GbE MMF Example



Needs Mod for SSC



Behavior Simulation Methodology

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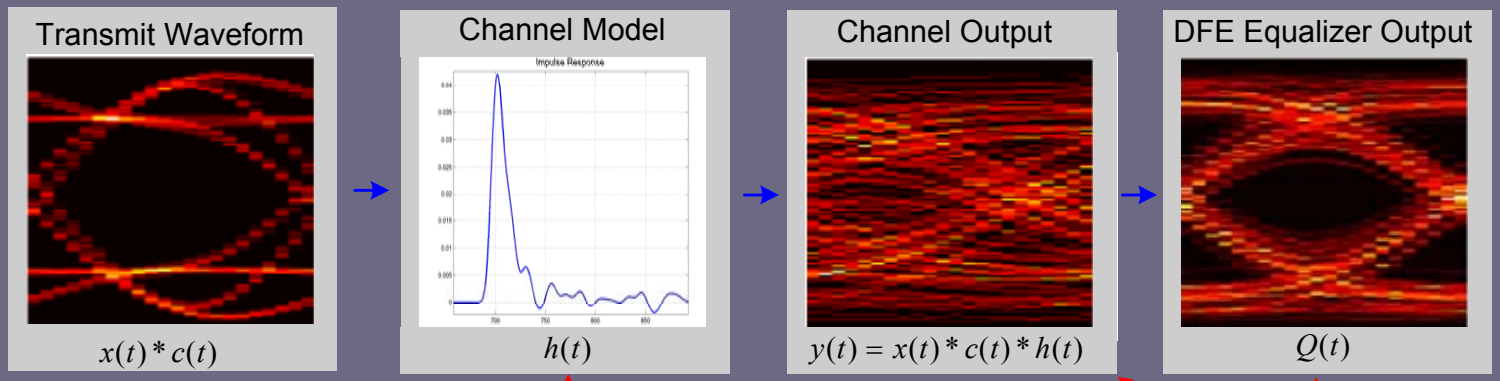
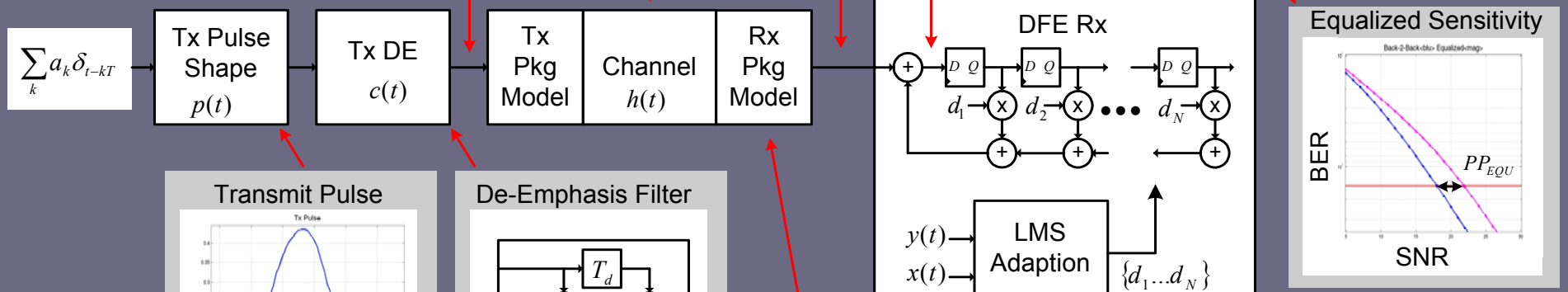
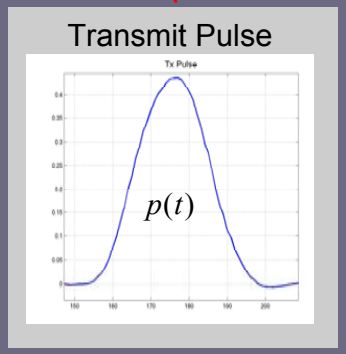
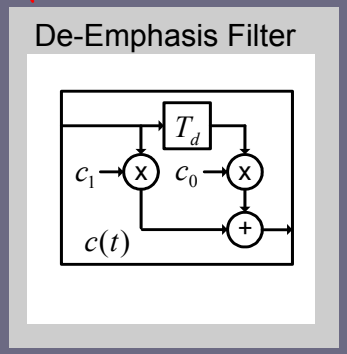
S-Parameter Based Channel Mode









Pulse Shape Based on Test Chip

Mellitz Capacitive Package Mode RL~ 7dB @3GHz

Semi-Analytic BER Used to Estimate Sensitivity Plot

Visual Check of Simulation Methodology

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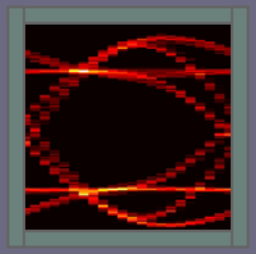
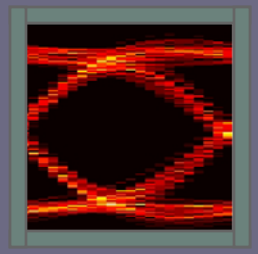
- Simulation vs. Measured
  - 6 Gbps Output Driver Test Chip
  - 6dB 2 Tap De-Emphasis
- Good Agreement With Measured
  - Eye Opening and Eye Shape
  - Jitter at Zero Crossing

6dB De-Emphasis Simulated Eyes

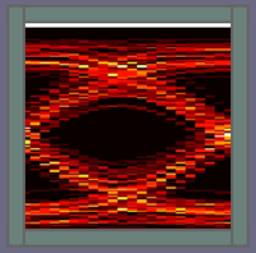
1m



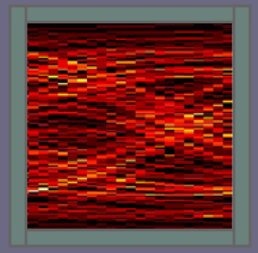
6m



10m

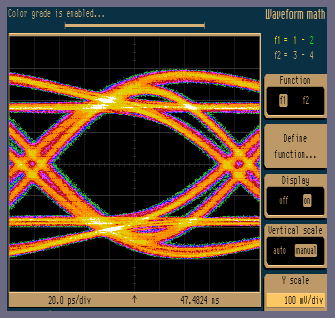


15m

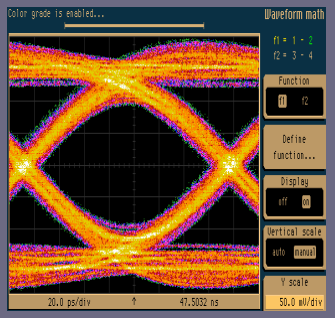


6dB De-Emphasis Measured Eyes

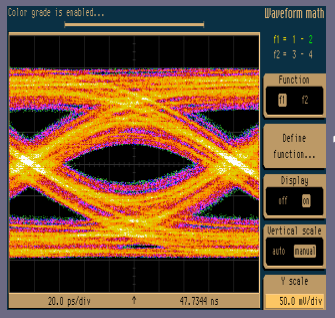
1m



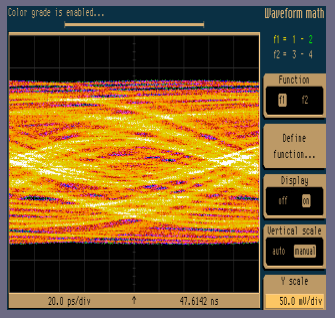
6m



10m



15m



HP24 w/ 2-Tap DFE

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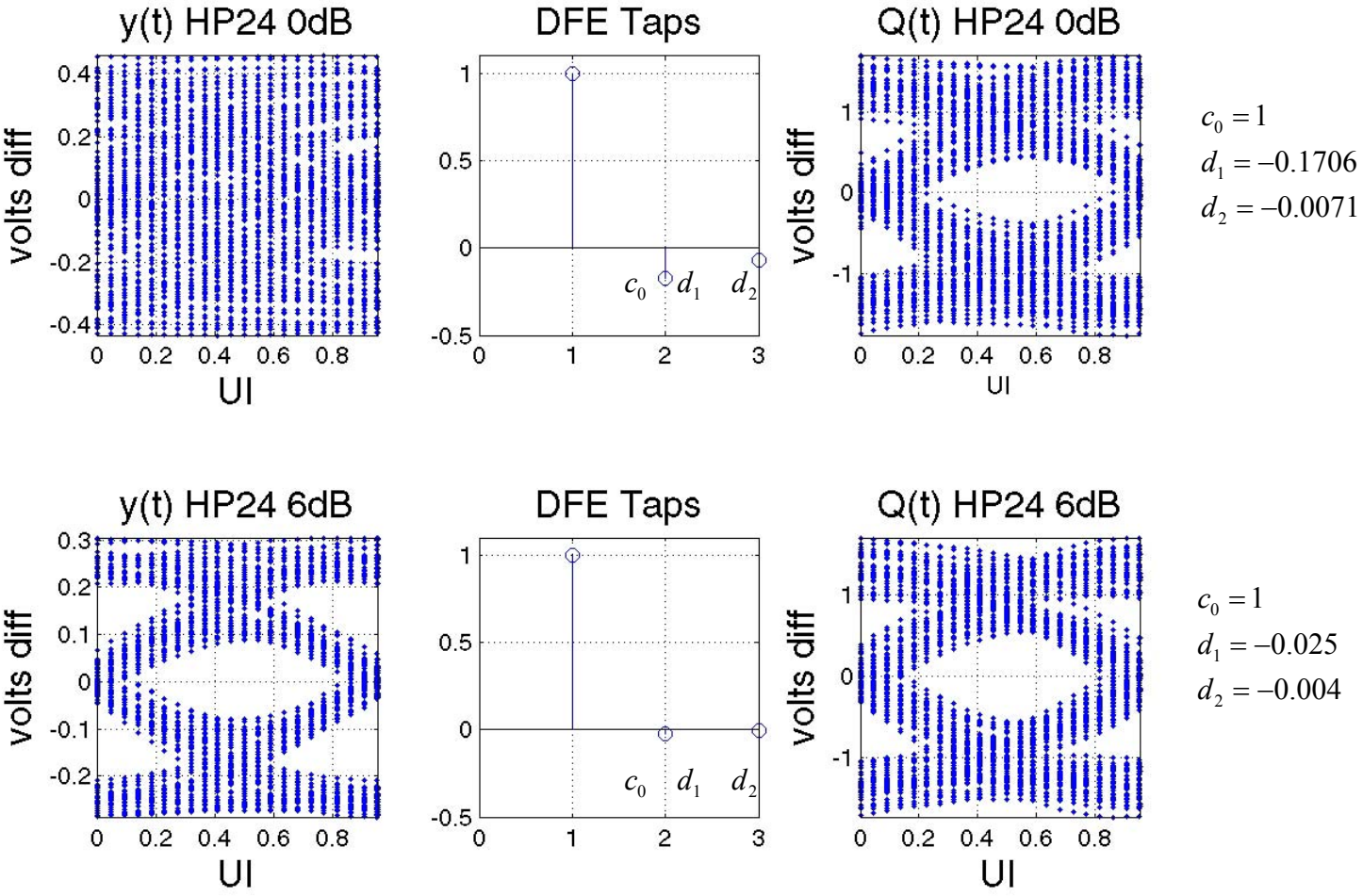
- LMS Solution to HP24 – Emulation of this channel yielded equal margin with nor without Tx De-Emphasis (Using Test Chip Tx Waveform)

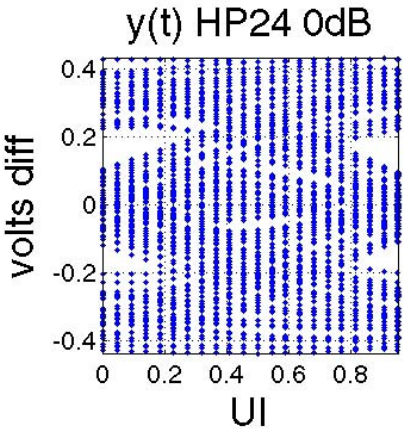


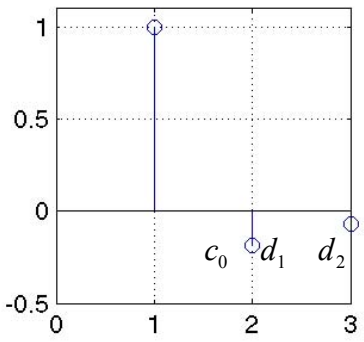
Channel Output **DFE Output (Output Scaled to +/-1)**

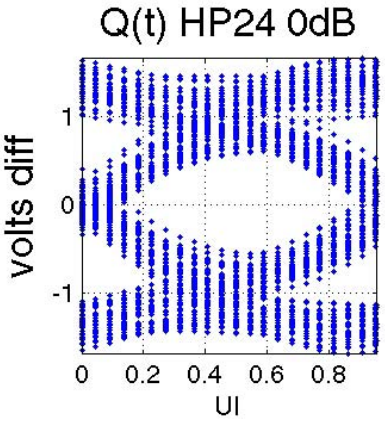
HP24 w/ 2-Tap DFE

VITESSE

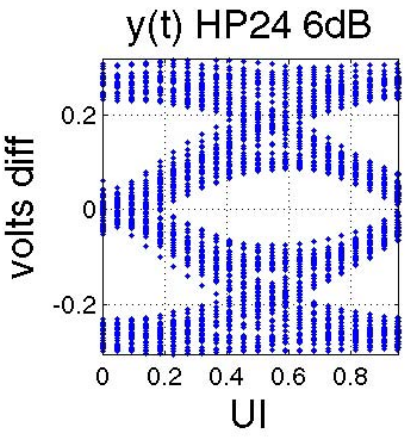
- LMS Solution to HP24 – Emulation of this channel yielded equal margin with nor without Tx De-Emphasis (Using Gaussian 0.3UI Tr/Tf Tx Waveform)

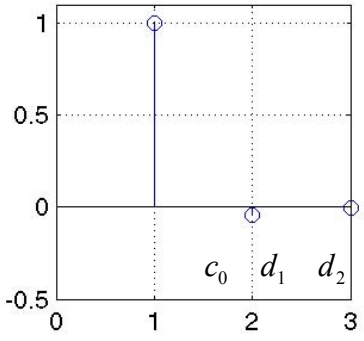


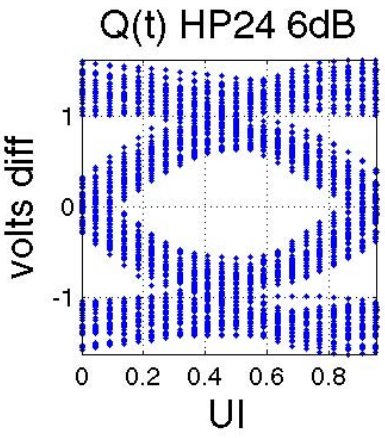




$c_0 = 1$
$d_1 = -0.1883$
$d_2 = -0.067$







$c_0 = 1$
$d_1 = -0.045$
$d_2 = -0.004$

Channel Output

DFE Output (Output Scaled to +/-1)