Attendance:

Mr. Ziad Matni	Agere Systems
Ms. Fei Xie	Agilent Technologies
Mr. Kevin Marks	Dell, Inc.
Mr. David Freeman	Finisar
Mr. Rob Elliott	Hewlett Packard Co.
Mr. Dan Colegrove	Hitachi Global Storage Tech.
Dr. Mark Seidel	Intel Corp.
Mr. Praveen Viraraghavan	LSI Logic Corp
Mr. Brian Day	LSI Logic Corp.
Ms. Juan Wang	Marvell Semiconductor, Inc
Mr. Paul Wassenberg	Marvell Semiconductor, Inc
Mr. David Geddes	Marvell Semiconductor, Inc.
Mr. Johnson	Marvell Semiconductor, Inc.
Mr. Wei Zhou	Marvell Semiconductor, Inc.
Mr. Galen Fromm	Molex Inc.
Mr. Hock Seow	NEC Electronics America, Inc
Mr. Amr Wassal	PMC-Sierra
Mr. Robert Watson	PMC-Sierra
Mr. Alvin Cox	Seagate Technology
Mr. Dan Smith	Seagate Technology
Ms. Judy Westby	Seagate Technology
Mr. Benoit Mercier	STMicroelectonics
Mr. Stephen Finch	STMicroelectronics
Mr. Massimo Pozzoni	STMicroelectronics
Mr. Doug Loree	Toshiba
Mr. Kevin Witt	Vitesse Semiconductor

26 in attendance

Agenda:

1. Speed negotiation sequence
SAS-2 SNW-3 Definition (06-355) [Wassal & Watson]
http://www.t10.org/ftp/t10/document.06/06-355r1.pdf

Uses existing RCDT.
Provides start bit plus retry bit.
If the retry bit values are different, then reset to initial values.
Incorporates marker bits every 9th location. These should be deleted per discussion.
Provides 56 bits + 8 CRC bits + 8 STOP bits.
The 56 bits need to be defined.

**Long burst versus COMWAKE for communication. COMWAKE may have an advantage
with the existing RCDT leaving only 100us for the data window.**

**Is there a problem with crosstalk being detected as a valid OOB sequence on neighbors?
SATA in slumber may be at an effective high impedance. SAS drives already send OOB at
SAS levels.**

**"CRC" is used as reference nomenclature for checking that the data was received
correctly. Is there a simple validation method? Is a validation method wanted? Previous**

discussions indicated that verification of correctly receiving data is desirable. What can be used? Need a proposal defining this. It was suggested during the call that we could possibly use the "keep alive 9th bit as a parity bit. Reference information supplied by Rob Elliott:
This is a tool that generates the XOR equations (in Verilog or VHDL) for any CRC polynomial and data width:

   http://www.easics.com/webtools/crctool

Information transferred:
Speeds supported
SSC transmitter capabilities
SSC currently being used (does this help?)
Channel class (loss) – Initiator-type would only have knowledge; End device could use.
Additional suggestions?

Rob Elliott to generate a proposal and post for next week's discussion.

If one port of a drive negotiated SSC on and the other port negotiated SSC off, the drive is allowed to shut SSC off on both ports provided there is a graceful method to shut if off. (Priority to SSC OFF)

What voltage level will this OOB communication be done at? COMSAS has already been negotiated and the preceding two windows were done at SAS levels. G3 is expected to be specified at 1200mV pk-to-pk max with some minimum specified, so should that be the level used? Initial OOB is started at SATA levels of 400-600mV pk-to-pk if attachment to SATA is supported.

Definitely at SAS level. See comments above concerning crosstalk.

Automatic rate or feature reduction:
Concerned that a link may not be performing at its highest potential, but it seems that the system could detect this and identify the issue. This is complicated in the fact that if a 6Gbps device failed at 6Gbps but worked at 3Gbps, how would the system know that it was a 6Gbps-capable device if the expander did the negotiation? Is this something that is available in a mode page or other identification?

2. Window 4 structure

Seed value?
A concern was raised that using the scrambler in the training sequence may involve the link layer. Seagate suggests that the 0 seed not be required with every window. Intel also expressed support.

Start of window:
Since the last interval in the configuration window is idle, the training data may start at the beginning of the final speed negotiation window, but shall start by the end of a defined RCDT (not necessarily the same length of time as the previous RCDT's). Input is needed on how long this RCDT should be.

Completion of window:
How is the final speed negotiation window completed? Should there be ALIGN0/ALIGN1 after TRAINdone is exchanged to verify dword sync?
Need to verify the impact to state machines to determine if the ALIGN exchange is needed.

Failure of G4 window next steps.

Reference documents:

SAS-2 Start-up training sequence (05-397) [Newman]
http://www.t10.org/ftp/t10/document.05/05-397r5.pdf

Next conference call Aug 3, 2006

Agenda:

Long burst versus COMWAKE.
Review information transferred proposal by Rob.
Information transferred validation.
Final speed negotiation window details.

PARTICIPANT INFORMATION:

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Webex information:
https://seagate.webex.com/seagate
Topic: SAS-2 PHY WG
Date: Thursday, Aug 3, 2006
Time: 10:00 am, Central Daylight Time (GMT -05:00, Chicago)
Meeting number: 826 515 680
Meeting password: 6gbpsSAS