Minutes of SAS Physical Working Group teleconference, June 23, 2006 T10/06-296r0

Attendance

Mr. Bernhard Laschinsky	Agere Systems
Mr. Ken Paist	Agere Systems
Mr. Bryan Kantack	Agilent
Mr.David Freeman	Finistar
Mr. Barry Olawsky	Hewlett Packard Co.
Mr. Rob Elliott	Hewlett Packard Co.
Mr. Harvey Newman	Infineon
Mr. Schelto van Doorn	Intel Corp
Mr. Michael Jenkins	LSI Logic Corp.
Mr. Praveen Viraraghavan	LSI Logic Corp.
Mr. Gabriel Romero	LSI Logic Corp.
Mr. David Geddes	Marvell
Mr. Jeff Choun	Marvell
Mr. Paul Wassenberg	Marvell
Ms. Helen Liu	Maxxim
Mr. Yuriy Greshishchev	PMC-Sierra
Mr. Henry Wong	PMC-Sierra
Mr. Amr Wassel	PMC-Sierra
Mr. Alvin Cox	Seagate Technology
Mr. Dan Smith	Seagate Technology
Mr. Ivan Bietti	ST Microelectronics
Mr. Massimo Pozzoni	ST Microelectronics
Mr. Doug Loree	Toshiba
Mr. Adrian Robinson	Vitesse Semiconductor
Mr. Jim Welch	

25 People Present

Agenda:

SSC

http://www.t10.org/ftp/t10/document.06/06-263r2.pdf

Discussed Rob's updated proposal. Has included references to SSC information on the internet and started making changes to describe SSC. Follow-up teleconferences will be held on June 29 and July 6 prior to the SAS PHY working group face-to-face on July 11.

Regarding the updates, it was determined that the clock tolerance should not be included in the spread numbers.

Are definitions for down spreading and center spreading acceptable?

Table 52 and 53 titles need to be changed. Move frequency numbers to a separate table and only identify SSC type with application.

ST indicated that they would rather train on an SSC signal rather than a non-SSC signal. Agere and Vitesse indicated that it is better to train on non-SSC, but there would be a need to verify signal integrity after SSC is turned on. Training with SSC enabled is probably possible, but this has no data to support that it can actually be done. **It was suggested that it be assumed on for now and if it has to be changed later, then it can change.** To change it later could be a

significant design impact for drives. Expanders are expected to have independent control of SSC on PHY's already, so the impact would be less for them.
SSC can be enabled and disabled without significant impact to the transmitted signal if done at the zero-crossing but it may take several microseconds to make the change from SSC to non-SSC.

Should a minimum SSC range be specified? Rob indicated he wants a minimum specified, but most who voiced an opinion did not support a minimum setting. SATA initially had problems with SSC but these seem to be getting better over time. One comment made indicated that the SATA ranges seen by that person typically from 1000 ppm to 3000 ppm rather than the full 5000 ppm allowed. Many thought it best to be a purchase specification requirement rather than a standard if a minimum value is desired.

Several comments were made regarding EMI and the SSC pattern. The pattern requirements still need some sort of clarification so that an issue of overrunning buffers is not caused, but also that the pattern is effective in reducing EMI. The "area under the curve" approach was mentioned. But it in itself can permit a square wave implementation that would cause a buffer overrun issue.
Ideas on how to define should be posted to the reflector or sent to Rob.

Rob will update his proposal based on today's discussion and post over the weekend.

Speed negotiation sequence

http://www.t10.org/ftp/t10/document.06/06-295r0.pdf

- Reviewed the new presentation and had some concerns about the final negotiation window RCDT. Do expanders with many PHY's need more than 300uS to process the information?
- Should there be a fixed value or just start sending training pattern when ready?
- How should the configuration data be sent? Should it be a 32-byte packet, handled by new primitives, or some other option?
- What information should be included?

Please respond with comment to the reflector or to Amr Wassel (PMC Sierra)

Additional items needing investigation/comment:

- Should SSC be on or off during receiver equalization setting?

Today's comments indicated that there are both advantages and disadvantages to having SSC active during the initial setting process. Having it on while setting equalization is an untested item, but is probably possible. If setting is done while it is off, then the signal reception needs to be verified after it is turned on.

- Is it viable to make a drive have independent SSC control on the transmitters of its two ports? Independence is required to set the receiver equalization without SSC since one port may be operating prior to the other one performing speed negotiation.

It is possible in some designs, but an alternate suggestion of turning off SSC at a zero-crossing for both PHY's was proposed as an alternative. There may be some timing issues with a smooth disable of SSC.

- In the beginning of the final speed negotiation window, does there need to be an idle time or can both devices immediately start transmitting the training pattern? It is assumed that if G2 is required, the sequence would follow the SAS 1.1 standard.

A 300uS window was suggested in the 06-295. Since this is close to the existing RCDT of the other windows and minimal compared to the training interval maximum time, it was suggested to just use the existing RCDT time. Some indicated they would like to go ahead and start the training pattern when they were ready rather than at a set time. Additional feedback is needed regarding this. It was also stated that some expanders with many PHY's may have a problem getting the information processed in that amount of time if all the PHY's were trying to communicate with the processor at the same time.

- It is assumed that all expanders and initiators are capable of receiving downspread SSC. Are there any know exceptions?

Still needs to be answered with a positive or negative response.

- Will an initiator or expander accept downspreading from a SAS device running at G1 or G2 speed?

Still needs to be answered with a positive or negative response.

- If a phy transmitter has SSC disabled or is using downspread SSC only, it could get away with inserting fewer ALIGNs - 1/128 (the SATA ratio) would cover sending to either SAS or SATA phys with downspread SSC. Is that complication worth a 0.8% performance improvement? (e.g. at 6 Gbps, this is 4.77 MBps). Use 1/64 for all?

Please comment on this.

If at all possible, it would be of great benefit to have the SSC and speed negotiation sequence resolved at the July T10 meeting. These items are the most critical as they impact ASIC design. Other specification issues are likely to be controlled by adjustable parameters while these issues likely affect basic hardware design.

Next conference call June 29, 2006

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Webex information:
https://seagate.webex.com/seagate
Topic: SAS-2 PHY WG
Date: Thursday, June 29, 2006
Time: 10:00 am, Central Daylight Time (GMT -05:00, Chicago)
Meeting number: 826 515 680
Meeting password: 6gbpsSAS