Attendance

Mr. Andy Turudic	Agere Systems
Ms. Pat Thaler	Agilent
Mr. Paul von Stamwitz	AMCC
Mr. Howard Chang	AMCC
Mr. Brian Miller	Amphenol Assembletech
Mr. Paul Griffith	Broadcom Corp.
Mr. Ron Roberts	Broadcom Corp.
Mr. Clemet Yuen	Broadcom Corp.
Mr. Ichiro Fujimri	Broadcom Corp.
Mr. Ali Ghiasi	Broadcom Corp.
Mr. Sagar Kenkare	Broadcom Corp.
Mr. James Lott, Jr.	Dallas emiconductor
Mr. Patrick Carrier	Dell, Inc.
Mr. David Freeman	Finistar
Mr. Michael Lawson	Finistar
Mr. Douglas Wagner	FCI
Mr. Johnathan Buckr	FCI
Mr. Dejan Mijuskovic	Freescale Semiconductor
Mr. Mike Fitzpatric	Fujitsu
Mr. Rob Elliott	Hewlett Packard Co.
Mr. William Ham	Hewlett Packard Co.
Mr. Joe Foster	Hewlett Packard Co.
Mr. J. P. Miller	Hewlett Packard Co.
Mr. Thomas Grieff	Hewlett Packard Co.
Mr. Dennis Alexander	Hewlett Packard Co.
Mr. Greg Larson	Hewlett Packard Co.
Mr. Matt Schumacher	Hewlett Packard Co.
Mr. Kevin Leigh	Hewlett Packard Co.
Mr. Pak Chan	Hewlett Packard Co.
Mr. Keveh Naderi	IBM
Mr. Harvey Newman	Infineon Technologies
Mr. Andrew Cable	Intel Corp.
Mr. Mark Seidel	Intel Corp.
Mr. Mike Y. He	Intel Corp.
Mr. Bill Bissonette	Intel Corp.
Mr. James Mueller	LeCroy Corporation
Mr. Mike Micheletti	LeCroy Corporation
Mr. Frank Gasparik	LSI Logic Corp.
Mr. Michael Jenkins	LSI Logic Corp.
Mr. Wei Zhou	Marvell Corp.
Mr. David Geddes	Marvell Corp.
Mr. Mark Evans	Maxtor Corp.
Mr. Richard Uber	Maxtor Corp.
Mr. Eric Kvamme	Maxtor Corp.
Mr. Mike Jackson	Mindshare, Inc.
Mr. Jay Neer	Molex
Mr. Galen Fromm	Molex
Mr. Mitsutoshi Sugawara	NEC Electronics America
Mr. Hock Seow	NEC Electronics America
Mr. Michael Hopgood	Nvidia Corp.
Mr. Yurley Greshishchev	PMC-Sierra

Mr. Ting Chan	QLogic Corp.
Mr. Arie Krantz	QLogic Corp.
Mr. Henry Kuo	QLogic Corp.
Mr. Mike Lerer	Rapid Prototypes, Inc.
Mr. Alvin Cox	Seagate Technology
Mr. Allen Kramer	Seagate Technology
Mr. Willis Whittington	Seagate Technology
Mr. Brent Hessen-Schmidt	Synthesys Research, Inc.
Mr. David Helster	Tyco Electronics
Mr. Dave Griesemer	Tyco Electronics
Mr. David Allen	Vitesse Semiconductor
Mr. Kevin Witt	Vitesse Semiconductor
Mr. Michael Yeager	Vitesse Semiconductor
Mr. Phillip Roberts	Vitesse Semiconductor
Mr. Nick Van Bavel	Vitesse Semiconductor

66 people identified, 82 present

The meeting started at 9:00 am, May 25, 2005.
HP was thanked for sponsoring the meeting.
Attendees introduced themselves.

The following is a list of the presentations and their links to the T10 web site. I have included some notes on most presentations that may be useful if looking for something in particular. The notes do not represent the T10 position and should not be considered as a bias for or against a particular subject. They may reflect the comments of either the presenter or a participant at the meeting and may be worth considering during the review of the presentation material. The links were current at the time of posting. Check the T10 site for possible updates, as some presentations were to be revised.

05-219r0 Survey of high-speed serial technologies - Yuriy Greshischev, PMC-Sierra
http://www.t10.org/ftp/t10/document.05/05-219r0.pdf

XAUI
Compliance channel with only S21, okay since requires physical compliance channel.
XFI
9.95 – 11.1 Mbps, 200mm, one connector plus FR4, specifies advanced S parameters, interoperability by test board
OIF CEI
BER <10-15, Comprehensive specification including jitter

Multi-level
PAM-4 (four level) - Not used by any standard to date
Duo-binary (three level) - 802.3ap was considering but ended up with NRZ

FCAL MJSQ – open eye or closed eye processed to open it
Stateye – closed eye

Transceiver equalization @ 6 Gbps
- Discrete time filters
- Continuous time filters
- Decision Feedback equalizer

05-215r0 IEEE 802.3ab (Gigabit Ethernet: 1000BASE-T) and IEEE 802.3an (10 Gigabit Ethernet: 10GBASE-T) - Nick Van Bavel, Vitesse
http://www.t10.org/ftp/t10/document.05/05-215r0.pdf

Overview of Ethernet signaling, coding, filtering and media issues
100B-T 50k 170mW
1000B-T 62.5Mhz 500k 500mW
10GB-T 400Mhz 10M gate for signal processing 14.5 W (conservative) 20 W in 90 nm

UTP cheap cable?
15W, 10uS latency, 10M gates
Probably no a good starting place for SAS. Even reduced length cable does not meet 4W maximum power, latency too long, and gate count too high.

05-202r0 IEEE 802.3aq Overview (10 Gigabit Ethernet on FDDI-grade MMF cable: 10GBASE-LRM) - Kevin Witt, Vitesse
http://www.t10.org/ftp/t10/document.05/05-202r0.pdf

Optical
Technique Chosen
• NRZ w/ Center and Offset launch
• No Training sequences (blind equalization)

Eye is closed in RX Stress test at Rx end
Tx/Rx Compliance testing applicable to SAS?

05-214r1 IEEE 802.3ap (Backplane Ethernet) 1 Gbps/10 Gbps - Ali Ghiasi, Broadcom
http://www.t10.org/ftp/t10/document.05/05-214r1.pdf

FLP “OOB” not XCVR Friendly for > 3 Gb/s
– Requires turning on/off transmitter very quickly ~100 ns pulse.
– Receiver must have envelope detect to detect bursts.
– PLL must acquire lock and adapt at the start of each training sequence

Has both transmitter and receiver electrical requirements.
Compliance channel includes summing to include crosstalk and reflections.
Biggest challenge is stub length on backplanes

SAS Auto-negotiation can leverage 802.3ap DME (Differential Manchester Encoding) to overcome OOB limitations.

05-208r0 INCITS T11 Fibre Channel Signal Specification Architecture - application to higher speeds - Bill Ham, HP
http://www.t10.org/ftp/t10/document.05/05-208r0.pdf

Bill Ham’s overview of channel based versus connector based specifications

As far as the standards are concerned it is only the mating interface of the connectors that needs to remain backward compatible: the rest of the connector and its mounting interface may need to change, however –the SCA-2 is good at least to 8.5G (SCA-2’s are used mostly for Beta points)

05-200r0 Overview of OIF CEI - Mike Lerer, Rapid Prototypes
http://www.t10.org/ftp/t10/document.05/05-200r0.pdf

CEI-6G Specifications

- Baud Rate 4.976 to 6.375 Gigabaud/second
- NRZ Differential Signaling
- Nominal Impedance 100 Ohm
- Supports Hot Plug
- AC coupling Required - assumed part of receiver
- DC Coupling Optional
- BER 10-15

05-210r0 OIF-CEI-6G overview - Yuriy Greshischev, PMC-Sierra
http://www.t10.org/ftp/t10/document.05/05-210r0.pdf
05-199r0 Next Gen Serial Rapid I/O (SRIO) PHY Preliminary 5.0/6.25 Gbps Electrical Spec Status [Mike Lerer, Rapid Prototypes]
http://www.t10.org/ftp/t10/document.05/05-199r0.pdf

Multi-lane striping.
Looking at OIF specification model.
Willing to work with T10 and share technical data on scrambling, CRC, DFE, etc.

05-198r0 Channel Compliance Testing Utilizing Novel Statistical Eye Methodology (StatEye) - Harvey Newman, Infineon
http://www.t10.org/ftp/t10/document.05/05-198r0.pdf

Channel compliance tool. Has issues as far as being used as a normative spec for receiver. Doesn't work with CJTPAT.

05-203r0 SAS-2 6Gbps Test Results - Kevin Witt, Vitesse
http://www.t10.org/ftp/t10/document.05/05-203r0.pdf

Presentation of idealized backplane and external cable test results. Did not include noise sources. Amplitude was not stated or the amount of de-emphasis required. Did not know whether the de-emphasis would fit within a 1200/800 mV pk-pk transmitter spec.

05-211r0 PMC-Sierra QuadPHY 6G device - Yuriy Greshischev, PMC-Sierra
http://www.t10.org/ftp/t10/document.05/05-211r0.pdf

05-221r0 6G Data over Legacy Backplanes - Mike Jenkins, LSI Logic
http://www.t10.org/ftp/t10/document.05/05-221r0.pdf

Feed-forward equalization and decision feedback equalization. OIF 6G-LR, 350mW WC per duplex channel.
Data eye for 35" FR4 has 62% pre-emphasis with 1V pk-to-pk signal.

05-216r0 and 05-217r0 OIF backplane at 6 Gbps and 11 Gbps - Galen Fromm, Molex
http://www.t10.org/ftp/t10/document.05/05-216r0.pdf
http://www.t10.org/ftp/t10/document.05/05-217r0.pdf

05-220r0 SAS 6 Gbps proposal based on OIF CEI 6G-LR - Mike Jenkins, LSI Logic
http://www.t10.org/ftp/t10/document.05/05-220r0.pdf

Open eye spec won't work at 6Gbps.
5-tap DFE in reference RX is relatively costly and probably not required for a SAS environment.
OOB should have some "slow limit".

05-204r0 Towards a SAS-2 Physical Layer Specification - Kevin Witt, Vitesse
http://www.t10.org/ftp/t10/document.05/05-204r0.pdf

Need cable length and backplane length to determine what to spec.
Need direction from STA regarding usage models.

05-218r0 Mini SAS 4i/4x connector performance at 6 Gbps - Galen Fromm, Molex
http://www.t10.org/ftp/t10/document.05/05-218r0.pdf

Revision will be posted.

05-212r0 SAS-2 System design considerations - Barry Olawsky, HP
http://www.t10.org/ftp/t10/document.05/05-212r0.pdf

HP wish list of features:
SATA support (verbal - 800mV eye opening at transmitter good for backplanes)
PHY knobs for amplitude, slew rate and pre-emphasis
BER should be better than <10-12
External cable length concerns
FCAL is looking at CAT-5, so should SAS look at this for longer cheap cable?
Since other protocols deal with packets rather than link ownership, should SAS be looking at this?

05-209r0 SAS OOB challenges: scale or not to scale - Yurey Greshischev, PMC-Sierra
http://www.t10.org/ftp/t10/document.05/05-209r0.pdf

Alvin will send the proposal to the T10 reflector to get responses concerning shipping product and future expectations.

05-222r0 Problems with PAM4, linear equalization, PR2, PR4, etc. - Mike Jenkins, LSI Logic
http://www.t10.org/ftp/t10/document.05/05-222r0.pdf

Actions:

Alvin to post notice of OOB rate proposal to reflector for feedback.

STA:
Define usage model expectations for 6Gbps (External cable length, internal connection requirements (number of connectors, media types, and lengths)
Is a CAT-5 application necessary or reasonable?

Adjournment 5:08pm May 26, 2005