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# OIF CEI 6G LR OVERVIEW

*Graeme Boyd, Yuriy Greshishchev*

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# Outline

- Why CEI-6G LR is of Interest to SAS-2 ?
- CEI-6G- LR Specification Methodology
- CEI-6G- LR Requirements Summary
- OIF CEI-6G Extrapolation to SAS-2

# Why CEI-6G is of Interest to SAS-2 6G ?

- CEI-6G methodology and requirements were developed with main target to double the throughput of “legacy backplanes” from (2.5 -3.125) Gb/s to (5-6.25 ) Gb/s with low BER < 1e-15

- CEI-6G is a ratified document, interoperability was demonstrated by a number of silicon vendors

- CEI-6G evolves in CEI-11G – a possible path to future generations after SAS-2

# Optical Internetworking Forum Framework

**Physical and Link Layer (PLL) Working Group:**

- Electrical Interfaces for OC-192, OC768
  - Framer and packet interfaces (SFI-4, SFI-5, SPI-4, SPI-5, SXL-5), TFI
- Common Electrical Interfaces
  - CEI 6G-LR, CEI 6G-SR
  - CEI 11G

# CEI 6G, 11G Documents

- **CEI-02.0** "Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O"
  - CEI-6G-SR/LR & CEI-11G-SR were ratified in Dec 2004
  - CEI-11G-LR/MR were ratified in Feb 2005

- OIF CEI6G was extensively covered at DesignCon: "Introducing the OIF Common Electrical I/O Project" DesignCon 2004.

# Jitter Methodologies

- Fiber Channel Methodology for Jitter and Signal Quality Specification – MJSQ (MJS-1999, MJSQ, rev14 -2004)
  - Deals with the "Open Eye" interfaces
  - Originally was developed to serve FC specifications, however has become an industry wide methodology
  - Defines jitter components, Tx,Rx measurement methods
- Statistical Eye (OIF)
  - Was mainly developed to target "Closed Eye" interfaces with BER requirement $<10^{-15}$-$10^{-18}$. Based on analytical BER simulation technique ("StatEye") with 5-tap ideal DFE to open the eye and S-parameters to represent the "channel"
  - StatEye.org is a non-profit open source forum. Operates under the open source license agreement. [www.StatEye.org](www.StatEye.org)
  - OIF is working on cleaning the code up (consultant)

# OIF Jitter and Interoperability Methodology: A

- Method A: Interfaces where neither transmit emphasis or receiver equalization are required for the receiver eye to be open to within the BER of interest
  - Define test patterns:CID=72; PRBS31
  - Channel interoperability
    - Channel and crosstalk S-parameters, Tx,Rx return loss
    - Use Statistical Eye Analyses method to confirm BER, that is eye opening:
      - Amplitude at time zero sampling point
      - Jitter at zero amplitude sampling point
  - Tx interoperability
    - The Tx jitter components
    - Tx Eye mask
  - Rx interoperability
    - Should pass BER test for a stressed signal

# OIF Jitter and Interoperability Methodology: B-E

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- **Method B:** where transmit emphasis may be used however receiver equalization is not required for the receiver eye to be open to within the BER of interest
- **Method C:** where transmit emphasis may be used and the receiver eye requires Linear Continuous Time equalization (from channel interoperability point of view) to be open to within the BER of interest
- **Method D:** where transmit emphasis may be used and the receiver eye requires DFE equalization (from channel interoperability point of view) to be open to within the BER of interest
- **Method E:** where a simple receiver equalization may be used to improve the margin of the link and transparent applications may be used and the receiver eye is still open to within the BER of interest.

# OIF CEI-6G Specification Method

- For CEI-6G-SR the OIF has chosen to specify the transmitter and receiver. This then implies what are compliant channels.
  - Similar to most other SERDES standards, except that OIF is using statistical eye's rather than worst case eye's
  - Method B
- CEI-6G-LR can have a closed eye at the receiver, standard methods do not work anymore, so OIF has chosen to move the "receiver" spec point to after an "ideal 5 tap DFE". Thus specifying the transmitter and compliment channels while implying the receiver spec.
  - The real receiver implementation needs to be equivalent or better than a 5 tap DFE
  - Method D

# CEI-6G Definitions

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CEI6G: 4.976 – 6.375Gbps

SR: 0 – 200mm, up to 1 connector

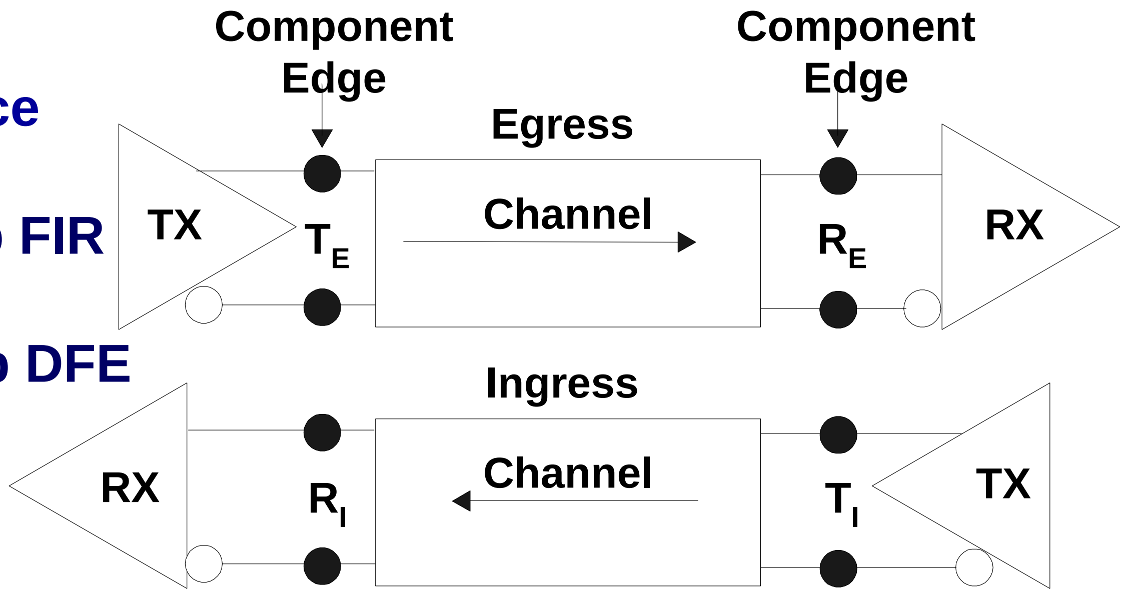
LR: 0 – 1000mm, up to 2 connector

PCB channel, NRZ

Reference Models:

Tx: 2-tap FIR

Rx: 5-tap DFE




**Does specify:**

-Data characteristics

-Channel models

-Compliance points

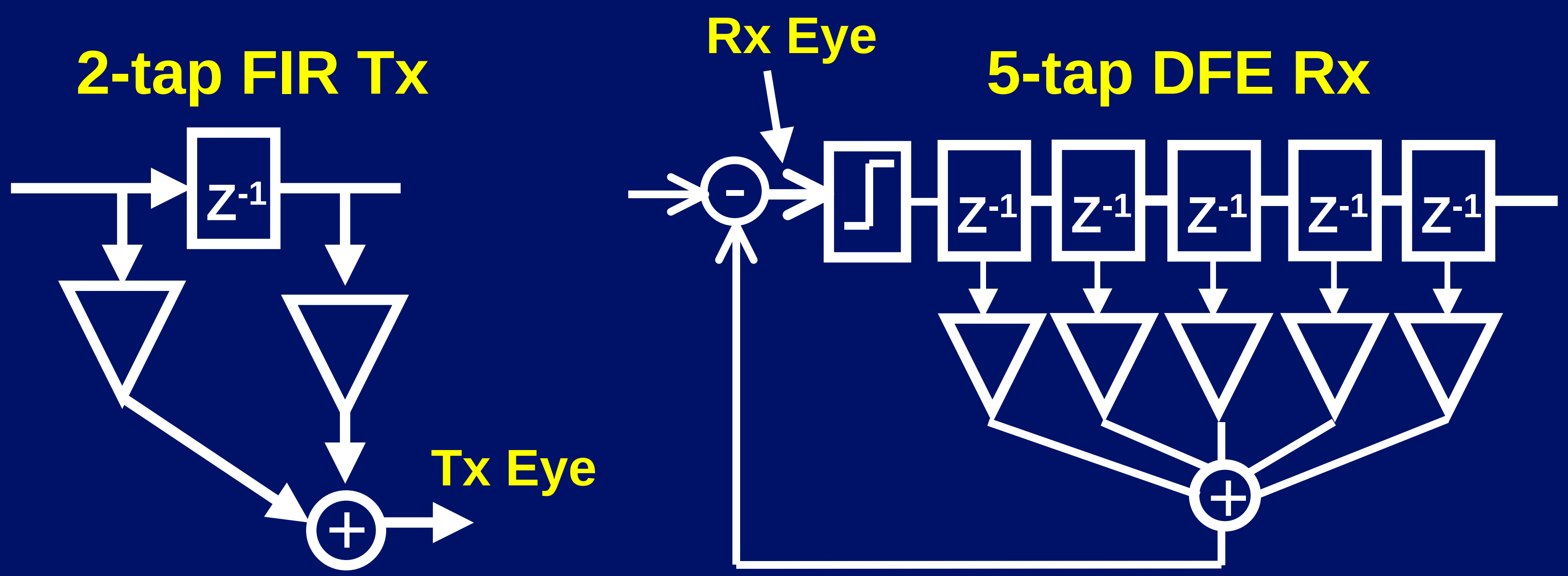
-Jitter, BER

**Does not specify:**

-Lane count, Pinout, Mgt interface,

-Power supply, Connector, High level functionality, protocol

# Rx and Tx Reference Models



# CEI 6G,11G Specific Requirements

- BER to be less than 1e-15
- Average transition density and average DC balance needs to converge to 0.5 over a long period (>$10^9$ bits) with a probability of at least one minus the BER ratio
- If a fixed block coding scheme is used (e.g. 8B/10B), the input data must be either scrambled before coding or the coded data must be scrambled prior to transmission
  - This will prevent input data creating “killer patterns” (e.g. CJPAT patterns)
- SONET/SDH can be viewed as a coding scheme that can create worst case patterns (via the un-encoded overhead bytes). Two such cases would be the A1/A2 pattern and the Z0 byte that can be anything (each unscrambled byte is repeated N times in an OC-N stream [N = 3, 12, 48, 192])
- For LR the eye is closed at the receiver, hence requiring receiver equalization

# CEI 6G,11G Specific Features

- Rather than specifying materials, channel components, or configurations, the CEI focuses on effective channel characteristics
  - Hence a short length of poorer material should be equivalent to a longer length of premium material. A ‘length’ is effectively defined in terms of its attenuation rather than its physical length

- Both driver and receiver lane-to-lane skew are each allowed up to 500ps. Higher layers must allow for this (1ns) skew as well as some PCB skew
- The ground difference between the driver and the receiver shall be within ±50mV for SR links and ±100mV for LR/MR links (i.e. 50mV per connector)

# OIF CEI Characteristics Summary

| Characteristic | CEI-6G-SR | CEI-6G-LR |
|---|---|---|
| Output differential voltage, mVppd | 400 min<br>750 max | 800 min<br>1200 max |
| Output Rise/Fall time, ps | > 30 | Same as 6G-SR |
| Output Total Jitter, UIpp@ BER=1e-15 | 0.3 | |
| Reference Tx equalizer, FIR | 2 tap<br>< 3dB | 2 tap<br>< 6dB |
| Reference Rx equalizer, DFE or FFE | Not present | 5 tap DFE |
| Rx differential input @ BER=1e-15:<br>Total Jitter, UIpp<br>Amplitude, mVppd | <br><br>< 0.6 (no SJ)<br>> 125 | After 5 tap DFE<br><br>< 0.6<br>>100 |

# BER script (PMC's StatEye ) Analysis Flow

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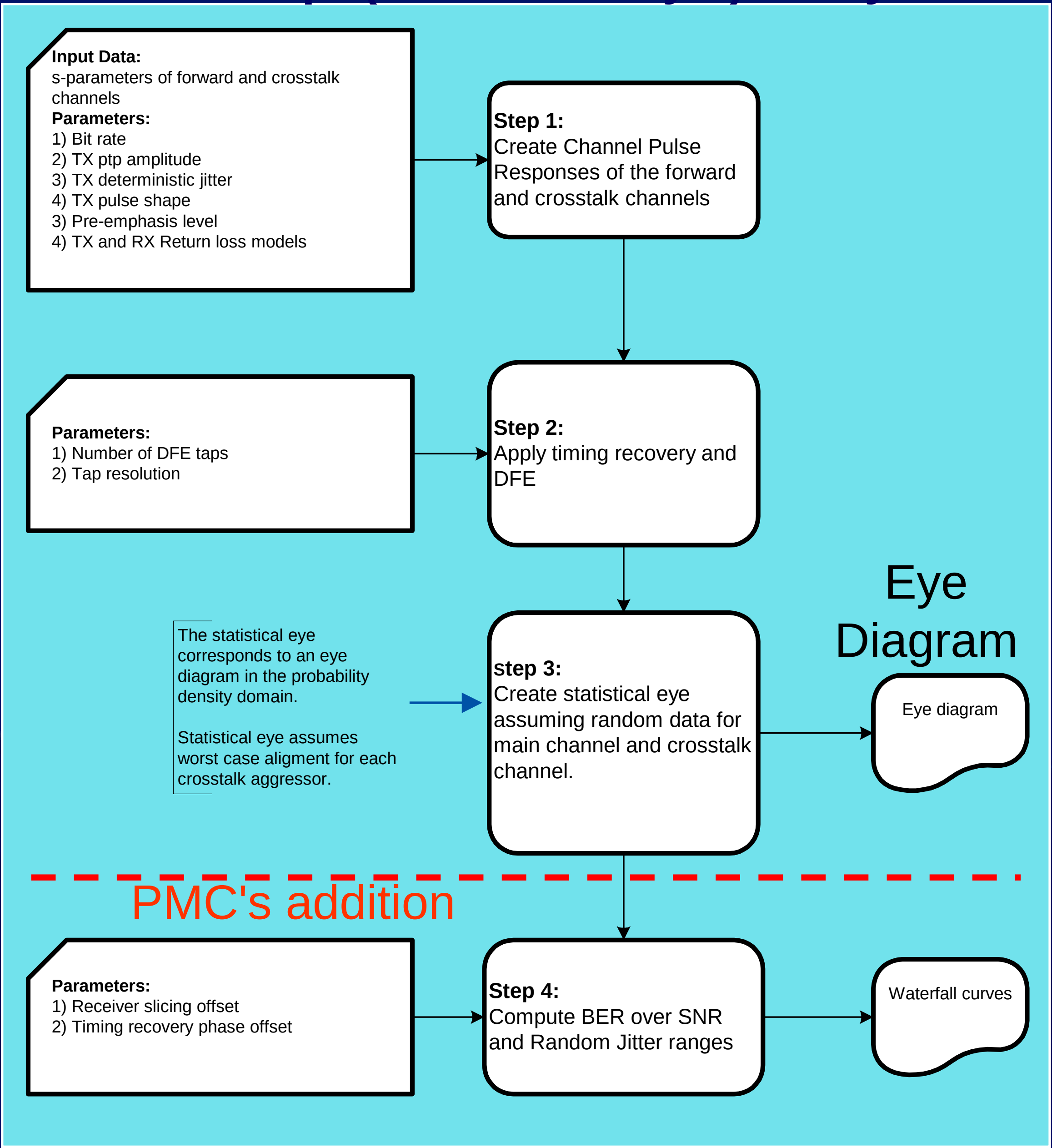
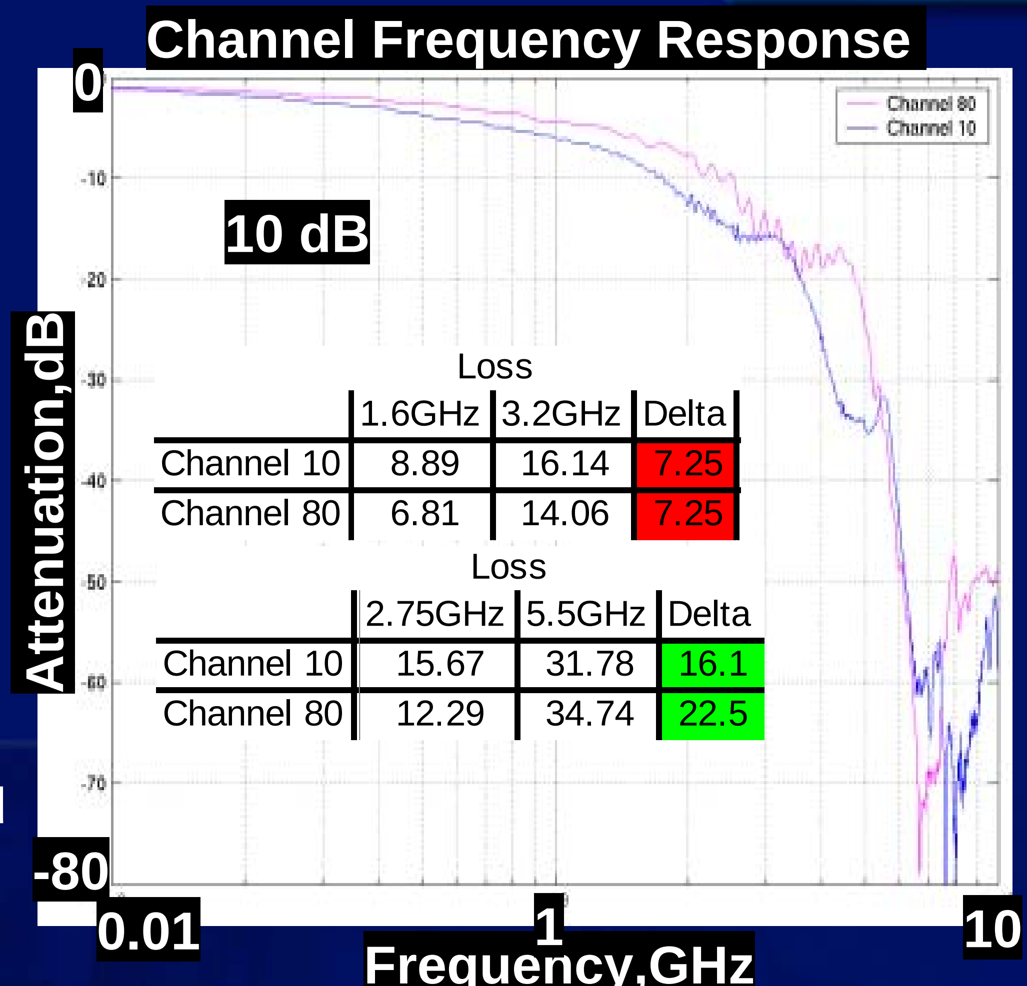



## BER Analysis considers lots of variables, Including:

- System variables (bit rate, coding)
- Channel S-parameters
- Cross-talk S-parameters
- Transmit parameters (Pre-emphasis, swing, etc.)
- Equalization configurations
- Clock recover unit parameters
- BER calculation parameters (thermal noise, slicer level, jitter, clock offset)

# Channel Examples

- PMC-Sierra has a library of over 180 measured channels from various sources
  - Varying connectors, material, trace geometry, lengths, etc
- Two arbitrary ones:
  - Channel 10 (30'' FR-4)
  - Channel 80 (24'' FR-4)
- Both channels contain 2 connectors and were designed for 2.5 to 3.125Gb/s rates



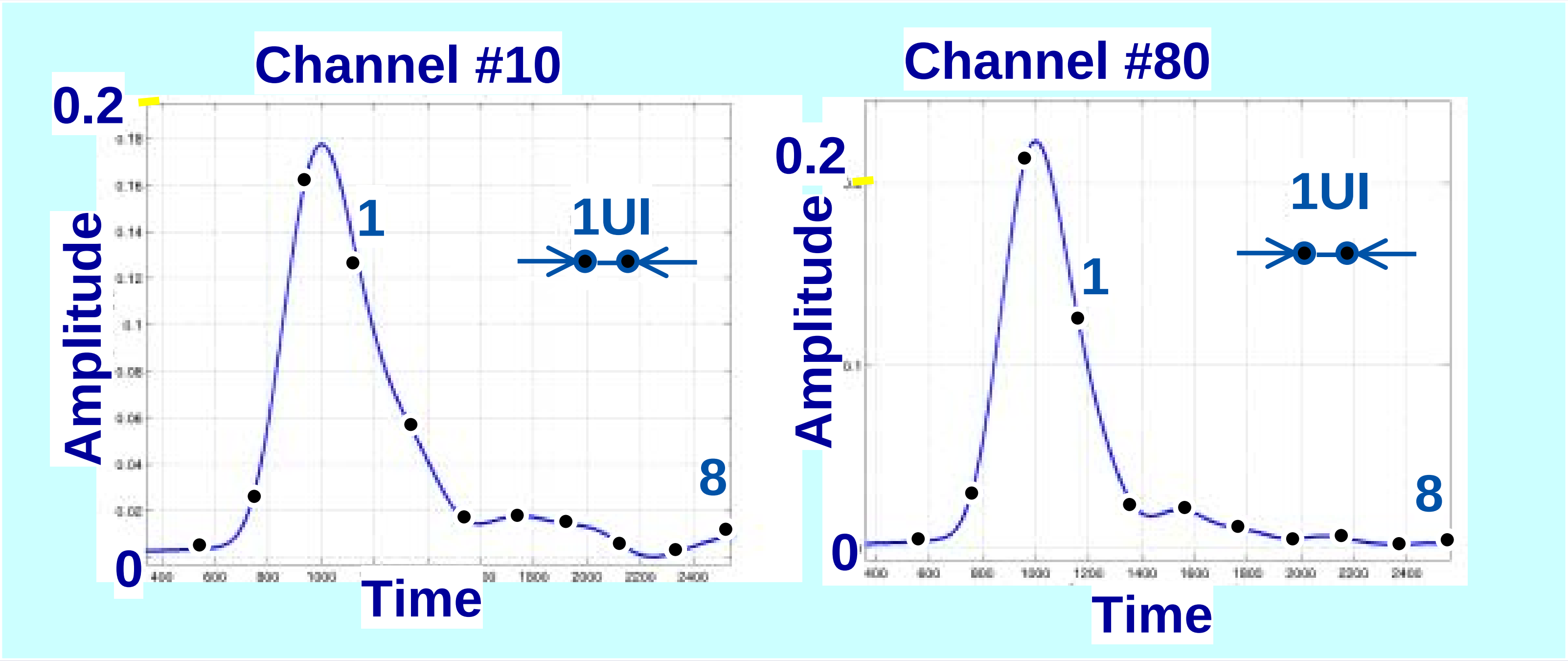

Loss

| | 1.6GHz | 3.2GHz | Delta |
|---|---|---|---|
| Channel 10 | 8.89 | 16.14 | 7.25 |
| Channel 80 | 6.81 | 14.06 | 7.25 |

Loss

| | 2.75GHz | 5.5GHz | Delta |
|---|---|---|---|
| Channel 10 | 15.67 | 31.78 | 16.1 |
| Channel 80 | 12.29 | 34.74 | 22.5 |

# Channels Pulse Response



# Simulations NRZ 6.375Gb/s, No Cross Talk, With Max CEI-6G Tx Jitter, Channel 10

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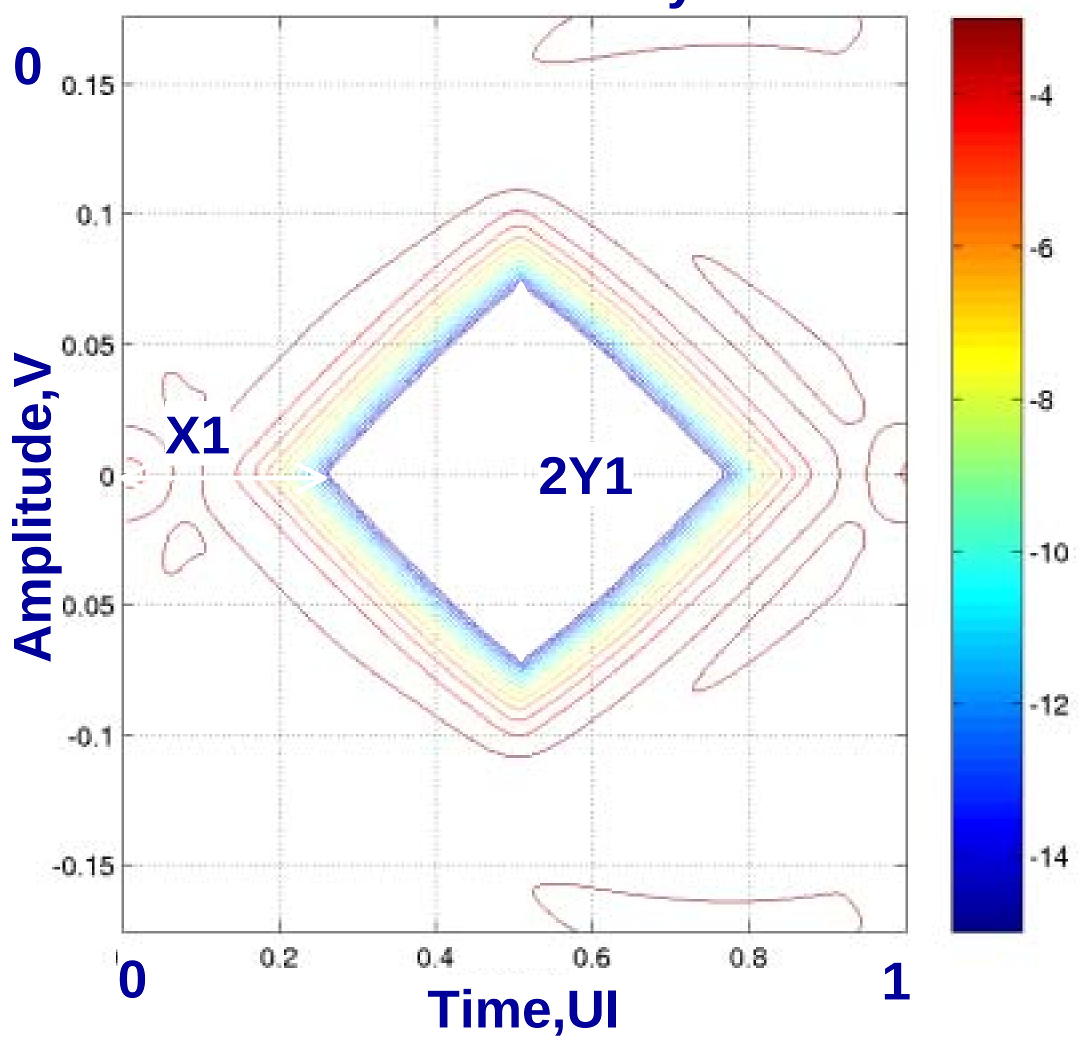
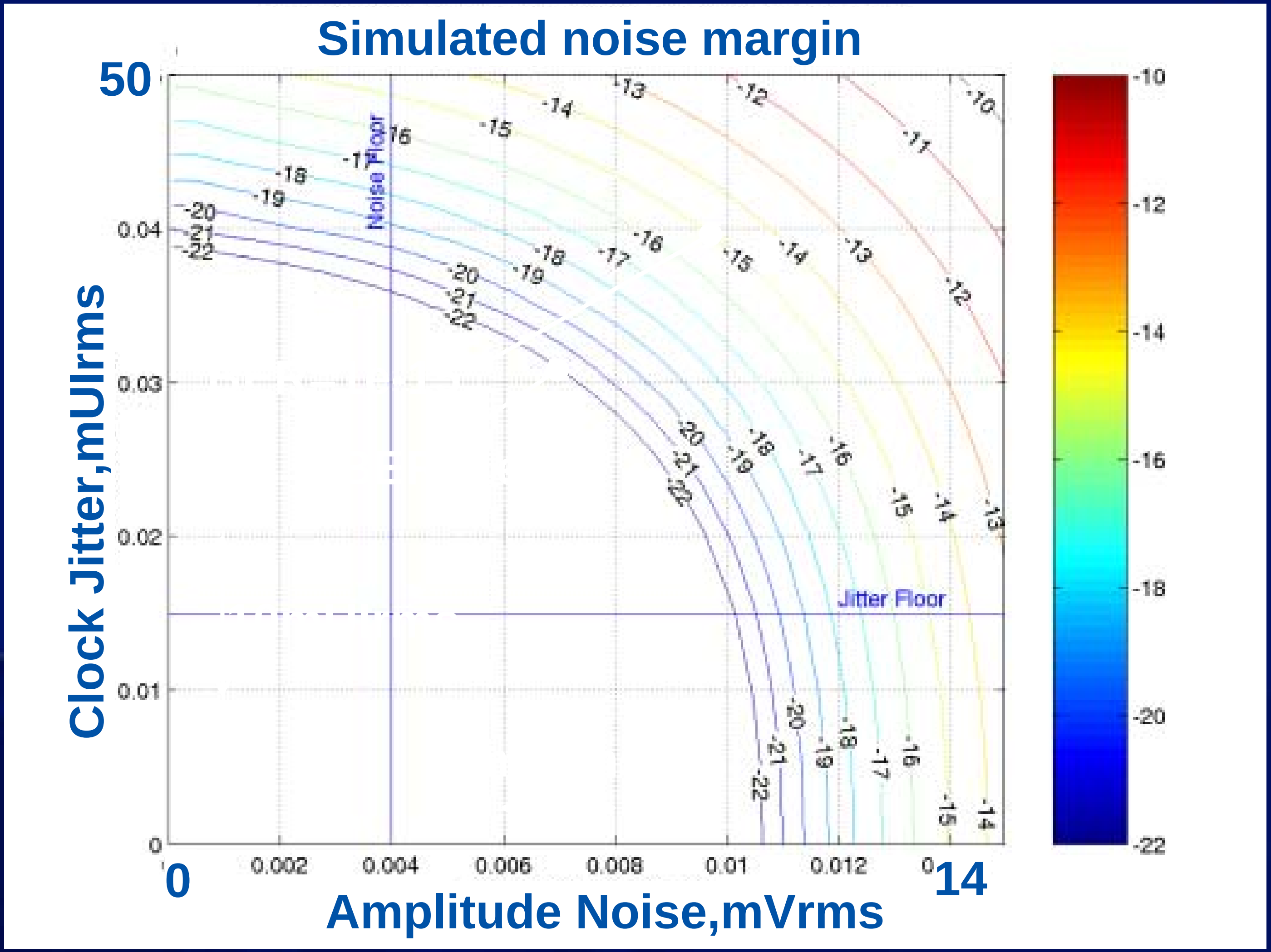
## Simulated Statistical Eye after DFE

Parameters:
Datatype: NRZ
Bit Rate: 6.375 Gbits/s
Channel Number: 10
Tx Taps: [ 1.00 ]
Tx Amp: 1.00Vppd
Traditional DFE
8 postC DFE Taps:
[ 0.1233 0.0552 0.0167 0.0171 0.0111 0.0089 0.0037 0.0045 ]
DAC Bits: floatingPoint
clk from optimal ISI point: -0.28
Tx DJ: 0.150UIpp
Tx RJ: 0.010UIrms




**@BER=1e-15**
**TJ= 0.49UIpp**
**2Y1 =145mV**

Simulations NRZ 6.375Gb/s, No Cross Talk, With Max CEI-6G Tx Jitter, Channel 10, Noise Margin



# CEI-6G extrapolation to SAS-2

| Characteristic | CEI-6G-LR | SAS -2 |
|---|---|---|
| Targeted technology node | 0.13um or lower | 90nm 0.13um |
| Interconnect | Backplane 2 connectors | Backplane 2 connectors Cable |
| TX Amplitude, mV | 800/1200 | 800/1200 1600 for SAS1.1? |
| BER | 1e-15 | 1e-15 ? |
| OOB | NO | YES@1.5Gb/s |
| Encoding | Allowable | 8b/10b ? |
| Scrambling | Required for BER | YES |
| Compliance points | IC component edge (pins) | TBD |
| Up channel | Not specified | TBD |

# SAS-2 First Effort Required Based on CEI-6G Experience (a silicon vendor view)

1. Make available to SAS-2 WG S-parameters for the interconnect modeling @ 6G with StatEye or with other tools
   - Must include crosstalk
2. Find an agreement on CEI-6G specification methodology, numbers and reference models
   - Reference Tx: 2 tap FIR
   - Reference Rx 5 tap DFE
   - Liaise with OIF on CEI specification (to pull parts of the doc)
3. Refine numbers based on SAS-2 interconnect specifics and variability

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