To: T10 Technical Committee
From: Rob Elliott, HP (elliott@hp.com)
Date: 6 November 2004
Subject: 04-370r0 SAS-1.1 Merge IT and IR with XT and XR

Revision history
Revision 0 (6 November 2004) First revision

Related documents
sas1r06 - Serial Attached SCSI 1.1 revision 6
04-337 SAS-1.1 TCTF editorial changes (Barry Olawsky, HP)

Overview
1. The XT/XR compliance points are currently used for both expanders and initiators that support being attached to SATA devices, while IT/IR are used for those that do not support being attached to SATA devices.

The only differences between XT/XR and IT/IR are:

a) clock frequency tolerance: +350/-5350 ppm (for spread-sprectrum support) at XR, +/-100 ppm at IR; and
b) minimum receiver eye voltage levels: 225 mV at XR, 325 mV at IR.

Every other number is the same. This results in a lot of duplicated numbers. For example, all the XR rows in the jitter tables are the same as the IR rows.

The XT/XR and IT/IR compliance points are proposed to be combined into a single set of IT/IR compliance points, with the differences for SATA drive support highlighted where necessary.

2. There is some confusion over where exactly the compliance points are located. Proposed figures are added showing the location of the compliance points for each type of connector interface.

3. SATA II defines numerous types of devices, including 3 Gbps devices:

c) 1i = 1.5 Gbps original SATA-1.0a spec for internal cables (transmit 400-600 mV; receive 325 mV).
d) 1m = 1.5 Gbps for hosts using “short” backplanes and external cables (requires the HBA transmit within a tighter range 500-600 mV, and requires that it receive a lower level of 240 mV).
e) 1x = 1.5 Gbps for external use and port selectors (bumps transmitter up to 1600 mV).
f) 2i = 3 Gbps for internal use (transmit 400-700 mV).
g) 2m = 3 Gbps for “short” backplanes and external cables (transmit 500-700 mV; receive 240 mV).
h) 2x = 3 Gbps for external use and port selectors (transmit 800-1600 mV; receive 275 mV).

SAS expanders and HBAs that support SATA devices should work with all of the above, including the most difficult 1i and 2i devices. The existing minimum receiver eye voltage level of 225 mV supports 1i devices.

A place for the minimum receive voltage level is proposed. The actual value is not proposed. A number needs to be determined that supports all types of 3 Gbps devices including 2i devices.

4. SATA II allows OOB signals to optionally be created from 1.5 Gbps D24.3 characters (0011 patterns) rather than ALIGN primitives (which have some lower frequency content due to the fact that ALIGN(0) contains K28.5).

Because of this, “ALIGN burst” needs to be renamed to avoid confusion. “OOB burst” is proposed. Chapter 5 currently uses “OOB ALIGN burst” so those simply reduce to “OOB burst”. Chapter 6 uses “ALIGN burst” on its own, so those change to “OOB burst.”

5. The internal cables/internal backplanes/external cables table should not specify common mode impedance for “mated connectors.” All the other specifications (media, receiver termination, transmitter source termination) are already made through mated connectors (per note b).

6. The internal wide cable needs to add “differential impedance imbalance,” as is already specified for the internal cables/internal backplanes/external cables.

7. Many table entries do not clearly state whether they are expressing a minimum or maximum value. Clarification is proposed where needed.

Suggested changes

5.3 Transmitter and receiver electrical characteristics

5.3.1 Compliance points

Signal behavior at separable connectors and ~~integrated circuit package connections that satisfy the description for a compliance point~~ require compliance with transmitter and receiver characteristics defined by this standard only if the connectors ~~or integrated circuit package connections~~ are identified as compliance points by the supplier of the parts that contain or comprise the candidate compliance point. Table 1 lists the compliance points.

Table 1 — Compliance points

Compliance point	Type	Description
IT	intra-enclosure	Transmitter, as measured through a mated Internal connector (i.e., SAS plug, SAS internal cable receptacle, SAS internal cable SATA-style signal cable receptacle, SAS backplane receptacle, or SAS internal wide cable receptacle)~~; transmit serial port~~
IR	intra-enclosure	Receiver, as measured through a mated Internal connector~~; receive serial port~~
CT	inter-enclosure	Transmitter, as measured through a mated External connector (i.e., SAS external cable plug, SAS external receptacle)~~; transmit serial port~~
CR	inter-enclosure	Receiver, as measured through a mated External connector~~; receive serial port~~
~~XT~~	~~intra-enclosure~~	~~Expander or SAS initiator phy; transmit serial port~~
~~XR~~	~~intra-enclosure~~	~~Expander or SAS initiator phy; receive serial port~~

[begin all-new portion]

Figure 1 shows the locations of the CT and CR compliance points using an external cable.

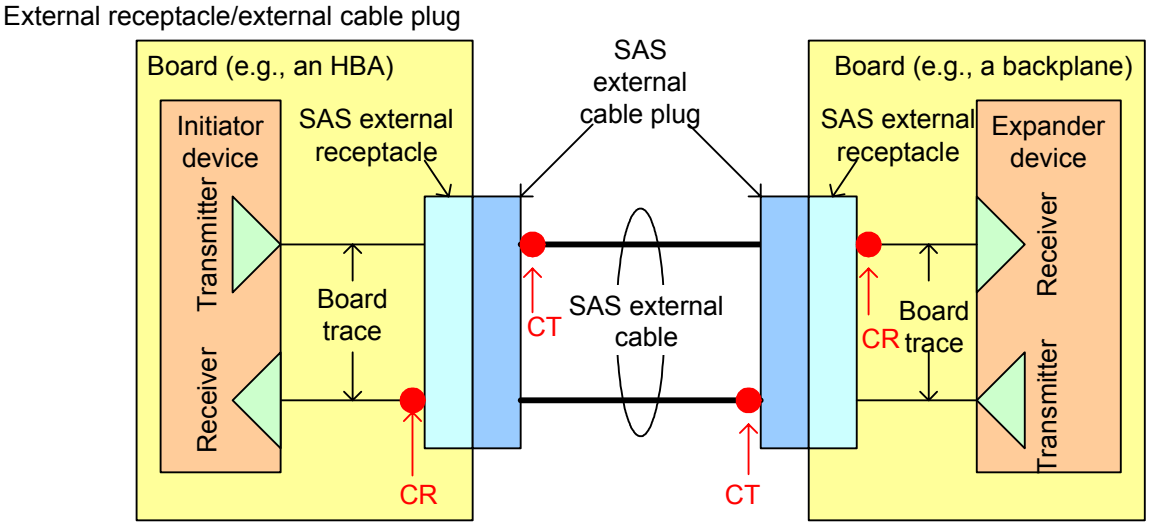

Figure 1 — External cable CT and CR compliance points

Figure 2 shows the locations of the IT and IR compliance points using a backplane with a SAS backplane receptacle (see 5.2.3.4) that is not attached to a SATA device.

Backplane receptacle/SAS plug

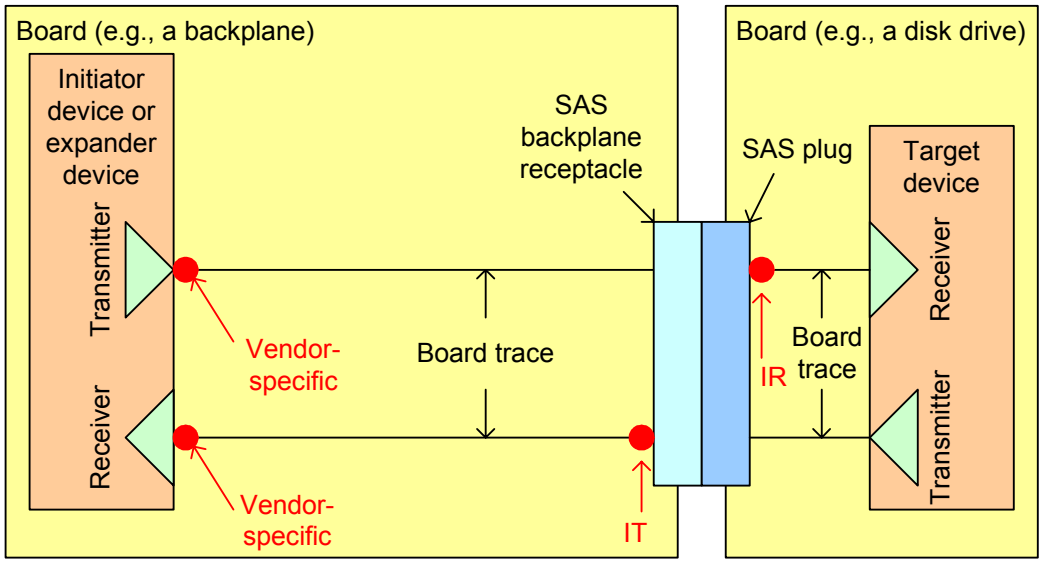

Figure 2 — Backplane IT and IR compliance points

If the backplane supports SATA devices being attached to the SAS backplane receptacle (see 5.2.3.4), there are no IT or IR compliance points. SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 3.

Backplane receptacle/SATA device plug

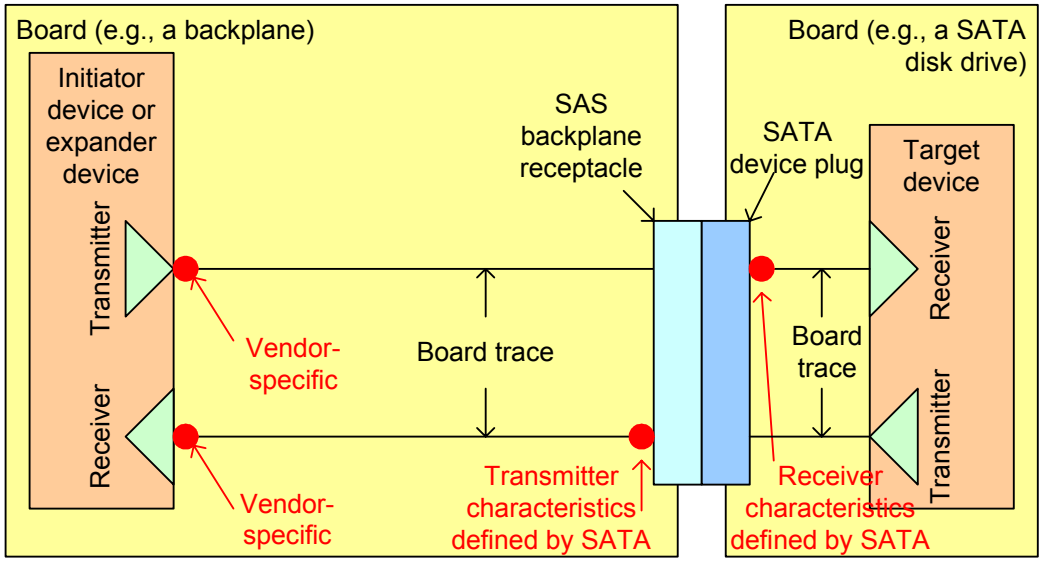

Figure 3 — Backplane compliance points with SATA device attached

Figure 4 shows the locations of the IT and IR compliance points using an internal wide cable.

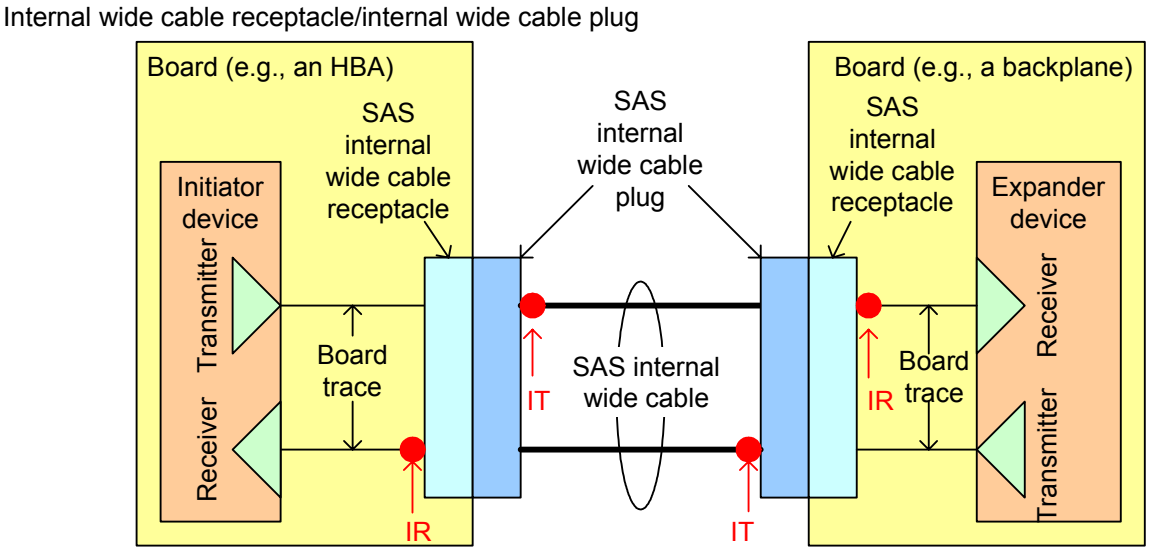

Figure 4 — Internal wide cable IT and IR compliance points

Figure 5 shows the locations of the IT and IR compliance points using an internal wide cable and a backplane, where the backplane is not attached to a SATA device.

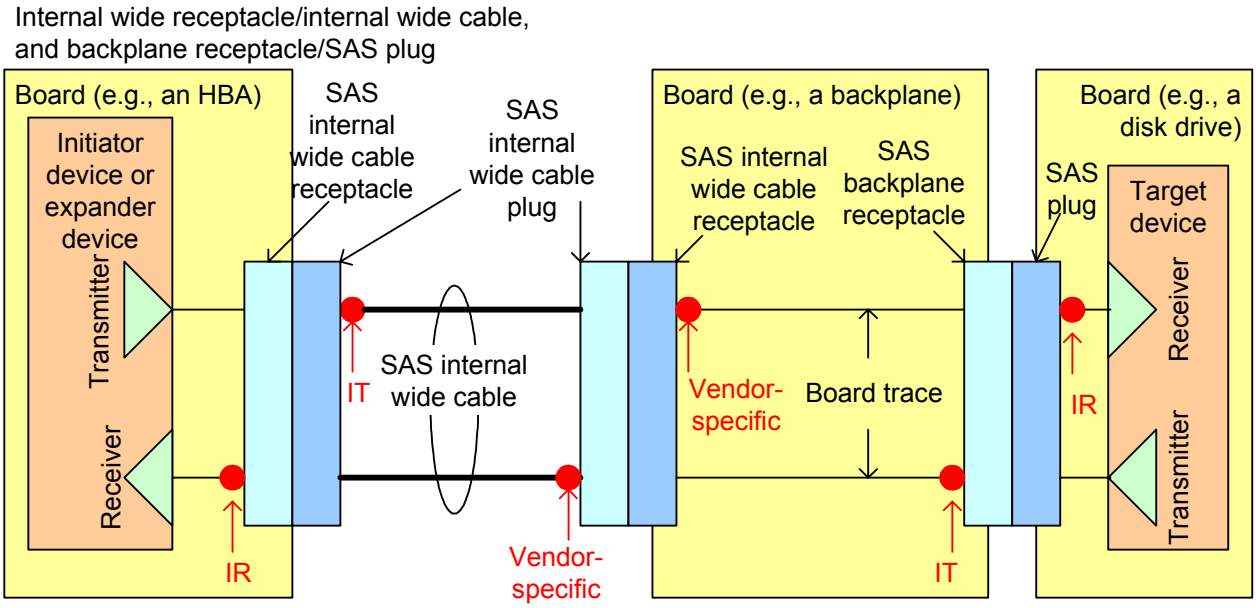

Figure 5 — Internal wide cable and backplane IT and IR compliance points

If the backplane supports SATA devices being attached to the SAS backplane receptacle, there are no IT and IR compliance points at that connector. SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 6.

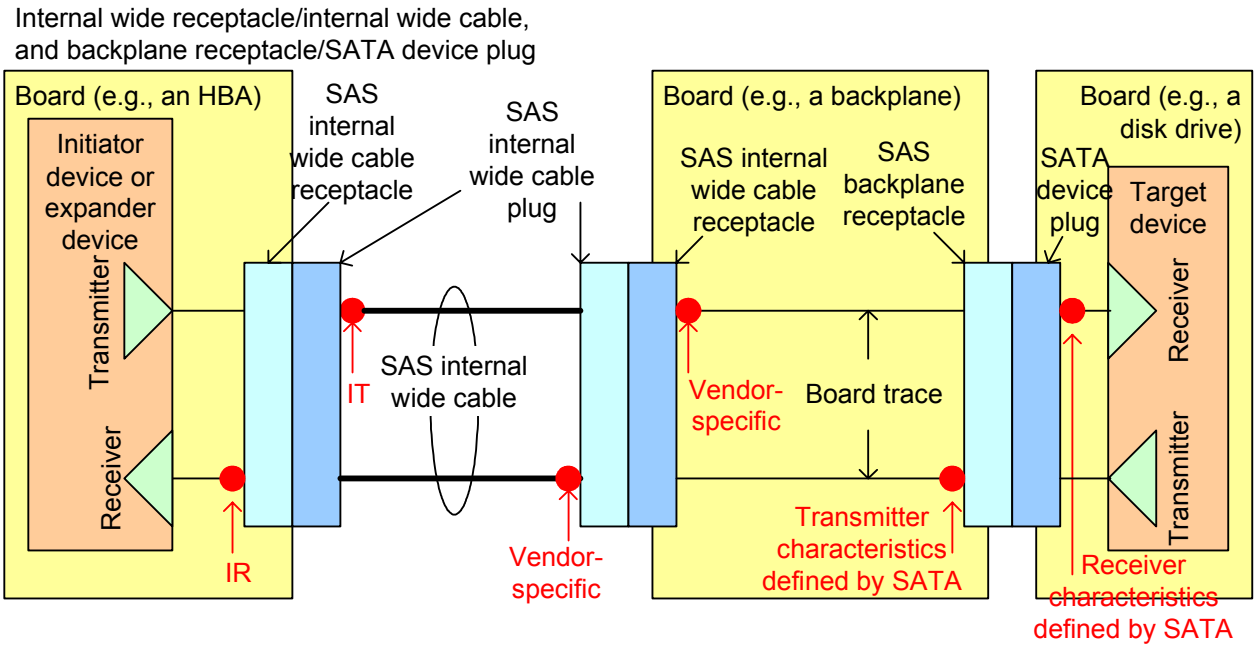

Figure 6 — Internal cable and backplane compliance points with SATA device attached

Figure 7 shows the locations of the IT and IR compliance points using an internal cable.

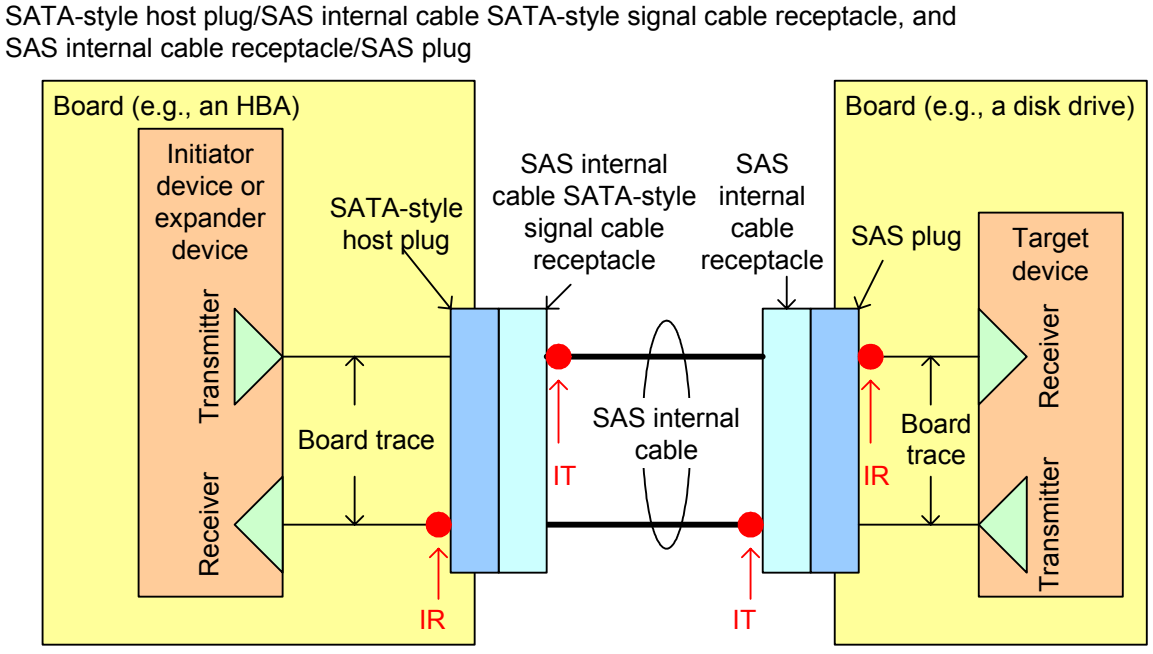

Figure 7 — Internal cable IT and IR compliance points

[end of all-new portion]

5.3.2 General interface specification

A TxRx connection is the complete simplex signal path between the output reference point of one phy or retimer to the input reference point of a second phy or retimer, over which a BER of < 10^{-12} is achieved.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in media.

This subclause defines the interfaces of the serial electrical signal at the compliance points IT, IR, CT, and CR~~, XT, and XR~~ in a TxRx connection. ~~The IT, IR, CT, and CR points are located at the connectors of a TxRx connection~~.

Each compliant phy shall be compatible with this serial electrical interface to allow interoperability within a SAS environment. All TxRx connections described in this subclause shall exceed the BER objective of 10^{-12}. The parameters specified in this section support meeting this requirement under all conditions including the minimum input and output amplitude levels.

For external cables, these signal specifications are consistent with using good quality passive cable assemblies constructed with shielded twinaxial cable with 24 gauge solid wire up to eight meters in length.

Figure 8 shows the transmitter transient test circuit.

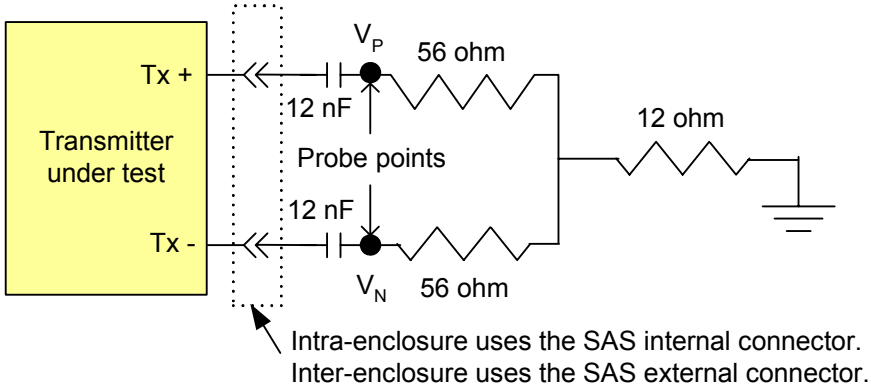

Figure 8 — Transmitter transient test circuit

Figure 9 shows the receiver transient test circuit.

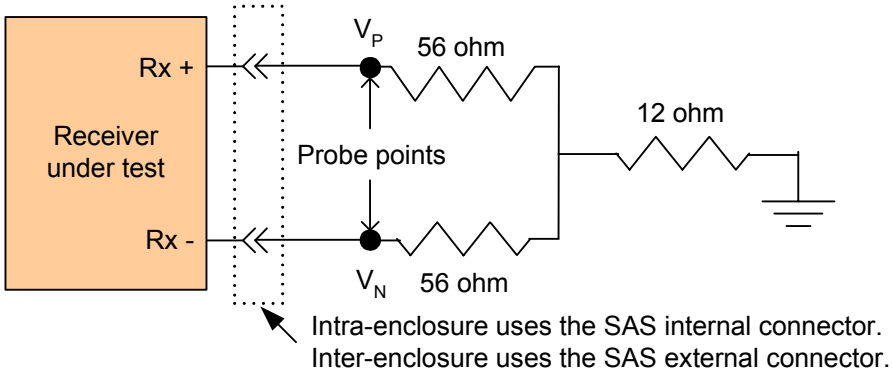

Figure 9 — Receiver transient test circuit

Table 2 defines the general interface characteristics.

Table 2 — General interface characteristics

Characteristic	Units	1,5 Gbps	3,0 Gbps
Physical link rate	MBps	150	300
Bit rate (nominal)	Mbaud	1 500	3 000
Unit interval (UI)(nominal)	ps	666,$\overline{6}$	333,$\overline{3}$
Physical link rate tolerance at ~~XR~~ [b] IR, if a SATA device is attached [b]	ppm	+350 / -5 350	
Physical link rate tolerance at IR if a SATA device is not attached and at CR	ppm	± 100	
Physical link rate tolerance at IT~~,~~ and CT, ~~and XT~~	ppm	± 100	
Media Impedance (nominal) [a]	ohm	100	
A.C. coupling capacitor, maximum [c]	nF	12	
Transmitter transients, maximum [d]	V	± 1,2	
Receiver transients, maximum [d]	V	± 1,2	
Receiver A.C. common mode voltage tolerance V_{CM}, minimum [e]	mV(P-P)	150	
Receiver A.C. common mode frequency tolerance range F_{CM} [e]	MHz	2 to 200	

[a] The media impedances are the differential impedances.
[b] Allows support for SATA devices with spread spectrum clocking (see ATA/ATAPI-7 V3). ~~SAS initiator phys supporting being attached to SATA devices should also use these tolerances.~~
[c] The coupling capacitor value for A.C. coupled transmit and receive pairs.
[d] The maximum transmitter and receiver transients are measured at nodes V_P and V_N on the test loads shown in figure 8 (for the transmitter) and figure 9 (for the receiver) during all power state and mode transitions. Test conditions shall include the system power supply ramping at the fastest possible rate for both power on and power off conditions.
[e] Receivers shall tolerate sinusoidal common mode noise components within the peak-to-peak amplitude (V_{CM}) and the frequency range (F_{CM}).

Editor's Note 1: in all tables in this proposal, joined the 1.5 and 3.0 Gbps cells together if they have the same value. This helps highlight the differences.

5.3.3 Eye masks

5.3.3.1 Eye masks overview

The eye masks shown in this subclause shall be interpreted as graphical representations of the voltage and time limits on the signal at the compliance point. The time values between X1 and (1 - X1) cover all but 10^{-12} of the jitter population. The random content of the total jitter population has a range of ± 7 standard deviations.

5.3.3.2 Receive eye mask at IR~~,~~ and CR~~, and XR~~

Figure 10 describes the receive eye mask. This eye mask applies to jitter after the application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).

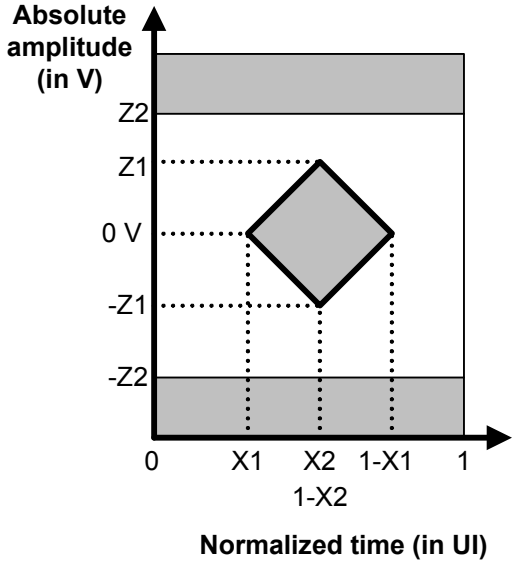

Figure 10 — Eye mask at IR~~,~~ and CR~~, and XR~~

Verifying compliance with the limits represented by the receive eye mask should be done with reverse channel traffic present in order that the effects of crosstalk are taken into account.

5.3.3.3 Jitter tolerance masks

Figure 11 describes the receive tolerance eye masks at IR~~,~~ and CR~~, and XR~~ and shall be constructed using the X2 and Z2 values given in table 4. $X1_{OP}$ shall be half the value for total jitter in table 5 and $X1_{TOL}$ shall be half the value for total jitter in table 6, for jitter frequencies above ((bit rate) / 1 667).

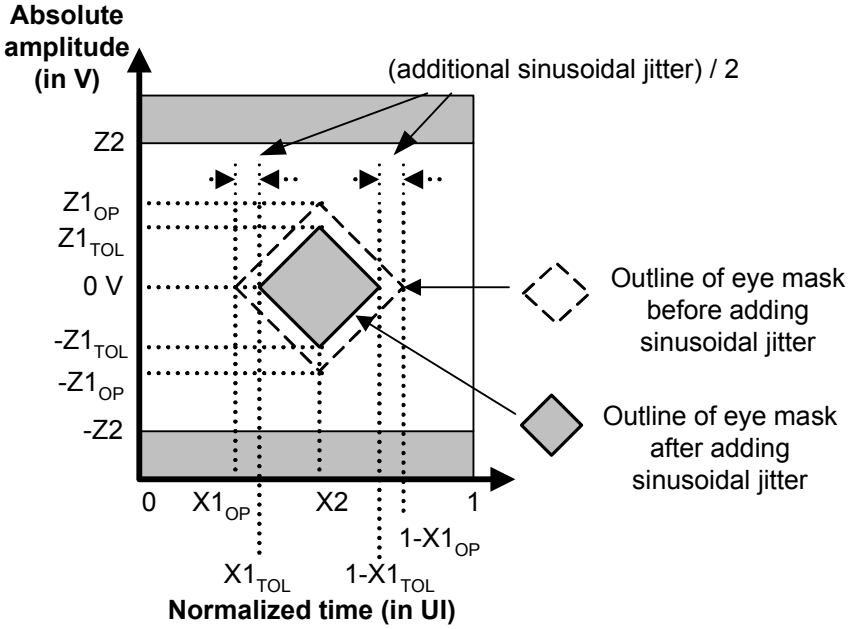

Figure 11 — Deriving a tolerance mask at IR~~,~~ and CR~~, or XR~~

The leading and trailing edge slopes of figure 10 shall be preserved. As a result the amplitude value of Z1 is less than that given in table 4 and $Z1_{TOL}$ and $Z1_{OP}$ shall be defined from those slopes by the following equation:

$$Z1_{TOL} = Z1_{OP} \times \frac{X2_{OP} - (0,5 \times \text{additional sinusoidal jitter}) - X1_{OP}}{X2_{OP} - X1_{OP}}$$

where:

a) $Z1_{TOL}$ is the value for Z1 to be used for the tolerance masks; and
b) $Z1_{OP}$, $X1_{OP}$, and $X2_{OP}$ are the values in table 4 for Z1, X1, and X2.

The X1 points in the receive tolerance masks are greater than the X1 points in the receive masks, due to the addition of sinusoidal jitter.

Figure 12 defines the sinusoidal jitter mask.

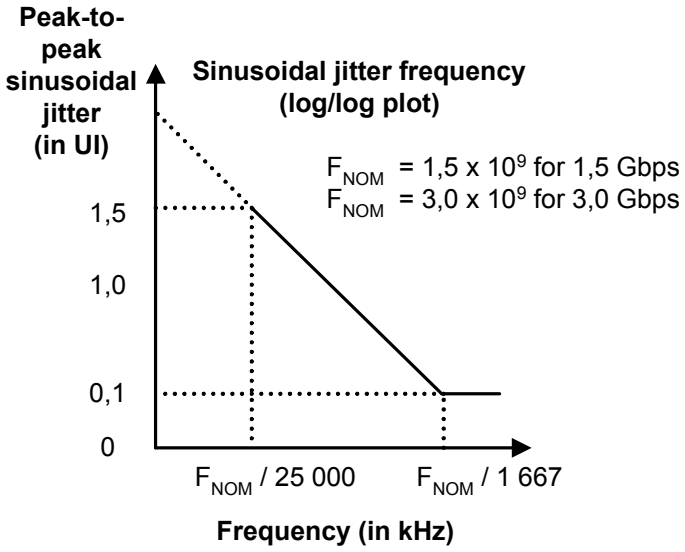

Figure 12 — Sinusoidal jitter mask

5.3.4 Signal characteristics at IT,and CT, ~~and XT~~

This subclause defines the inter-operability requirements of the signal at the transmitter end of a TxRx connection as measured into the zero-length test load specified in figure 14. All specifications are based on differential measurements.

Expander phys supporting being attached to SATA devices shall use SATA 1.0 signal levels (see ATA/ATAPI-7 V3) during the first OOB sequence after a power on or hard reset if the 1,5 Gbps transfer rate is supported. As soon as COMSAS has been exchanged, the expander phy shall increase its transmit levels to the SAS voltage levels specified in table 4. If a COMINIT is not received within a hot-plug timeout at SATA 1.0 signal levels, the expander phy shall increase its transmit levels to the SAS voltage levels and perform the OOB sequence again. If no COMINIT is received within a hot-plug timeout of the second OOB sequence the expander phy shall initiate another OOB sequence using SATA 1.0 signal levels. The expander phy shall continue alternating between sending COMINIT at SATA 1.0 signal levels and SAS signal levels until a COMINIT is received.

If the OOB sequence is completed at the SAS voltage level and a SATA device is detected rather than a SAS target device, the expander phy shall switch to SATA 1.0 voltage levels and repeat the OOB sequence.

NOTE 1 - SAS initiator phys supporting being attached to SATA devices may use the same algorithm as expander phys.

SAS initiator phys and SAS target phys shall transmit OOB signals using SAS signal levels.

Table 3 specifies the signal characteristics at IT~~,~~ and CT~~XT, and XT~~.

Table 3 — Signal characteristics at IT~~,~~and CT~~, XT~~

Compliance point	Signal characteristic [a]	Units	1,5 Gbps	3,0 Gbps
IT, CT~~, XT~~	Maximum skew [b]	ps	20	15
	Tx Off Voltage [c]	mV(P-P)	< 50	
	Maximum rise/fall time [d]	ps	273	137
	Minimum rise/fall time [d]	ps	67	
	Maximum transmitter output imbalance [e]	%	10	
	OOB offset delta [f]	mV	± 25	
	OOB common mode delta [g]	mV	± 50	

[a] All tests in this table shall be performed with zero-length test load shown in figure 14.
[b] The skew measurement shall be made at the midpoint of the transition with a repeating 0101b pattern on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Tx+ and Tx- signals. Skew is defined as the time difference between the means of the midpoint crossing times of the Tx+ signal and the Tx- signal.
[c] The transmitter off voltage is the maximum A.C. voltage measured at compliance points IT~~,~~and CT~~, and XT~~ when the transmitter is unpowered or transmitting D.C. idle (e.g., during idle time of an OOB signal).
[d] Rise/fall times are measured from 20 % to 80 % of the transition with a repeating 0101b pattern on the physical link.
[e] The maximum difference between the V+ and V- A.C. RMS transmitter amplitudes measured with CJTPAT (see 5.3.8) into the test load shown in figure 14, as a percentage of the average of the V+ and V- A.C. RMS amplitudes.
[f] The maximum difference in the average differential voltage (D.C. offset) component between the burst times and the idle times of an OOB signal.
[g] The maximum difference in the average of the common mode voltage between the burst times and the idle times of an OOB signal.

5.3.5 Signal characteristics at IR~~,~~ and CR~~, and XR~~

Table 4 defines the compliance point requirements of the signal at the receiver end of a TxRx connection as measured into the test loads specified in figure 13 and figure 14.

Table 4 — Signal characteristics at IR~~,~~ and CR~~, and XR~~ (part 1 of 2)

Compliance point	Signal characteristic	Units	~~SATA~~	1,5 Gbps	3,0 Gbps
IR~~e~~	Jitter (see figure 10) [b]	N/A	~~N/A~~	See table 5	See table 5
	Maximum 2 x Z2	mV(P-P)	~~N/A~~	1 600	
	Minimum 2 x Z1, if a SATA device is not attached	mV(P-P)	~~N/A~~	325	275
	Minimum 2 x Z1, if a SATA device is attached	mV(P-P)	~~N/A~~	225	TBD
	Maximum X1 [a]	UI	~~N/A~~	0,275	
	X2	UI	~~N/A~~	0,50	
	Maximum Skew [d]	ps	~~N/A~~	80	75
	Maximum voltage (non-operational)	mV(P-P)	~~N/A~~	2 000	
	Minimum OOB ~~ALIGN~~ burst amplitude [c], if attaching a SATA device is not supported	mV(P-P)	~~N/A~~	240 [g]	
	Minimum OOB ~~ALIGN~~ burst amplitude [c], if attaching a SATA device is supported	mV(P-P)	~~N/A~~	225 [g]	225 [h]
	Maximum noise during OOB idle time [c]	mV(P-P)	~~N/A~~	120	
	Maximum near-end crosstalk [f]	mV(P-P)	~~N/A~~	100	
CR	Jitter (see figure 10) [b]	N/A	~~N/A~~	See table 5	See table 5
	Maximum 2 x Z2	mV(P-P)	~~N/A~~	1 600	
	Minimum 2 x Z1	mV(P-P)	~~N/A~~	275	
	Maximum X1 [a]	UI	~~N/A~~	0,275	
	X2	UI	~~N/A~~	0,50	
	Maximum Skew [d]	ps	~~N/A~~	80	75
	Maximum voltage (non-operational)	mV(P-P)	~~N/A~~	2 000	
	Minimum OOB ~~ALIGN~~ burst amplitude [c]	mV(P-P)	~~N/A~~	240 [g]	
	Maximum noise during OOB idle time [c]	mV(P-P)	~~N/A~~	120	
	Maximum near-end crosstalk [f]	mV(P-P)	~~N/A~~	100	

Table 4 — Signal characteristics at IR~~,~~ and CR~~, and XR~~ (part 2 of 2)

Compliance point	Signal characteristic	Units	~~SATA~~	1,5 Gbps	3,0 Gbps
~~XR~~	~~Jitter (see figure 10)~~ [b]	~~N/A~~	~~See table 5~~	~~See table 5~~	~~See table 5~~
	~~2 x Z2~~	~~mV(P-P)~~	~~1 600~~	~~1 600~~	~~1 600~~
	~~2 x Z1~~	~~mV(P-P)~~	~~225~~	~~325~~	~~275~~
	~~X1~~ [a]	~~UI~~	~~0,275~~	~~0,275~~	~~0,275~~
	~~X2~~	~~UI~~	~~0,50~~	~~0,50~~	~~0,50~~
	~~Skew~~ [d]	~~ps~~	~~50~~	~~80~~	~~75~~
	~~Max voltage (non-op)~~	~~mV(P-P)~~	~~2 000~~	~~2 000~~	~~2 000~~
	~~Minimum OOB ALIGN burst amplitude~~ [c]	~~mV(P-P)~~	~~240~~	~~240~~	~~240~~
	~~Maximum noise during OOB idle time~~ [c]	~~mV(P-P)~~	~~120~~	~~120~~	~~120~~
	~~Max near-end crosstalk~~ [f]	~~mV(P-P)~~	~~100~~	~~100~~	~~100~~

[a] The value for X1 shall be half the value given for total jitter in table 5. The test or analysis shall include the effects of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).

[b] The value for X1 applies at a total jitter probability of 10^{-12}. At this level of probability direct visual comparison between the mask and actual signals is not a valid method for determining compliance with the jitter output requirements.

[c] With a measurement bandwidth of 1,5 times the baud rate (i.e., 4,5 GHz for 3,0 Gbps).

[d] The skew measurement shall be made at the midpoint of the transition with a repeating 0101b pattern on the physical link. The same stable trigger, coherent to the data stream, shall be used for both the Rx+ and Rx- signals. Skew is defined as the time difference between the means of the midpoint crossing times of the Rx+ signal and the Rx- signal.

[e] ~~If being attached to SATA devices is supported at the IR location, requirements of SATA shall be met at IR.~~

[f] Near-end crosstalk is the unwanted signal amplitude at receiver terminals IR~~,~~and CR~~, and XR~~ coupled from signals and noise sources other than the desired signal. Refer to SFF-8410.

[g] The burst portion of the OOB signal is comprised of either 1,5 Gbps ALIGN (0) dwords or 3,0 Gbps ALIGN (0) dwords (see 6.6).

[h] The burst portion of the OOB signal is comprised of either 1,5 Gbps D24.3 characters, 1,5 Gbps ALIGN (0) dwords, or 3,0 Gbps ALIGN (0) dwords (see SATA-2).

For IR compliance points at the SATA

5.3.6 Jitter

Table 5 defines the maximum allowable jitter at IR~~,~~ and CR~~, and XR~~.

Table 5 — Maximum allowable jitter at IR~~,~~ and CR~~, XR~~

Compliance point	1,5 Gbps [a, b]		3,0 Gbps [a, b]	
	Deterministic jitter [e]	Total jitter [c, d, e, f]	Deterministic jitter [e]	Total jitter [c, d, e, f]
IR	0,35	0,55	0,35	0,55
CR	0,35	0,55	0,35	0,55
~~XR~~	~~0,35~~	~~0,55~~	~~0,35~~	~~0,55~~

[a] Units are in UI.
[b] The values for jitter in this section are measured at the average amplitude point.
[c] Total jitter is the sum of deterministic jitter and random jitter. If the actual deterministic jitter is less than the maximum specified, then the random jitter may increase as long as the total jitter does not exceed the specified maximum total jitter.
[d] Total jitter is specified at a probability of 10^{-12}.
[e] The deterministic and total values in this table apply to jitter after application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).
[f] If total jitter received at any point is less than the maximum allowed, then the jitter distribution of the signals is allowed to be asymmetric. The total jitter plus the magnitude of the asymmetry shall not exceed the allowed maximum total jitter. The numerical difference between the average of the peaks with a BER < 10^{-12} and the average of the individual events is the measure of the asymmetry. Jitter peak-to-peak measured < (maximum total jitter - |Asymmetry|).

5.3.7 Receiver jitter tolerance

Table 6 defines the amount of jitter the receiver shall tolerate at IR~~,~~and CR~~, and XR~~.

Table 6 — Receiver jitter tolerance

Compliance point	1,5 Gbps [a]			3,0 Gbps [a]		
	Sinusoidal jitter [b, c]	Deterministic jitter [e, f, h]	Total jitter [h]	Sinusoidal jitter [b, d]	Deterministic jitter [e, g, h]	Total jitter [h]
IR	0,10	0,35	0,65	0,10	0,35	0,65
CR	0,10	0,35	0,65	0,10	0,35	0,65
~~XR~~	~~0,10~~	~~0,35~~	~~0,65~~	~~0,10~~	~~0,35~~	~~0,65~~

[a] Units are in UI.
[b] The jitter values given are normative for a combination of deterministic jitter, random jitter, and sinusoidal jitter that receivers shall be able to tolerate without exceeding a BER of 10^{-12}. Receivers shall tolerate sinusoidal jitter of progressively greater amplitude at lower frequencies, according to the mask in figure 12 with the same deterministic jitter and random jitter levels as were used in the high frequency sweep.
[c] Sinusoidal swept frequency: 900 kHz to > 5 MHz.
[d] Sinusoidal swept frequency: 1 800 kHz to > 5 MHz.
[e] No value is given for random jitter. For compliance with this standard, the actual random jitter amplitude shall be the value that brings total jitter to the stated value at a probability of 10^{-12}. The additional 0,1 UI of sinusoidal jitter is added to ensure the receiver has sufficient operating margin in the presence of external interference.
[f] Deterministic jitter: 900 kHz to 750 MHz.
[g] Deterministic jitter: 1 800 kHz to 1 500 MHz.
[h] The deterministic and total values in this table apply to jitter after application of a single pole high-pass frequency-weighting function that progressively attenuates jitter at 20 dB/decade below a frequency of ((bit rate) / 1 667).

5.3.8 Jitter test pattern

The CJTPAT shall be used for all jitter testing unless otherwise specified. Annex A defines the required pattern on the physical link and provides information regarding special considerations for scrambling and running disparity.

5.3.9 Impedance and media specifications

Table 7 defines impedance and media requirements for internal cables, internal backplanes, and external cables.

Table 7 — Impedance and media req's for internal cables, internal backplanes, and external cables
(part 1 of 2)

Requirement	Units	1,5 Gbps	3,0 Gbps
Maximum Time domain reflectometer rise time 20 % to 80 % [a, b]	ps	100	50
Media (Backplane or cable)			
Differential impedance [b, c, d]	ohm	100 ± 10	
Maximum Differential impedance imbalance [b, c, d, g]	ohm	5	
Common mode impedance [b, c, d]	ohm	32,5 ± 7,5	
Mated connectors			
Differential impedance [b, c, d]	ohm	100 ± 15	

Table 7 — Impedance and media req's for internal cables, internal backplanes, and external cables
(part 2 of 2)

Requirement	Units	1,5 Gbps	3,0 Gbps
Differential impedance imbalance [b, c, d, g]	ohm	5	
~~Common mode impedance [b, c, d]~~	~~ohm~~	~~32,5 ± 7,5~~	
Receiver termination			
Differential impedance [b, e, f]	ohm	100 ± 15	
Maximum Differential impedance imbalance [b, e, f, g]	ohm	5	
Receiver termination time constant [b, e, f]	ps	150 max	100 max
Common mode impedance [b, e]	ohm	20 min/40 max	
Transmitter source termination			
Differential impedance [b]	ohm	60 min/115 max	
Maximum Differential impedance imbalance [b, g]	ohm	5	
Common mode impedance [b]	ohm	15 min/40 max	

[a] All times indicated for time domain reflectometer measurements are recorded times. Recorded times are twice the transit time of the time domain reflectometer signal.

[b] All measurements are made through mated connector pairs.

[c] The media impedance measurement identifies the impedance mismatches present in the media when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the media, when present, but includes any intermediate connectors or splices. The mated connectors measurement applies only to the mated connector pair at each end, as applicable.

[d] Where the media has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[e] The receiver termination impedance specification applies to all receivers in a TxRx connection and covers all time points between the connector nearest the receiver, the receiver, and the transmission line terminator. This measurement shall be made from that connector.

[f] At the time point corresponding to the connection of the receiver to the transmission line the input capacitance of the receiver and its connection to the transmission line may cause the measured impedance to fall below the minimum impedances specified in this table. The area of the impedance dip (amplitude as ρ, the reflection coefficient, and duration in time) caused by this capacitance is the receiver termination time constant. The receiver time constant shall not be greater than the values shown in this table. An approximate value for the receiver termination time constant is given by the product of the amplitude of the dip (as ρ) and its width (in ps) measured at the half amplitude point. The amplitude is defined as being the difference in the reflection coefficient between the reflection coefficient at the nominal impedance and the reflection coefficient at the minimum impedance point. The value of the receiver excess input capacitance is given by the following equation:

$$C = \frac{\text{receiver termination time constant}}{(R0 \parallel RR)}$$

where (R0 || RR) is the parallel combination of the transmission line characteristic impedance and termination resistance at the receiver.

[g] The difference in measured impedance to ground on the plus and minus terminals on the interconnect, transmitter or receiver, with a differential test signal applied to those terminals.

Editor's Note 2: in table 7, propose removing "Common mode impedance" in the mated connectors section, as it should only apply to media

Table 8 defines impedance and media requirements for internal wide cables.

Table 8 — Impedance and media requirements for internal wide cable

Requirement	Units	1,5 Gbps	3,0 Gbps
Maximum time domain reflectometer rise time 20 % to 80 % [a, b]	ps	70	
Media (cable)			
Differential impedance [b, c, d]	ohm	100 ± 10	
Maximum Differential impedance imbalance [b, c, d, e]	ohm	5	
Common mode impedance [b, c, d]	ohm	32,5 ± 7,5	
Mated connectors			
Differential impedance [b, c, d]	ohm	100 ± 15	
Maximum differential impedance imbalance [b, c, d, g]	ohm	5	
Mated connector assembly			
Maximum insertion loss [b, c, d]	dB	6	
Maximum near-end crosstalk on the following (adjacent) signal pairs: RX0/TX0, TX0/RX1, RX1/TX1, RX2/TX2, TX2/RX3, and RX3/TX3 [b, f, g]	dB	-33	
Maximum near-end crosstalk on the following signal pairs: RX0/RX1, RX0/TX1, TX0/TX1, RX2/RX3, RX2/TX3, and TX2/TX3 [b, f, g]	dB	-45	
Maximum near-end crosstalk on all other signal pairs [b, f, g]	dB	-50	
Maximum intra-pair skew [b]	ps	10	

[a] Filtering may be used to obtain the equivalent rise time. The filter consists of the two-way launch/return path of the test fixturing, the two-way launch/return path of the test cable, and the software or hardware filtering of the time domain reflectometer scope. The equivalent rise time is the rise time of the time domain reflectometer scope output after application of all filter components. When configuring software or hardware filters of the time domain reflectometer scope to obtain the equivalent rise time, filtering effects of test cables and test fixturing shall be included.

[b] All measurements are made through mated connector pairs.

[c] The media impedance measurement identifies the impedance mismatches present in the media when terminated in its characteristic impedance. This measurement excludes mated connectors at both ends of the media, when present, but includes any intermediate connectors or splices. The mated connectors measurement applies only to the mated connector pair at each end, as applicable.

[d] Where the media has an electrical length of > 4 ns the procedure detailed in SFF-8410, or an equivalent procedure, shall be used to determine the impedance.

[e] The difference in measured impedance to ground on the plus and minus terminals on the interconnect, transmitter or receiver, with a differential test signal applied to those terminals.

[f] The range for this frequency domain measurement is 10 MHz to 4 500 MHz.

[g] The far end of the mated cable assembly shall be terminated in its characteristic impedance. Insertion loss variations (i.e., cable length) may change the measurement result.

Editor's Note 3: in table 8, propose adding "Differential impedance imbalance" since it has been defined in table 7 already (for SAS).

5.3.10 Electrical TxRx connections

TxRx connections may be divided into TxRx connection segments. In a single TxRx connection individual TxRx connection segments may be formed from differing media and materials, including traces on printed

wiring boards and optical fibers. This subclause applies only to TxRx connection segments that are formed from electrically conductive media.

Each electrical TxRx connection segment shall comply with the impedance requirements of table 7 for the media from which they are formed. An equalizer network, if present, shall be part of the TxRx connection.

TxRx connections that are composed entirely of electrically conducting media shall be applied only to homogenous ground applications (e.g., between devices within an enclosure or rack, or between enclosures interconnected by a common ground return or ground plane).

5.3.11 Transmitter characteristics

For all inter-enclosure TxRx connections, the transmitter shall be A.C. coupled to the interconnect through a transmission network.

For intra-enclosure TxRx connections the expander transmitter shall be A.C. coupled to the interconnect. Other transmitters may be A.C. or D.C. coupled.

A combination of a zero-length test load and the transmitter compliance transfer function (TCTF) test load methodology is used for the specification of the inter-enclosure and intra-enclosure transmitter characteristics. This methodology specifies the transmitter signal at the test points on the required test loads. The transmitter shall use the same settings (e.g., pre-emphasis, voltage swing) with both the zero-length test load and the TCTF test load. The signal specifications at IR~~,~~and CR~~, and XR~~ shall be met under each of these loading conditions.

The TCTF is the mathematical statement of the limiting transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask.

The transmission magnitude response of the TCTF for IT ~~and XT~~ is given by the following equation for 3,0 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((6,5 \times 10^{-6} \times f^{0,5}) + (2,0 \times 10^{-10} \times f) + (3,3 \times 10^{-20} \times f^2)) \text{ dB}$$

for 50 MHz < f < 3,0 GHz, and:

$$|S_{21}| = -10,884 \text{ dB}$$

for 3,0 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The transmission magnitude response of the TCTF for CT is given by the following equation for 3,0 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((1,7 \times 10^{-5} \times f^{0,5}) + (1,0 \times 10^{-10} \times f)) \text{ dB}$$

for 50 MHz < f < 3,0 GHz, and:

$$|S_{21}| = -10,694 \text{ dB}$$

for 3,0 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The transmission magnitude response of the TCTF for IT ~~and XT~~ is given by the following equation for 1,5 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((6,5 \times 10^{-6} \times f^{0,5}) + (2,0 \times 10^{-10} \times f) + (3,3 \times 10^{-20} \times f^2)) \text{ dB}$$

for 50 MHz < f < 1,5 GHz, and:

$$|S_{21}| = -5,437 \text{ dB}$$

for 1,5 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The transmission magnitude response of the TCTF for CT is given by the following equation for 1,5 Gbps:

$$|S_{21}| = -20 \times \log_{10}(e) \times ((1,7 \times 10^{-5} \times f^{0,5}) + (1,0 \times 10^{-10} \times f)) \text{ dB}$$

for 50 MHz < f < 1,5 GHz, and:

$$|S_{21}| = -7,022 \text{ dB}$$

for 1,5 GHz < f < 5,0 GHz,

where:

f is the signal frequency in hertz.

The TCTF is used to specify the requirements on transmitters that may or may not incorporate pre-emphasis or other forms of compensation. A compliance interconnect is any physical interconnect with loss equal to or greater than that of the TCTF at the above frequencies that also meets the ISI loss requirements shown in figure 15 and figure 16.

Compliance with the TCTF test load requirement shall be determined by measuring the signal produced by the transmitter through a physical compliance interconnect attached to the transmitter.

Compliance with the zero-length test load requirement shall be determined by measurement made across a load equivalent to the zero-length load shown in figure 14.

For both test load cases, the transmitter shall deliver the output voltages and timing listed in table 4 at the designated compliance points. The default mask shall be CR for inter-cabinet TxRx connections and IR for intra-cabinet TxRx connections. The eye masks are shown in 5.3.3.

Figure 13 shows the compliance interconnect test load.

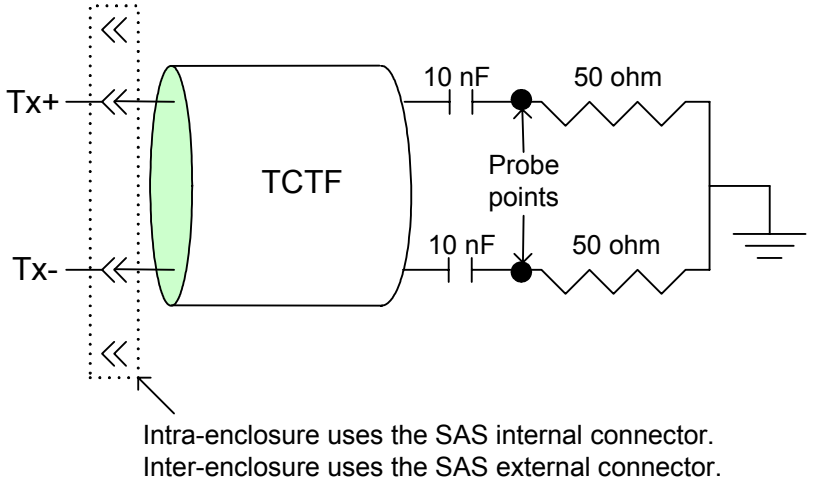

Figure 13 — Compliance interconnect test load

Figure 14 shows the zero-length test load.

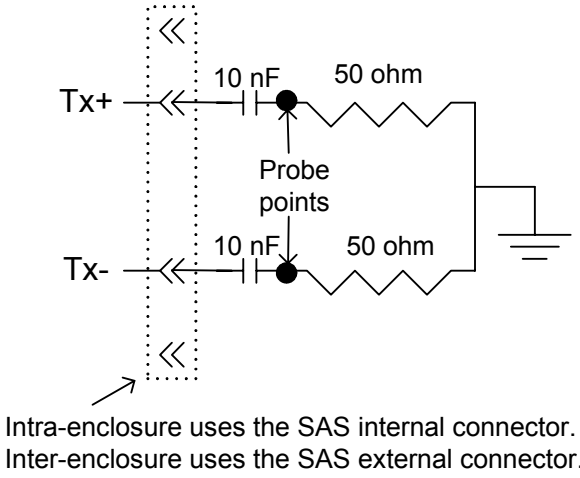

Figure 14 — Zero-length test load

Figure 15 shows an ISI loss example at 3,0 Gbps.

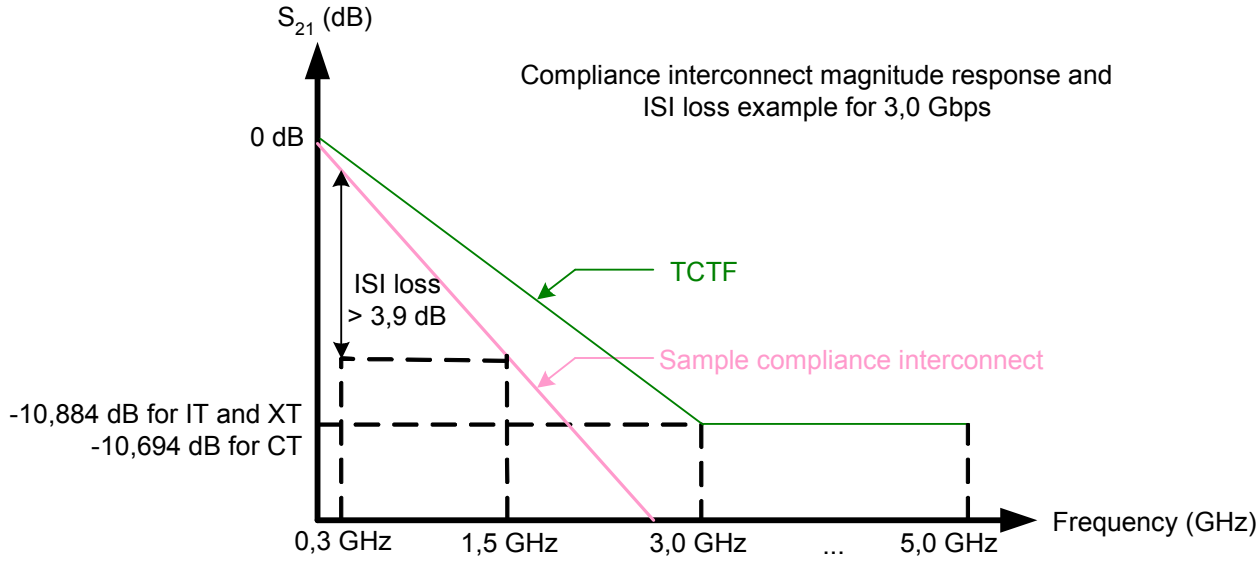

Figure 15 — ISI loss example at 3,0 Gbps

Figure 16 shows an ISI loss example at 1,5 Gbps.

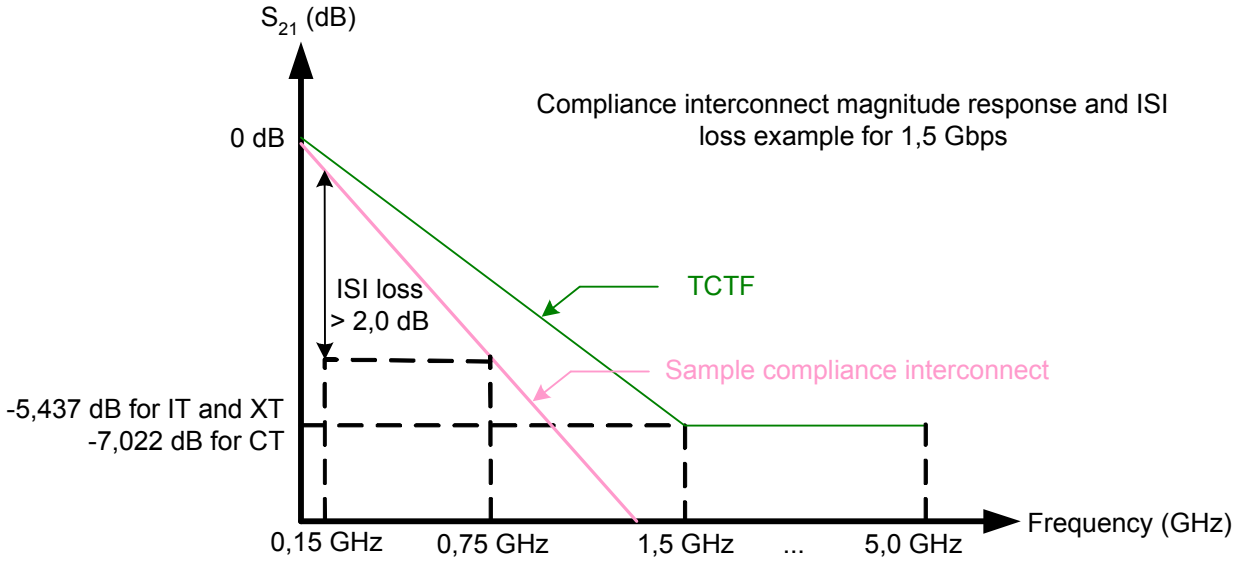

Figure 16 — ISI loss example at 1,5 Gbps

5.3.12 Receiver characteristics

The receiver shall be A.C. coupled to the interconnect through a receive network. The receive network shall terminate the TxRx connection by a 100 ohm equivalent impedance as specified in table 7.

The receiver shall operate within a BER of 10^{-12} when a SAS signal with valid voltage and timing characteristics is delivered to the compliance point from a 100 ohm source. The received SAS signal shall be considered valid if it meets the voltage and timing limits specified in table 4.

Additionally the receiver shall also operate within the BER objective when the signal at a receiving phy has the additional sinusoidal jitter present that is specified in table 6 and the common mode signal V_{CM} over frequency range F_{CM} as specified in table 2. The jitter tolerance figure is given in figure 11 for all Rx compliance points in a TxRx connection. The figure given assumes that any external interference occurs prior to the point at which the test is applied. When testing the jitter tolerance capability of a receiver, the additional 0,1 UI of sinusoidal jitter may be reduced by an amount proportional to the actual externally induced interference between the application point of the test and the input to the receiving phy. The additional jitter reduces the eye opening in both voltage and time.

5.3.13 Spread spectrum clocking

Phys shall not transmit with spread spectrum clocking. Expander phys that support being attached to SATA devices shall support receiving with spread spectrum clocking (see ATA/ATAPI-7 V3). The expander device shall retime data from a SATA device with an internal clock before forwarding to the rest of the SAS domain.

NOTE 2 - If SAS initiator devices support being attached to SATA devices, they should follow the same rules as expander phys.

5.3.14 Non-tracking clock architecture

Phys shall be designed with a non-tracking clock architecture; the receive clock derived from the received bit stream shall not be used as the transmit clock. Expander phys that support being attached to SATA devices shall tolerate clock tracking by the SATA device.

NOTE 3 - If SAS initiator devices support being attached to SATA devices, they should follow the same rules as expander phys.

5.4 READY LED signal electrical characteristics

A SAS target device uses the READY LED signal to activate an externally visible LED that indicates the state of readiness and activity of the SAS target device.

All SAS target devices using the SAS plug connector (see 5.2.3.2) shall support the READY LED signal.

The READY LED signal is designed to pull down the cathode of an LED using an open collector or open drain transmitter circuit. The LED and the current limiting circuitry shall be external to the SAS target device.

Table 9 describes the output characteristics of the READY LED signal.

Table 9 — Output characteristics of the READY LED signal

State	Test condition	Requirement
Negated (LED off)	$0 V \le V_{OH} \le 3,6 V$	$-100 \mu A < I_{OH} < 100 \mu A$
Asserted (LED on)	$I_{OL} = 15 mA$	$0 \le V_{OL} \le 0,225 V$

The READY LED signal behavior is defined in 10.4.1.

6 Phy layer

6.6 Out of band (OOB) signals

Out of band (OOB) signals are low-speed signal patterns detected by the phy that do not appear in normal data streams. They consist of defined amounts of idle time followed by defined amounts of burst time. During the idle time, the physical link carries D.C. idle (see 3.1.30) ~~is transmitted~~. During the burst time, ~~ALIGN (0) primitives are transmitted repeatedly~~the physical link carries signal transitions. ~~The transmitter output levels during burst time and idle time are described in 5.3.4.~~ The signals are differentiated by the length of idle time between the burst times.

SATA defines two OOB signals: COMINIT/COMRESET and COMWAKE. COMINIT and COMRESET are used in this standard interchangeably. Phys compliant with this standard identify themselves with an additional SAS-specific OOB signal called COMSAS.

To transmit an OOB signal, a transmitter shall repeat these steps six times:

1) transmit D.C. idle for an idle time; and
2) transmit an ~~ALIGN~~ OOB burst consisting of ALIGN (0) primitives for a burst time.

It shall then transmit D.C. idle for an OOB signal negation time. The transmitter output levels during burst time and idle time are described in 5.3.4.

The ALIGNs used in OOB signals should be at generation 1 (G1) physical link rates (i.e., 1,5 Gbps). The ALIGNs are only required to generate an envelope for the detection circuitry, as required for any signaling that may be A.C. coupled. If G2 ALIGNs are used, the number of ALIGNs doubles compared with G1 ALIGNs.

A SAS transmitter should transmit ALIGNs at the G1 physical link rate to create the burst portion of the OOB signal, but may transmit ALIGNs at its lowest supported physical link rate if it is not able to transmit at the G1 physical link rate and shall not transmit them at a physical link rate faster than its lowest supported physical link rate.

...

Figure 74: 3 times change ALIGN burst to OOB burst

Figure 75: 2 times change ALIGN burst to OOB burst

...

A receiver shall detect an OOB signal after receiving four consecutive idle time/burst time pairs (see figure 75). It is not an error to receive more than four idle time/burst time pairs. A receiver shall not detect the same OOB signal again until it has detected the corresponding negation time (i.e., a COMINIT negation time for a COMINIT) or has detected a different OOB signal (e.g., if a COMINIT was previously detected, then four sets

of COMWAKE idle times followed by burst times are detected, a COMWAKE is detected; another COMINIT may follow).

A SAS receiver shall detect OOB signals comprised of ALIGN (0) primitives transmitted at any rate up to its highest supported physical link rate. This includes physical link rates below its lowest supported physical link rate (e.g., a SAS receiver supporting only 3,0 Gbps detects 1,5 Gbps based ALIGNs, providing interoperability with a SAS transmitter supporting both 1,5 Gbps and 3,0 Gbps). A SAS receiver that supports SATA devices shall also detect OOB signals comprised of D24.3 characters transmitted at 1, 5 Gpbs.

...

The SATA port selection signal shall be composed of 5 COMINIT signals, each starting a specified time interval, T1 or T2, as shown in figure 76, after the start of the ~~ALIGN~~ OOB burst portion of the previous COMINIT signal. The values of T1 and T2 shall be as shown in table 47.