SAS PHY WG Minutes 9/8/2003   T10/03-314r0

Atterndees:

Peter Herz   3Ware, Inc.
Tim Symons   Adaptec, Inc.
Doug Wagner   FCI
Bill Ham   Hewlett Packard
Rob Elliott   Hewlett Packard
Dan Colegrove   Hitachi Global Storage Tech
Bill Bissonette   Intel Corp
John Lohmeyer   LSI Logic Corp.
Mark Miquelon   LSI Logic Corp.
Jie Fan   Madison Cable Corp.
Wang-Liangjiu   Marvell Semiconductor
Jay Neer   Molex Inc
Jerry Kachlic   Molex Inc
Larrie Carr   PMC-Sierra, Inc.
Rachelle Trent   PMC-Sierra, Inc.
Henry Kuo   QLogic Corp
Alvin Cox   Seagate Technology
Allen Kramer   Seagate Technology
Vit Novak   Sun Microsystems, Inc.
Robert Kando   Texas Instruments
Michael Wamsley   Tyco Electronics
Nitish Amin   Vitesse

22 People present for all or part of the meeting.

The meeting was opened at 1:20, Monday September 8, 2003

Agenda:

1. Internal 4x cable status
2. External cable pin assignment change
3. New items

1. Internal cable status

The 4-lane internal cable proposal 03-240r0 was briefly discussed. Updated
drawings will be included in the next revision of the SFF document to be supplied
by Amphenol. A two-lane proposal is also being added within the SATA
documentation. The SAS PHY WG had no issues with adding the two-lane
version. The number of sideband signals has increased from four to six. All six
sideband signals are included in both the four-lane and two-lane versions.

2. External cable pin assignment change

The majority of the meeting was spent on this topic. Bill Bissonette of Intel presented a background presentation showing the reasons behind desiring a change to the current external pinout. That presentation will be posted as a separate document. SATA ii will use a similar external connector (or the same – keying has not been defined yet in SATA). There are several reasons supporting the pinout change for the SAS external connector:

1. Signal crossover can be achieved within the cable rather than on the PCB.
2. PCB layout is greatly simplified and can reduce the number of layers required on the system or backplane PCB, thus reducing cost and complexity of implementation.
3. SATA has rejected the SAS pinout and will locate the Rx and Tx pairs together rather than at opposite locations on the connector. If SAS does not change, the cable assemblies for SAS and SATA will not interchange.
4. Some hosts buss adapters are designed to support both SAS or SATA modes by determining what is connected to them during the initiation phase. If SAS and SATA external connector pinouts are different, such devices will not provide as much flexibility to the market.
5. 6Gbps applications will benefit from the simplified PCB layout between the IC and the connector.

Reasons to not support the change:

1. Locating TX next to Rx will have greater near-end crosstalk.
2. Designs may exist that have incorporated the original SAS pinout.

Alvin Cox will write the proposal to change the external pinout in SAS 1.1. Effect to SAS 1.0 needs to be determined. This is a major change to the specification in that the proposal requires a cable that is not interchangeable with the existing specification.

3. New business

3Ware desires a twelve-lane external proposal. The proposal would be added to SAS 1.1.

The meeting closed at 4:15 am Monday September 8, 2003.

Alvin Cox
Seagate Technology, LLC