SSM Draft Minutes August 15, 2002

Aug 15 SSM - Foxconn, Radisson – Knotts Berry Farm, Buena Park, California

1. AGENDA SSM MEETING 9:00 AM – 5:00 PM
2. Introductions
3. Attendance

Paul Aloisi	TI	Paul_Aloisi@TI.com	603.222.8687
Jason Chou	Foxconn	Jasonc@foxconn.com	408.919.6141
Dan Dawiedczyk	Molex	ddawiedczyk@molex.com	630.718.5945
A. Bruce Manildi	Seagate	bruce_manildi@seagate.com	831.439.7229
Donald Getty	TI	donald_getty@ti.com	714.593.9856
Henry Chiu	QLogic	henry.chiu@qlogic.com	949.389.6553

4. Agenda development
5. Approval of previous minutes - 02-263r0

Approved – no updates – approved as posted

6. Action item review –

First two are complete, haven't heard from Dick Uber

7. Administrative structure
8. Presentation Policy
10. Presentations
10.1 Carry over presentations

10.1.3 Backplane presentation, [Bruce Manildi]

Bruce delivered a short verbal presentation on the status and methodology going forward on developing models for backplanes. A discussion followed on the difficulties due to the many pairs and the non-uniformity of the trace layout for the different pairs on a backplane. Jason Chou suggested looking into Cadence 'Spectra-Quest' and 'Speed 2000' from Sigrity for backplane simulation.

10.2 New presentations

None

10.3 Basic system model, [Bill Troop IBM]

Bill was not present. Umesh Chandra will contact for availability of model or at least Bill's thinking about the model.

10.4 SSM-2 Document review -
10.4.1 SSM-2

11. Matrix development for SSM-2
11.1 Overview section: owner, (Bill Ham)
11.2 Transceiver chips: owner, (Richard Huber)
11.3 Bus segment termination: owner, (Paul Aloisi / Don Getty)
11.4 Host bus adapter (transceiver board): owners, (Lee Hearn)
11.5 Mated connectors: owner, (Martin Ogbuokiri, Steve Wong)
11.6 Transition regions: owners, (Bob Gannon, Jason Chou)
11.7 Bulk cable: owner, (Jie Fan, Zane Daggett, Greg Vaupotic)

11.8 Backplane: owner, (Bruce Manildi)
11.9 Cable assemblies, owner (Jason Chou (Lead), Bob Gannon, Steve Wong backup)
11.10 How to develop IBIS model section 6.2.1, - Complete for transceivers, Connectors - Molex - Guss Panella (Dan D. will check)
12. Simulation integration strategy
12.1 System configurations - Topology, (Bruce Manildi)
12.2 Data patterns, (Bruce Manildi)
12.3 Data rate - (group) - Ultra640 & Ultra1280 additions

16. Next meetings

Oct 15 SSM Editing, 16 SSM, 17 PIP Jie, Massachusetts
Dec 3 PIP Editing, 4 PIP, 5 SSM Bob Gannon Electronica Pantera, Mexico

17. Action Items:

17.1 Action items from previous meetings

Jie, Nicholaos and Zane Daggett will review cable model section 7.3.2 for the June Editing meeting. Jie Fan will write up a new procedure for creating the models that will be sent to Bruce Manildi before the next meeting, that Bruce will distribute. Verify Gigatest method. (Some input from Jie, but need the multi line with crosstalk)

Richard Huber will review the transceiver model section 7.4.2 for the June Editing meeting.

Lee Hearn & (Paul Aloisi Contact Bill Weurtz for an LSI representative and Qlogic representative) to review section 8.1 & 9.4.3 Host bus adapter model for the June Editing meeting.

Bob Gannon, Nicholaos Limberopoulos & Martin Ogbuokiri will review Cable assemblies section 8.2 for the June Editing meeting.

Bruce Manildi will review the Backplane model section 8.3 & 9.4.3 for the June Editing meeting.

Umesh will contact Bill Troop about reviewing the system section 8.4, 9.5 & 10 for the Oct Editing meeting. (Send request in April, no reply yet)

6.2.1.5.10 Driver section needs the additions for SPI-5 - Bruce Manildi.

Contacted Bill Petty about LSILogic Transceiver involvement – no commitment as of 8/15.
Frank Gasparic to help on driver and transceiver model – will they update the models on the web site.

17.2 New action items from present meeting

17.2.1 Bruce Manildi to follow up on action items.
17.2.2 8 new action items developed during review of SSM-2 rev 3. The results of completion of these action items should complete the document:

17.2.2.1 Transceiver model 7.4.2 – Dick Huber to review
17.2.2.2 Sec 8.1 – review by LSIL, Qlogic, and Adaptec
17.2.2.3 Sec 8.4 – review by Bill Troop of IBM
17.2.2.4 Sec 9.5 – review by Bill Troop
17.2.2.5 Sec 9.2, 9.3, 9.4 call IBIS to see their plans for these models
17.2.2.6 Sec 9.4 – circuit model validation procedure
17.2.2.7 Sec 10 – Simulation strategy – Umesh Chandra
17.2.2.8 Sec 10.2 – Data Pattern – Bruce to call Bill Ham and get his ideas
17.2.2.9
Publish rev 3 on T10 website – Bruce Manildi

18. Adjourn