SCSI signal modeling study group (SSM) 01-126r0
April 04, 2001
Westboro, MA

Subject: Draft minutes for the SSM working group on April 04,05 2001 in Westboro, MA

This was the next meeting to address the general subject of modeling for parallel SCSI. Paul Aloisi of TI led the meeting. Bill Ham of Compaq took these minutes. There was a good attendance from a broad spectrum of the industry. Jie Fan of Madison Cable hosted the meeting.

Last approved minutes: 01-075r1.

1. AGENDA SSM MEETING

1. AGENDA SSM MEETING....1
2. Introductions....2
3. Attendance....2
4. Agenda development....3
5. Approval of previous minutes....3
6. Action item review....3
7. Administrative structure....3
8. Presentation Policy....3
9. Presentations....4
 9.1 Carry over presentations....4
  9.1.1 Cable extraction data, Jie Fan, Umesh, Madison, using bulk cable from PIP round robin 2....4
  9.1.2 Periodic Structures in transmission lines, Larry Barnes, LSI Logic....4
  9.1.3 Parameter extraction for transition region models, Bob Gannon 4
  9.1.4 Models for instrumentation interfaces status, Jason Chou....5
 9.2 IBIS status, Larry Barnes....6
 9.3 New presentations....6
10. Creation of a basic system model, Bill Troop IBM....7
 10.1 Purpose....10
 10.2 Simulation Overview....10
 10.3 Details of Simulation....11
 10.4 Conclusions....12
11. Matrix development for SSM....13
 11.1 Transceiver chips: owner, Larry Barnes....13
 11.2 Bus segment termination: owner, Paul Aloisi / Don Getty....14
 11.3 Host bus adapter / target board (transceiver board): owner, Lee Hearn....14
 11.4 Mated connectors: owner, Martin Ogbuokiri....14
 11.5 Transition regions: owners, Bob Gannon, Greg Vaupotic....14
 11.6 Cable (bulk cable): owner, Jie Fan, Zane Daggett, Greg Vaupotic 15
 11.7 Backplane: owner, Larry Barnes....15
 11.8 Cable assemblies, owner TBD....15
 11.9 How to develop IBIS model annex, Barnes....15
12. Simulation integration strategy....15

12.1 System configurations - Topology 16
12.2 Data patterns, Bill Ham (new owner) 16
12.3 Data rate 17
13. Tools: 17
14. Document framework, Barnes 17
15. Should the group standardize on the IBIS connector matrices? 17
16. New business 18
17. Next meetings 18
18. Action Items: 18
18.1 Action items from previous meetings 19
18.2 New action items from present meeting 20
19. Adjourn 20

2. Introductions

Paul Aloisi opened the meeting and conducted the introductions and reviewed the meeting purpose. He thanked Jie Fan of Madison Cable for hosting the meeting.

3. Attendance

Attendance at working group meetings does not count toward attendance requirements for T10 plenaries.

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Paul Aloisi	Texas	paul_aloisi@ti.com	603-429-8687

	Instruments		

4. Agenda development

The agenda shown was that used.

5. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were made. Paul Aloisi moved and Greg Vaupotic seconded that the draft minutes be approved. Motion passed unanimously. This document will be posted as document 01-075r1.

6. Action item review

The action items were reviewed with the status indicated in the action item section of the minutes.

7. Administrative structure

The present administrative structure for SSM is:

Paul Aloisi, TI, chair
Larry Barnes, LSI Logic, Vice chair
Bill Ham, Compaq, Secy

8. Presentation Policy

This item is included for easy reference and will be retained in future minutes.

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

9. Presentations

9.1 Carry over presentations

9.1.1 Cable extraction data, Jie Fan, Umesh, Madison, using bulk cable from PIP round robin 2

2D extraction models from cable design information for round cable were determined to be not practical due in part to the intrinsically 3D nature of the problem. Gigalabs is going to provide S-parameter measurements and RLGC models.

From here the intent is to use these RLGC models as part of the system simulation modeling effort (led by Bill Troop).

9.1.2 Periodic Structures in transmission lines, Larry Barnes, LSI Logic

[Item is still active but no new input this meeting.]

9.1.3 Parameter extraction for transition region models, Bob Gannon

[Still active and ongoing]

Bob noted that a company called Gigatest (www.gigatest.com) is in business to extract parameters from physical samples. Bob noted that they could be used for the cable assembly transition region models.

A possible coalition of cable assembly manufacturers could jointly approach Gigatest with the job of creating a model for a round cable to VHDCI transition region.

Another company called Zuken was mentioned by Larry B that can be contracted to build IBIS and HSPICE models from various starting points.

Bob Gannon is actioned start a group of cable assembly folks to create a transition region model using Gigatest as the vehicle.

The intent of this effort is to produce an RLGC model of the types of transition region types identified below:

- 30 AWG solid shielded round to VHDCI
- 30 AWG solid twist and flat to HD68 (actually being done by Bob himself)

These models will be delivered to Bill Troop for integration with the system simulation effort.

[This material needs to be moved into the document.]

In satisfaction of an action item the following matrix of transition regions and issues with each is defined:

Flat to connector- Boundary is the face of the IDC contact that touches the copper conductor.

Issues- Geometry of deformed insulation is difficult to measure and represent via CAD to capture impedance discontinuity. 3D CAD transformation needed to represent length of discontinuity is difficult to draw. Ansoft 3D package produces R,L, and C values, but no G.

Twist and Flat to connector- Boundary is the face of the IDC contact that touches the copper conductor.

Issues- Same as above with the additional concern of how to concatenate the twist and flat regions via SPICELink. There is no actual shield for physical ground reference. One needs to model +/- 1 signal sources, but the actual ground is virtual.

Round shielded to connector- Boundary is the beginning of the fan out required for attachment to connector at the point of crimp, solder or weld.

Issues- Accurate CAD representation of the fan out to contact to connector is very difficult to produce. Currently parameter extraction is under investigation with Gigatest Labs.

Round shielded (may be shielded and folded multi-twinax) to pcb- Boundary is the beginning of the fan out required for attachment to connector and the point of attachment of the wires to the pcb solder pads.

Issues- See above. The pcb solder to wire region is an additional CAD nightmare.

9.1.4 Models for instrumentation interfaces status, Jason Chou

[No new input at this meeting]

Jason has been working on the models to be used for instrumentation interfaces (such as oscilloscope probes). His investigation showed that

modeling is not in the mindset of the common instrumentation suppliers. Tektronix agreed to try to develop a model for the active differential probe. It was noted that the single ended probe may be more important because the differential probe gives no information about the common mode content of the signals and two single ended probes gives both the differential and the common mode.

Jason also explored the information available from basic circuit description of the probes. It was quickly determined that only active probes should be considered for SSM uses.

The capacitance levels reported by Jason appeared significantly higher than is available on state of the art probes.

Jason is actioned to provide a draft for the instrumentation interface section of the document.

9.2 IBIS status, Larry Barnes

Larry reviewed the present status with IBIS.

It has been determined that there is no way to model run length dependent (data pattern dependent) driver signals with present IBIS specifications. It has also been determined that current mode drivers cannot be accurately modeled with IBIS.

The run length dependent capability is being approached by introducing a programmable switch delay that allows a change in driver level after some delay. This allows a two level pre comp (as in SPI-4) to be accepted in an IBIS format. This capability is expected to be available in commercial tools within 6 months.

A more general approach called IBIS-x (a macro driven modeling syntax that is very different from, but backwards compatible with, the present IBIS) is also under development. IBIS-x will support current mode drivers as well as multilevel precompensation methods. Receiver modeling is also comprehended in IBIS-x. IBIS-x is expected to go for public comment in June 2001. IBIS-x could be available in commercial tools by spring 2002 or so.

IBIS models for SCSI that use current mode drivers will have to be approached creatively until IBIS-x is available.

The next IBIS forum meeting is April 20, 2001 (con call).

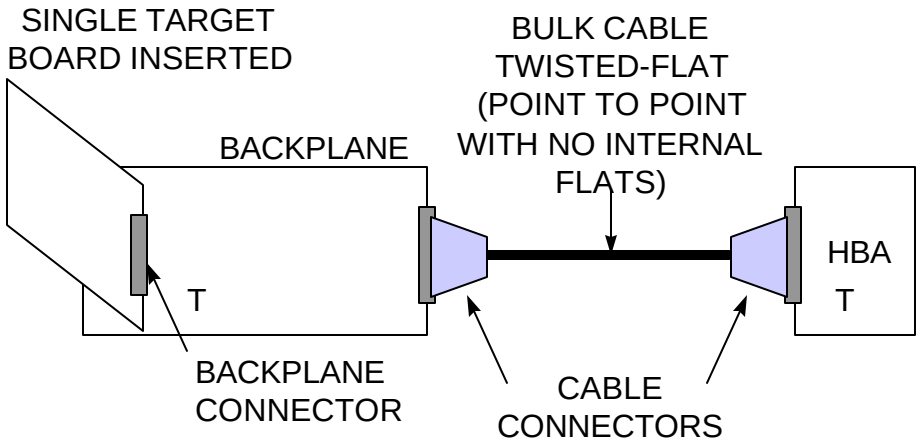
9.3 New presentations

None

10. Creation of a basic system model, Bill Troop IBM

Bill has executed the first complete simulation of a "real" SCSI construction in the SSM group. This is also probably the first time this has been done in the industry. This effort has been exceptionally useful in identifying properties and issues.

The trial basic composite simulation effort defined in the last meeting (shown below) was used with the addition of 5 more target boards.



TERMINATORS, T, ARE ATTACHED TO THE BACKPLANE AND HBA BOARDS

DRIVERS AND RECEIVERS AND ATTACHED TO THE TARGET AND HBA BOARDS

This is intended to be used as an example of a realistic complete SCSI segment and is expected to show where we have weaknesses in the concepts and model interfaces.

The general idea is for models of each element to be supplied in the form previously recommended and to actually create an overall integrated model that will yield waveforms.

The slightly edited version of Bill Troop's report on the effort is included below:

Report on a SCSI System Simulation
For The
T10 SCSI System Modeling (SSM) Group

Preliminary Results on Correlating Simulation Models with Actual Waveforms.

Written: May 30, 2001
Revised: April 26, 2001

Authors:
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Brad Herrman herrman@us.ibm.com

Table of Contents:

Purpose 10
Simulation Overview 10
Details of Simulation 11
Conclusions 12

List of Tables:

Table 1: Simulation Model Types 11

Table of Figures

Figure 1: Overview of SCSI Simulation System 11
Figure 2: Results of Simulation 12
Figure 3: Actual Waveforms at the SCSI Initiator Connector 13

10.1 Purpose

This primary purpose of this effort is to determine which simulation tool will allow a SCSI low voltage differential (LVD) initiator board to be connected to a multi-slot SCSI backplane using a cable. The tool must support IBIS models for the active components and RLGC models for the cables and connectors.

10.2 Simulation Overview

Since SCSI driver IBIS models that will perform cutback do not exist, 160M bytes per second operation will be used for this phase of the simulations. Using the Cadence SpectraQuest tool, a SCSI system model was created. A LSI SCSI initiator IBIS model was used as an SCSI signal source. An edge coupled, coplanar micro strip configuration printed circuit board model was used to connect the SCSI initiator to a surface-mounted 68-pin SCSI unshielded receptacle connector. The PCB model had a differential impedance of approximately 120 Ohms. A 2x2 RLGC model was used to represent a differential pair of conductors of a twist and flat cable. The other end of the cable is terminated in a 68-pin unshielded EBBI style plug connector. An Allegro board file from an existing six-slot SCSI DASD backplane was imported. The backplane was designed for Ultra 160 SCSI operation. It has six SCA-2 connectors with an electrical spacing of about 3 inches. It uses LVD SCSI signal terminator modules at the far end of the SCSI bus and next to the initiator module. The differential impedance of the unloaded backplane is approximately 130 Ohms. The backplane also has a SAF-TE module for monitoring system environmental parameters. All six slots of the backplane have hard drives inserted.

The original idea was to use IBIS models for the simulation components. However, it turned to be difficult to obtain verified IBIS models from most of the vendors. The IBIS models that we received either would not import into our system or had obvious errors that took multiple iterations with the vendors to correct. None of the vendors had any data to prove that the IBIS models were in any way correlated to reality. Most of the connector models were delivered to us in Spice format. The SCA-2 connector spice models were too cumbersome to simulate in a multi-connector backplane environment in a reasonable length of time. We found that a lumped RLC model gave us comparable results to the detailed single connector spice model in our environment and reduced the simulation time significantly. Table 1 lists the components involved in the SCSI system simulation and the model types associated with them.

Device	Model Type
SCSI Initiator	IBIS
Initiator PCB	Topology
68-Pin ANSI SCSI PCB Connector	Spice / RLGC
68-Pin ANSI SCSI Cable Connector	Spice / RLGC
Twist and flat cable	RLGC
68-Pin EBBI SCSI Cable Connector	Spice /RLGC
68-Pin EBBI SCSI PCB Connector	Spice / RLGC
Backplane PCB	Topology
HDD SCA-2 Connectors	Spice / RLGC
Hard Drives	Empirical text data
SAF-TE Chip	IBIS
SCSI LVD Terminator	Spice

Table 1: Simulation Model Types

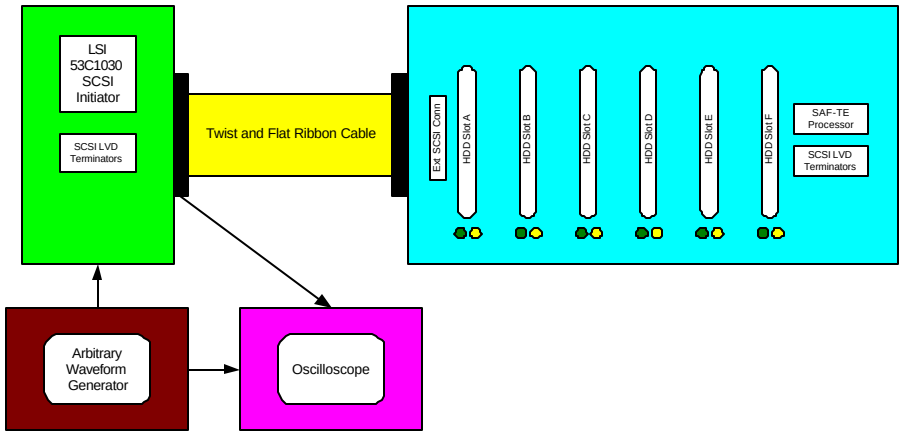

Figure 1: Overview of SCSI Simulation System

10.3 Details of Simulation

The simulation system is shown in Figure 1. A test board using the LSI SCSI initiator integrated circuit is connected using a coaxial cable to an Arbitrary Waveform Generator (AWG). The test board is connected using a twist and flat TPE cable to the SCSI hard drive backplane. The AWG is programmed to generate a string of data consisting of 3 low periods, 1 high period, 3 low periods, 3 high periods, 1 low period, 3 high periods, 1 low period, 1 high period, 1 low period, 1 high period, 1 low period, 1 high period. A LVD oscilloscope probe is attached to the SCSI signal near the initiator cable connector.

This simulation defines the period at 25 ns, which translates to a bus speed of 160 Mega transfers per second. This string is short enough to simulate in a reasonable length of time. The expectation of this effort is to validate the models used in the simulation so that more detailed results can be obtained later. Figure 2 shows the simulation results using the above described data string. The actual waveforms are shown in figure 3.

10.4 Conclusions

The results of this effort demonstrate the need to have the simulation models validated with the actual devices they purport to represent. The connector models need to be simplified multi-line models. The impedance of a loaded SCSI system is much lower than the unloaded system. The resistance values used for the termination of the bus should be matched to the actual system impedance. In the actual data, the waveform charged up the bus with a DC bias that was not shown in the simulation. A reflection into the switching region in the actual waveform did not show up in the simulation. Nevertheless, the results obtained in the lab and in the simulation are similar enough to encourage the effort to continue.

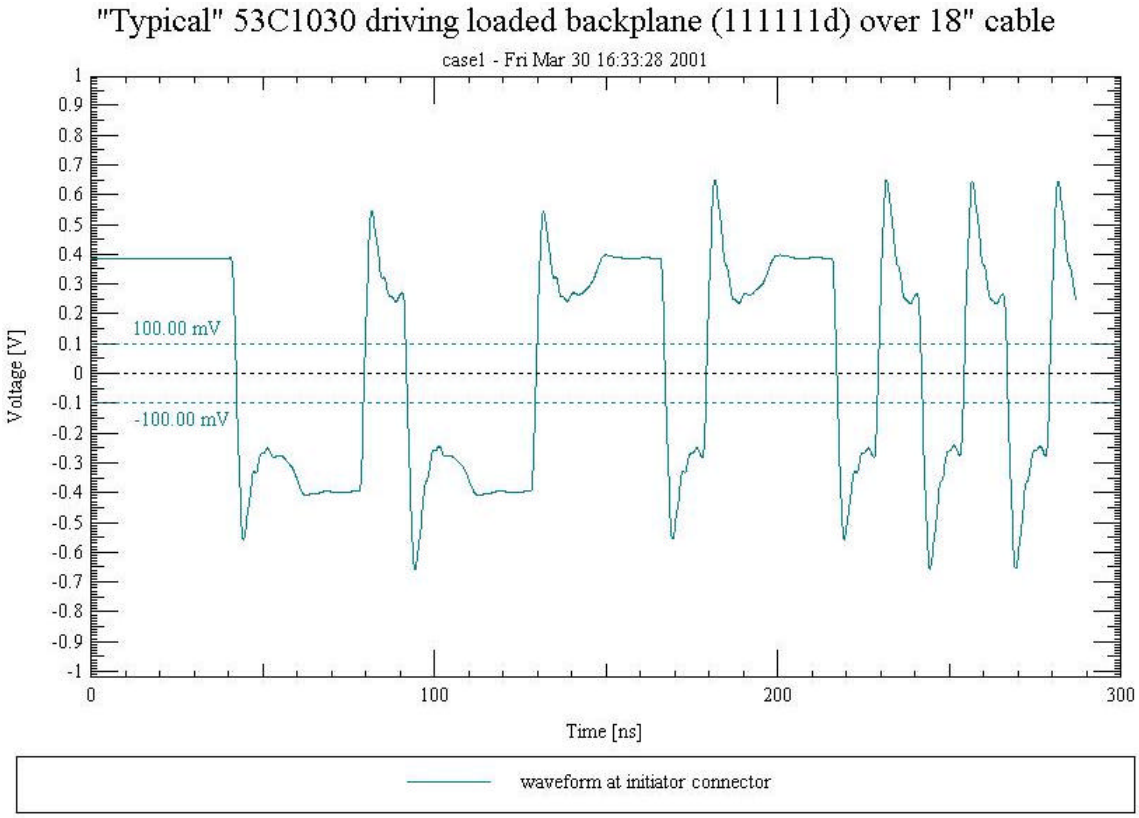

Figure 2: Results of Simulation

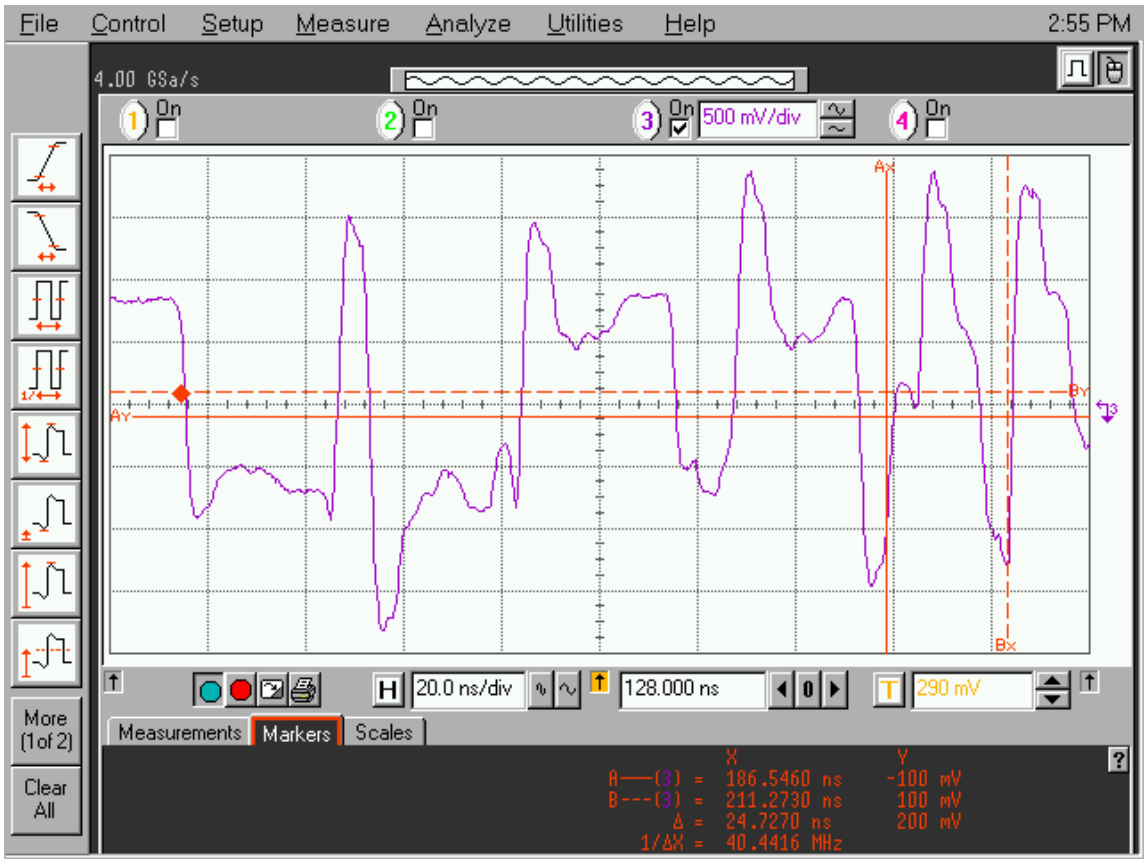

Figure 3: Actual Waveforms at the SCSI Initiator Connector

11. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This matrix is a concise description of the methodology to be used for the respective areas of the point to point SCSI bus segment. Several of the areas were significantly modified at this meeting. Note that the multidrop areas have not yet been identified.

This section contains some repeated information from the last minutes as it continues to be relevant and current.

11.1 Transceiver chips: owner, Larry Barnes

Interface is at packaging pins
Model types: Behavioral only (because it is the only transportable type)
Data patterns: TBD

ISI compensation: required but not presently believed compatible with IBIS capability – this means that IBIS will have to be enhanced.
Single line required - cross talk from non SCSI sources not considered in the model, SCSI line cross talk is not significant within the transceiver. Therefore multiline models are not required for transceivers. (Possible risk with some package types.)

11.2 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins
Model types: Either circuit or behavioral
Terminator type: multimode
Single line only

11.3 Host bus adapter / target board (transceiver board): owner, Lee Hearn

Interface is at transceiver board connectors used for the SCSI link (at the board side of the connector - not including the connector), transceiver chip pins, terminator chip pins, unused connectors are part of the board
Model types: Circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

11.4 Mated connectors: owner, Martin Ogbuokiri

No new content information.

Interface is at transceiver board and the beginning of the cable assembly transition region
Model types: Circuit
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,
single line, multiline

Connector models are in place at the Molex web site and pointers are now in place on the T10 site.

11.5 Transition regions: owners, Bob Gannon, Greg Vaupotic

Interfaces are at the connector termination and the uniform media

Model types: circuit
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multi-line

A start was made in this area – see Bob Gannon presentation above.

11.6 Cable (bulk cable): owner, Jie Fan, Zane Daggett, Greg Vaupotic

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: RLGC
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

11.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted components, (this subject is still not settled)
Model types: circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Issue: how to handle the unmated connectors on the backplane. Two sub issues: (1)lack of existence of unmated connector models and (2) convergence of the simulation with dangling open circuits. The latter can be handled by adding a high value resistance to the open circuit to "fool" the simulator.

11.8 Cable assemblies, owner TBD

Interfaces: connectors
Model types: circuit (possible combination of circuit and behavioral)
Constructions: point to point, multidrop

11.9 How to develop IBIS model annex, Barnes

Not discussed at this meeting.

12. Simulation integration strategy

Determine the goal of the simulation (examples: validate the basic behavior of a new component in a system, troubleshooting guidance, qualification of the signal integrity in a specific configuration, characterization of the expected EMI performance)

Determine the specific characteristics that are sought (example: ??)

Define the topology

Define the collection of components

Obtain the models for all the components

……subject discussion truncated – will continue next meeting.

12.1 System configurations - Topology

[Need pictures for below]

The following is a starting list of system configurations that need different considerations from a modeling perspective. Note that a device may be a SCSI expander.

1. Basic structure shown in the trial simulation work (single initiator/cable/single target on backplane)

2. Basic structure shown in the trial simulation work (single initiator/cable/multiple targets on backplane)

3. Expander isolated backplane with multiple targets on backplane

4. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). All connectors have devices attached.

5. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). Only the far end connector has a device attached - all other connectors have no devices attached - requires an unmated half-connector model.

6. Single target in an enclosure with a cable connection on the enclosure bulkhead to a round cable to an HBA in a different enclosure

12.2 Data patterns, Bill Ham (new owner)

Not discussed at this meeting. The main issue appears to be the ability of specific simulation packages to handle logical data pattern specifications.

12.3 Data rate

This item is left on the agenda due to lack of formal action on the topic. There is nothing special about the data rate that has been identified to date.

13. Tools:

Not discussed at this meeting. [Secy note, do we need to continue this item on the agenda?]

14. Document framework, Barnes

The document was reviewed and extensive modifications were made by the section editors. A publishable version of the document is nearly ready. Another off cycle editing meeting is needed to conclude this topic.

15. Should the group standardize on the IBIS connector matrices?

The following was copied from a recent IBIS meeting which shows the present status.

CONNECTOR SPECIFICATION Gus Panella, Molex

Gus Panella reported on the progress of the IBIS Connector Specification and reported on some of the changes:

- Removal of Physical Map because of unnecessary complexity
- Distinction of Side_A and Side_B pin maps
- Clarification of [Redistribution] Specific to mean comments are in the Header section
- Some number of pins, rows, and columns ranges to document physical limits
- More [Cn_Row_Swath] and [Cn_Column_Swath] distinction and edge definitions and usage

Gus stated that the current discussions involve following the IBIS-X group header suggestions, where practical. These include bracketing the header with [Begin Header] and [End Header] keywords.
He concluded that the document is reaching technical completion. The plan is to release the document for full IBIS Committee technical review and comments while the editorial cleanup of the document is being done.

IBIS CONNECTOR SPECIFICATION: PRELIMINARY PROPOSAL FOR A PIN NAMING LANGUAGE Ian Dodd, Cadence Design Systems

As part of the Connector Specification presentation, Ian Dodd displayed and discussed aspects of a proposal for pin naming language. The main points of the proposal are:

- Adopts C - like code style including C style formatting statements
- Predefines certain variables ROW, COLUMN, SIGNAL_NAME, and PIN_NAME
- Presumes all variables are integers and do not need to be declared
- Includes simple math operations and conditionals
- It can easily specify incrementing characters through addition
- The proposal might be compatible with the IBIS-X macro language.

There was no conclusion to this issue in this meeting. Resolution needs to wait until IBIS actually has this option available.

16. New business

17. Next meetings

Approved schedule:

June 13-14, 2001 1:30PM to 6 PM 06/13; 9AM to 6PM 06/14 New Haven, CT (Amphenol Spectra Strip)

Editing meeting in Colorado Springs at LSI Logic on 05/10,11, 2001 (looks like this may be a con call instead of a face to face meeting.)

Requested schedule:

August 15-16, 2001 1:30PM to 6 PM 08/15; 9AM to 6PM 08/16 Orange Co, CA (TI)

October 24-25, 2001 1:30PM to 6 PM 10/24; 9AM to 6PM 10/25 Colorado Springs, CO (LSI Logic)

December 12-13, 2001 1:30PM to 6 PM 12/12; 9AM to 6PM 12/13 Guadalajara, MX (JPM)

18. Action Items:

18.1 Action items from previous meetings

Status as of this meeting is shown.

Bruce Manildi to provide access information for the Seagate transceiver models to the T10 web site.
Status: A commitment now exists from the chip supplier to Seagate for IBIS models (no precomp). Encrypted HSPICE models are currently available from Seagate (NDA required). IBIS models are also available (conditions for release need to be established). Information needs to be loaded to the T10 web site. Umesh is the contact - carried over with significant progress.

Richard McMillan to provide access information for the Adaptec transceiver models to the web site.
Status: overcome by events - Adaptec does not intend to provide transceiver models in support of the SSM effort

Jie Fan, Madison Cable to provide access info for a cable media model to the T10 web site.
Status: model is done, verified and will be made available in circuit form - still needs info supplied to T10 web site - carried over

Bob Gannon to produce matrix of transition regions and issues with each.
Status: done

Zane Daggett, Hitachi, to provide bulk cable models to the SSM web site (per last meeting minutes).
Status: expect posting before next meeting (round 30 AWG solid will go up first followed by flat TPO) - carried over

Paul A to send emails to all folks with open action items on Tuesday of each week (until the action item is completed).
Status: ongoing

Larry Barnes to take the material in the SPI-3 and SPI-4 document relating to the signal budget and figure out how to incorporate into the SSM document
Status: carried over

Larry Barnes to send aperiodic emails to all folks with open document issues (until the issue is closed).
Status: ongoing

Section editors to provide material to Larry for the next revision of the document.
Status: ongoing

Bill Ham to add the interoperability material to his section
Status: partially done

Greg Vaupotic to post the document relating to reading the Ansoft matrix.
Status: done 01-111r0

TI (Don Getty) to post model info for terminators to the T10 web site.
Status: carried over with progress

Bob Gannon is actioned start a group of cable assembly folks to create a transition region model using Gigatest as the vehicle.
Status: done - Bob Gannon, Jason Chou, Greg Vaupotic, Dave Chapman?

Jason is actioned to provide a draft for the instrumentation interface section of the document.
Status: carried over

18.2 New action items from present meeting

Ham to contact JL to determine position on providing pointers to extracted models not from suppliers.
Status: new

Paul A. to place the SSM-2 project proposal on the web site and post the information on the reflector.
Status: new

19. Adjourn

The meeting adjourned at 6:00 PM