SCSI signal modeling study group (SSM) 01-075r1
April 04, 2001
Westboro, MA

Subject: Approved minutes for the SSM working group on February 21, 22, 2001 in Cypress, CA

This was the next meeting to address the general subject of modeling for parallel SCSI. Paul Aloisi of TI led the meeting. Bill Ham of Compaq took these minutes. There was a good attendance from a broad spectrum of the industry. Jason Chou of Foxconn hosted the meeting.

Last approved minutes: 01-020r1.

1. AGENDA SSM MEETING

2. Introductions

Paul Aloisi opened the meeting and conducted the introductions and reviewed the meeting purpose. He thanked Jason Chou of Foxconn for hosting the meeting.

3. Attendance

Attendance at working group meetings does not count toward attendance requirements for T10 plenaries.

Name	Company	E-Mail	Phone
Paul Aloisi	TI	Paul_Aloisi@TI.com	603-429-8687
Larry Barnes	LSI	larry.barnes@lsil.com	719-533-7432
Jason Chou	Foxconn	JasonC@foxconn.com	408-919-6141
Zane Daggett	Hitachi	zdaggett@hcm.hitachi.com	603-669-4347x236
Jie Fan	Madison Cable	jfan@madisoncable.com	508-752-2884
Bob Gannon	JPM	rgannnon@jmpco.com	860-537-6800
Don Getty	TI	Donald_getty@TI.com	408-246-3100x41
Bill Ham	Compaq	bill_ham@ix.netcom.com	
David MacQuown	Adaptec	david_macquown@corp.adaptec.com	408-957-6749
Martin Ogbuokiri	Molex	mogbuokiri@molex.com	630-527-4370
Dima Smolyansky	TDA	dima@tdasystems.com	503-246-2272
Bill Troop	IBM	troop@us.ibm.com	919-254-2695

4. Agenda development

The agenda shown was that used.

5. Approval of previous minutes

The minutes of the last meeting were reviewed and minor changes were made. Bill Ham moved and Zane Daggett seconded that the draft minutes be approved. Motion passed unanimously. This document will be posted as document 01-020r1.

6. Action item review

The action items were reviewed with the status indicated in the action item section of the minutes.

7. Administrative structure

The present administrative structure for SSM is:

Paul Aloisi, TI, chair
Larry Barnes, LSI Logic, Vice chair
Bill Ham, Compaq, Secy

8. Presentation Policy

This item is included for easy reference and will be retained in future minutes.

It is the policy of the SSM working group that all material presented at the SSM working group shall be made available electronically and posted on the T10 web site.

Material presented at the meeting should be uploaded to the T10 web site two weeks prior to the meeting. Alternatively the material may be electronically supplied to the chair or secretary at the meeting where the material is presented at the discretion of the chair.

Material should be free from any statement of confidentiality or restriction of use and should not contain any pricing or product scheduling information.

9. Presentations

9.1 Carry over presentations

9.1.1 Cable extraction data, Chuck Grant, Umesh, Madison, using bulk cable from PIP round robin 2

Deferred to next meeting.

9.1.2 Periodic Structures in transmission lines, Larry Barnes, LSI Logic

[Item is still active but no new input this meeting.]

9.1.3 Cable media modeling, Greg Vaupotic, Spectra Srip

[This material needs to be transferred to the document]

Greg went through material supplied to Larry Barnes for the document relating to modeling non-uniform cable media. A copy of this material is included below. Greg also went thru a presentation relating to how to read the outputs from the Ansoft tool. Greg is actioned to post the document relating to reading the Ansoft matrix.

Modeling Cable

A Twist N' Flat® ribbon cable is modeled as an example. Measurements from real samples are compared to modeled impedance. Regrettably, actual permittivity and dimensions are withheld due to proprietary concerns.

When a person lacks experience using electromagnetic simulators, and first starts modeling cable, careful attention must be given to several points.

Do not trust permittivity and loss tangent values provided on raw material data sheets. It is strongly recommended that material samples be measured using a wide bandwidth material analyzer, recording permittivity and loss tangent versus frequency.

Beginners usually want to start by examining real problems. This may not be the best way to begin. Instead, it might be better to gain modest experience by examining several structures where the results are already known. After the beginner can successfully model these known structures, achieving proper results, then careful examination of unconventional structures may begin. The Microwave Engineer's Handbook Volume 1 (Artech House) provides many structures and has generalized graphs showing both even-mode and odd-mode impedance. If one uses the Handbook examples, consider setting permittivity equal to one. When permittivity equals one, signal velocity is 100% of light speed. Then the beginner may calculate capacitance from the Handbook to compare with simulated capacitance.

For light speed: propagation time per meter = 3.3356 ns / meter and we know that

$$\text{PropTime per meter} = Z * C$$

so we can say

$$3.3356 * 10^{-9} = Z * C$$

and we can therefore calculate the implied Handbook capacitance

$$C = \frac{3.3356 * 10^{-9}}{Z} \quad \text{pF / meter}$$

to compare with simulated capacitance.

Another area for concern is how a cable structure is drawn for simulation. Simulators have a boundary that is drawn around the cable image. The simulator defines this boundary as ground. This ground must be much larger that the cable image for the simulated results to be correct, especially if the cable in question is not shielded. The author will usually start with a boundary that is 10 times the size of an unshielded cable image. Experiment is recommended. If changing the boundary size has trivial effect on the simulated results, then the boundary is probably large enough.

Sometimes, when drawing the cable, one might consider minor simplification to the drawing. The author's simulator (Ansoft) has a very primitive drawing program that makes it very difficult to draw very fine detail. For example, it is much easier to draw a Twist N' Flat® cable if the very thin lamination is ignored. The error will be very small, and the drawing will be much easier. Some structures, such as shielded parallel pairs, are easy to draw in detail.

One last point must be mentioned. With proper problem setup, the author has found all odd mode simulations to be correct. Even mode capacitance is also always correct. Even mode inductance is correct if simulations are performed using the L matrix and C matrix (no frequency dependence). However, when using the frequency dependent Impedance Matrix and Capacitance Matrix, serious errors have been observed in the calculated even mode inductance. Extreme caution is advised when calculating even mode inductance (and therefore even mode impedance and even mode propagation velocity). The source of this error is presently unknown.

An example

Five pairs from the flat region of a Twist N' Flat cable (very thin laminate ignored):

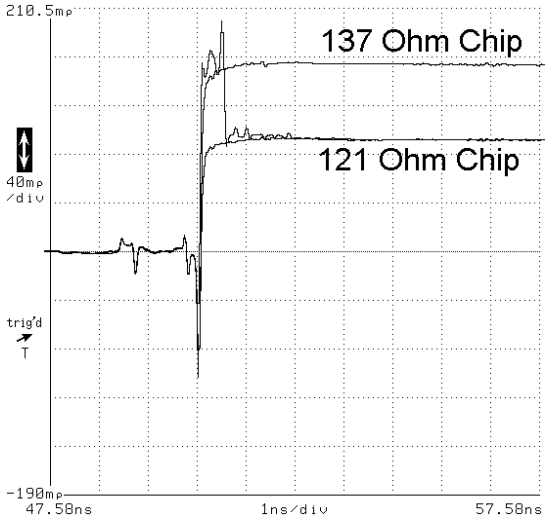
Undriven wires floating, not grouped.

Ansoft was used calculate the L matrix and C matrix. Ansoft's output included the Characteristic Impedance Matrix from which odd mode Z was calculated.

(We know that $Z_{DIFFERENTIAL} = 2 * Z_{ODD}$).

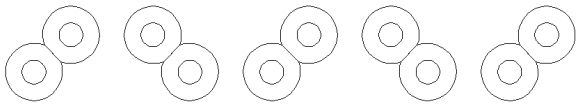
Results for Flat Region

Zodd = 71.89 Ω Þ Zdiff = 143.8 Ω



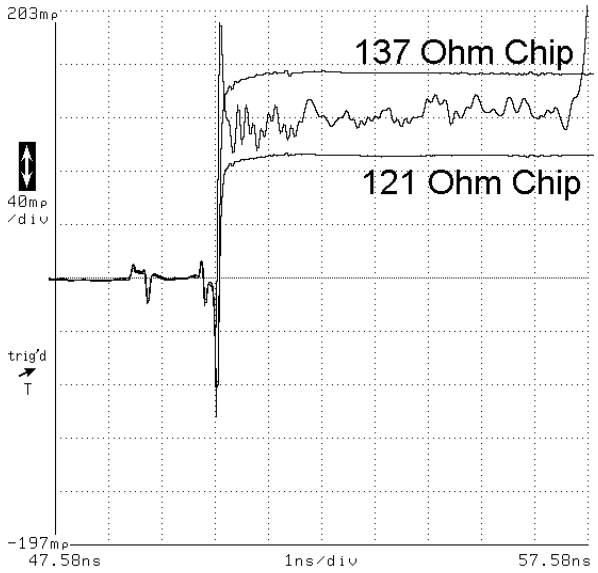
Expect 144 Ω from Modeling, measure ≈ 142 Ω

Twist Section



Results for Twist Region

Zodd = 62.77 Ω Þ Zdiff = 125.5 Ω



Expect 125.5 Ω from Modeling, measure ≈ 126 Ω

9.2 New presentations

9.2.1 Parameter extraction for transition region models, Bob Gannon

Bob noted that a company called Gigatest (www.gigatest.com) is in business to extract parameters from physical samples. Bob noted that they could be used for the cable assembly transition region models.

A possible coalition of cable assembly manufacturers could jointly approach Gigatest with the job of creating a model for a round cable to VHDCI transition region.

Another company called Zuken was mentioned by Larry B that can be contracted to build IBIS and HSPICE models from various starting points.

Bob Gannon is actioned start a group of cable assembly folks to create a transition region model using Gigatest as the vehicle.

9.2.2 Models for instrumentation interfaces status, Jason Chou

Jason has been working on the models to be used for instrumentation interfaces (such as oscilloscope probes). His investigation showed that modeling is not in the mindset of the common instrumentation suppliers. Tektronix agreed to try to develop a model for the active differential probe. It was noted that the single ended probe may be more important because the differential probe gives no information about the common mode content of the signals and two single ended probes gives both the differential and the common mode.

Jason also explored the information available from basic circuit description of the probes. It was quickly determined that only active probes should be considered for SSM uses.

The capacitance levels reported by Jason appeared significantly higher than is available on state of the art probes.

Jason is actioned to provide a draft for the instrumentation interface section of the document.

9.2.3 IBIS presentations, Larry Barnes

Larry went thru a series of presentations that may be found on the IBIS web site (www.eigroup.org/IBIS/Default.htm) Look for “articles” and then for “IBIS summit” then to Jan 01 directory.

Files mcmorrow.doc, dagostino.ppt, hegazy.ppt, were discussed.

Summaries for these presentations follow:

IBIS DOCUMENTATION FOR ACME ENGINEERING Scott McMorrow, Siqual Corporation

Documented a process used by a commercial IBIS model creator for developing and validating IBIS models. Salients points are

- Issues with gathering all of the specification and Spice model information from SPICE supplier – notably initial conditions and description of nodes and signals.
- Models developed by using internal tools based on improvements to the s2ibis2 utility.
- Models checked against several test circuits similar to those in the IBIS Accuracy Report. In particular a transmission line with a small capacitive loads are used. Figures of Merit are given with the model with an expected the range of 97% to 99%.
- Wrong die capacitance provides the second largest source of error.
- Die capacitance is extracted from the model using one of two methods. One is based on the response to a current source. The other is based on simulation of a driver and receiver and use Spice to find the value through optimization.

- Major EDA simulators that process IBIS models give essentially the same results as SPICE
- Differences between SPICE and IBIS simulations can normally be attributed to w DC errors in the IBIS I-V data. Mismatch between expected DC starting and ending values and those documented in the waveform tables cause overshoot glitches.
- The other main source of mismatch are related to the number of points in the V-T tables. IBIS currently has an overall 100 point limit that sometimes must be allocated between the different time shifted typ, and max columns. This can result in a 6% error in correlation. With 100 points per column, 99% correlation can be achieved. With 256 points, correlation is excellent and delays are with picoseconds.
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The conclusion was that IBIS model simulation can be as accurate as Spice model simulation. Other variables such as actual board impedances contribute far more deviation in actual measurement to simulated results than the accuracy deviations discussed in the correlation study.

THE JOY OF WEB MODELS Tom Dagostino, Mentor Graphics

A customer had asked Mentor to QC a set of IBIS models needed for a project. About 20 of them were obtained directly from semiconductor web sites. Most were quite acceptable and needed only minor corrections such as adding threshold and timing values. However, Tom had three really bad examples to share. While the review process involves more steps, the models illustrated in the presentation failed either or both the ibischk3 and visual inspection check.
The first model was a clock driver that had serious ibischk3 mismatches for rising and falling waveforms and I-V data.

- The pulldown table had zero current in the active region
- A visual inspection also revealed that C_comp value was constant for all three cases: typ, min, and max.

The second model was documented as a SCSI terminator. It passed ibischk3 with zero errors.

- The model type was listed as Output
- Had complete [Pulldown] and [Pullup] tables and [Ramp] data.
- The manufacturer has been contacted and stated that they would pass the information on. However, the manufacturer has not responded.

The third component had at least several bad models.
An _in model with a signal_name and Model_type Output had ibischk3 waveform errors. Vinh and Vinl were defined

- The typ, min, max temperatures were not correct
- The I-V table data contained zeros in the normal operating regions
- The [Ramp] data contained zeros.

Another _in model was documented as an I/O model with weak [Pullup] and [Pulldown] data and more [Ramp] data problems including negative time. Another had a constant voltage [Falling Waveform] table.

A model documented as an _out model, had meaningless and unrealistic conditions regarding the content of the data

- A max condition that was not consistent with the IBIS definitions
- Some tables had strange values inconsistent with typ, min, and max values.
- The [Pulldown] table had -0A values and [Ramp] data values of 0.
- For this component, the manufacturer has not yet responded to Tom's feedback.

Conclusion -- model developers need to do a better job in making models and QC'ing them before they are released.

LVDS MODELING Hazem Hegazy and Mohammed Korany, Mentor Graphics

Mohammed Korany reported on the problems associated with creating IBIS models for LVDS differential driver buffers with internal differential terminations. The problem is to extract the proper DC I-V data. He reviewed Three existing methods and then two new proposals. The last proposal gave the best results.
First Mohammed reviewed LVDS. He then reviewed two methods that have been proposed. The first one dealt with a voltage sweep at PAD with PADN connected to R_load and Vref. The second method used a mirrored negative current source at PADN. A third method was also presented where mirrored delta voltages are applied at PAD and PADN. All of these methods worked for 50 ohm loads and provided nearly overlaying IBIS and Spice simulations. Some DC offset was observed with 100 ohm terminations. However, all methods gave DC offsets when internal differential terminations existed in the LVDS model. Mohammed accounted for these offsets by showing the mathematical distribution of currents during extraction of the model.
Proposal I

- Similar to Method 3
- Has voltages attached to a Vmid value derived from averaging the low and high state voltages
- Produces better results
- Shows DC differences with internal terminators and the load equal to 100 ohms
- Only suppports using the R_fix value load

.
Proposal II

- Uses mirrored resistance changes with resistors connected to the Vref value
- Produces overlaying simulations for all cases.
- Results overlaied well for all differential conditions driving a lossy coupled differential line into a receiver load.

The internal differential resistor could be removed as another approach. But if the internal resistor is not know exactly – in the case of the driver does not have a high Z or input mode or if the Spice model is encrypted – this may not work

Other termination schemes including AC terminations may exist. It is important to get the model correct for DC and AC responses.
Mohammed concluded that LVDS IBIS modeling needs high DC resolution

Central themes of these presentations were defective models, correlation between IBIS and SPICE models, and LVDS simulations using different loads. At the moment there is no specific IBIS work going on to address LVD SCSI. Some degree of goodness was noted with different loads on the transmitter.

Larry also gave an update on the status of the “fallback schedule keyword” which is IBISese for SCSI’s version of precomp. The BIRD will be hatched by the next IBIS meeting over the next few weeks.

Support from Electronic Data Automation suppliers is important. To this end, folks from SSM that want the new keyword to be implemented should attend the following con call.

An IBIS open forum con call on March 02, 2001 at 8:00 AM to 9:55 AM Pacific time will take place. Dial in number 916 356-9200 , Reservation number 2-508084, passcode 6782941.

10. Matrix development for SSM

The following summarizes the present position for the SSM matrix. This matrix is a concise description of the methodology to be used for the respective areas of the point to point SCSI bus segment. Several of the areas were significantly modified at this meeting. Note that the multidrop areas have not yet been identified.

This section contains some repeated information from the last minutes as it continues to be relevant and current.

10.1 Transceiver chips: owner, Dean Wallace (need new owner)

Interface is at packaging pins
Model types: Behavioral only (because it is the only transportable type)
Data patterns: TBD
ISI compensation: required but not presently believed compatible with IBIS capability – this means that IBIS will have to be enhanced.
Single line required - cross talk from non SCSI sources not considered in the model, SCSI line cross talk is not significant within the transceiver. Therefore multiline models are not required for transceivers. (Possible risk with some package types.)

10.2 Bus segment termination: owner, Paul Aloisi / Don Getty

No new content information.

Interface is at package pins
Model types: Either circuit or behavioral
Terminator type: multimode
Single line only

10.3 Host bus adapter / target board (transceiver board): owner, Lee Hearn

Interface is at transceiver board connectors used for the SCSI link (at the board side of the connector - not including the connector), transceiver chip pins, terminator chip pins, unused connectors are part of the board
Model types: Circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

10.4 Mated connectors: owner, Martin Ogbuokiri

No new content information.

Interface is at transceiver board and the beginning of the cable assembly transition region
Model types: Circuit
Connector types: VHDCI, SCA-2, HD68
Mounting style: thru hole, SMT,
single line, multiline

Connector models are in place at the Molex web site and pointers are now in place on the T10 site.

10.5 Transition regions: owners, Bob Gannon, Greg Vaupotic

Interfaces are at the connector termination and the uniform media
Model types: circuit
Construction types: twisted flat, round fanout, laminated round, IDC flat?
Single line multi-line

A start was made in this area – see Bob Gannon presentation above.

10.6 Cable (bulk cable): owner, Jie Fan, Zane Daggett, Greg Vaupotic

Interfaces are at the beginning of the cable assembly transition region on either end.
Model types: RLGC
Cable types: flat, round shielded, round unshielded twisted flat?
Single line, multiline

10.7 Backplane: owner, Larry Barnes

Interfaces: connectors mounted on the backplane, directly mounted components, (this subject is still not settled)
Model types: circuit
PCB construction: edge, broadside, dielectric type / thickness, vias, pads, discontinuities
Single line, multiline

Issue: how to handle the unmated connectors on the backplane. Two sub issues: (1)lack of existence of unmated connector models and (2) convergence of the simulation with dangling open circuits. The latter can be handled by adding a high value resistance to the open circuit to "fool" the simulator.

10.8 Cable assemblies, owner TBD

Interfaces: connectors
Model types: circuit (possible combination of circuit and behavioral)
Constructions: point to point, multidrop

10.9 How to develop IBIS model annex, Barnes

11. Simulation integration strategy

Determine the goal of the simulation (examples: validate the basic behavior of a new component in a system, troubleshooting guidance, qualification of the signal integrity in a specific configuration, characterization of the expected EMI performance)

Determine the specific characteristics that are sought (example: ??)

Define the topology

Define the collection of components

Obtain the models for all the components

……subject discussion truncated – will continue next meeting.

11.1 System configurations - Topology

[Need pictures for below]

The following is a starting list of system configurations that need different considerations from a modeling perspective. Note that a device may be a SCSI expander.

1. Basic structure shown in the trial simulation work (single initiator/cable/single target on backplane)

2. Basic structure shown in the trial simulation work (single initiator/cable/multiple targets on backplane)

3. Expander isolated backplane with multiple targets on backplane

4. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). All connectors have devices attached.

5. Multi-drop flat cable connected to a single HBA board (terminator on cable on one end and on the HBA on the other end). Only the far end connector has a device attached - all other connectors have no devices attached - requires an unmated half-connector model.

6. Single target in an enclosure with a cable connection on the enclosure bulkhead to a round cable to an HBA in a different enclosure

11.2 Data patterns, Bill Ham (new owner)

11.3 Data rate, Dean Wallace (need new owner)

12. Tools:

Not discussed at this meeting

13. Document framework, Barnes

14. Should the group standardize on the IBIS connector matrices?

The following was copied from a recent IBIS meeting which shows the present status.

CONNECTOR SPECIFICATION Gus Panella, Molex

Gus Panella reported on the progress of the IBIS Connector Specification and reported on some of the changes:

- Removal of Physical Map because of unnecessary complexity
- Distinction of Side_A and Side_B pin maps
- Clarification of [Redistribution] Specific to mean comments are in the Header section
- Some number of pins, rows, and columns ranges to document physical limits
- More [Cn_Row_Swath] and [Cn_Column_Swath] distinction and edge definitions and usage

Gus stated that the current discussions involve following the IBIS-X group header suggestions, where practical. These include bracketing the header with [Begin Header] and [End Header] keywords.
He concluded that the document is reaching technical completion. The plan is to release the document for full IBIS Committee technical review and comments while the editorial cleanup of the document is being done.

IBIS CONNECTOR SPECIFICATION: PRELIMINARY PROPOSAL FOR A PIN NAMING LANGUAGE Ian Dodd, Cadence Design Systems

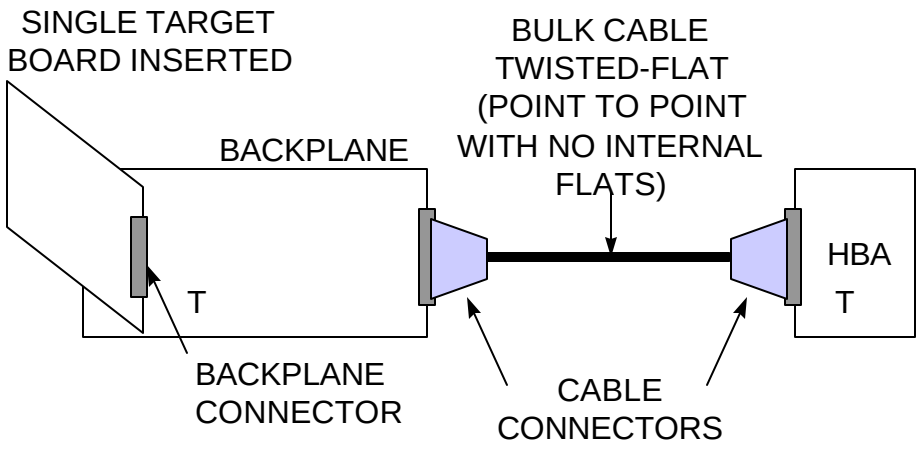
As part of the Connector Specification presentation, Ian Dodd displayed and discussed aspects of a proposal for pin naming language. The main points of the proposal are:

- Adopts C - like code style including C style formatting statements
- Predefines certain variables ROW, COLUMN, SIGNAL_NAME, and PIN_NAME
- Presumes all variables are integers and do not need to be declared
- Includes simple math operations and conditionals
- It can easily specify incrementing characters through addition
- The proposal might be compatible with the IBIS-X macro language.

There was no conclusion to this issue in this meeting. Resolution needs to wait until IBIS actually has this option available.

15. Creation of a trial basic composite simulation

The group tweaked the trial basic composite simulation effort defined in the last meeting. The general configuration to be considered is shown below:



TERMINATORS, T, ARE ATTACHED TO THE BACKPLANE AND HBA BOARDS

DRIVERS AND RECEIVERS AND ATTACHED TO THE TARGET AND HBA BOARDS

This is intended to be used as an example of a realistic complete SCSI segment and is expected to show where we have weaknesses in the concepts and model interfaces.

The general idea is for models of each element to be supplied in the form previously recommended and to actually create an overall integrated model that will yield waveforms.

Owners for each component were re-assigned as follows:

Backplane (named “Starter”): Database, IBM (Bill Troop); Parameter extraction from data base, IBM / LSI Logic (Bill Troop / Larry Barnes)

Backplane connector, Molex

Terminators, TI (Paul Aloisi)

Target Board and driver, Seagate (Umesh Chandra)

HBA Board and driver, IBM using LSI transceiver model and TI terminator w/Molex connector (Bill Troop)

Bulk cable media, Amphenol Spectra Strip (Greg Vaupotic)

Cable connector, Molex

Overall integration of pieces, IBM (Bill Troop)

A preliminary report is expected from Bill Troop by the April SSM meeting. This means that all component level models must be given to Bill in time for him to meet this schedule.

Paul Aloisi is actioned to contact Seagate to ensure that the target board IBIS model (for Ultra160 chips) is delivered to IBM in time for him to meet his April deadline.

16. New business

17. Next meetings

Approved schedule:

March 13-14, 2001 [SSM editing] 9AM to 5PM both days, Colorado Springs, CO (LSI Logic)

April 4-5, 2001 1:30PM to 6 PM 04/04; 9AM to 6PM 04/05 Worcester, MA (Madison)

Requested schedule:

June 13-14, 2001 1:30PM to 6 PM 06/13; 9AM to 6PM 06/14 New Haven, CT (Amphenol Spectra Strip)

August 15-16, 2001 1:30PM to 6 PM 08/15; 9AM to 6PM 08/16 Orange Co, CA (TI)

October 24-25, 2001 1:30PM to 6 PM 10/24; 9AM to 6PM 10/25 Colorado Springs, CO (LSI Logic)

December 12-13, 2001 1:30PM to 6 PM 12/12; 9AM to 6PM 12/13 Guadalajara, MX (JPM)

18. Action Items:

18.1 Action items from previous meetings

Status as of this meeting is shown.

Larry Barnes will hatch a BIRD at IBIS to incorporate transmitter ISI compensation as defined by SPI-4 (pre compensation).
Status: done

Bruce Manildi to provide access information for the Seagate transceiver models to the T10 web site.
Status: A commitment now exists from the chip supplier to Seagate for IBIS models (no precomp). Encrypted HSPICE models are currently available from Seagate. T10 web site info still needed. - carried over with significant progress.

Richard McMillan to provide access information for the Adaptec transceiver models to the web site.
Status: The present status of this item is not known -- carried over

Jie Fan, Madison Cable to provide access info for a cable media model to the T10 web site.
Status: model is done, verified and will be made available in circuit form - still needs info supplied to T10 web site - carried over

Bob Gannon to produce matrix of transition regions and issues with each.
Status: still partially done

Zane Daggett, Hitachi, to provide cable media models to the SSM web site (per last meeting minutes).
Status: data point collected, expect posting before next meeting (round 30 AWG solid will go up first followed by micro quick twist - carried over

Paul A to send emails to all folks with open action items on Tuesday of each week (until the action item is completed).
Status: ongoing

Larry Barnes to take the material in the SPI-3 and SPI-4 document relating to the signal budget and figure out how to incorporate into the SSM document
Status: carried over

Larry Barnes to send emails to all folks with open document issues on Tuesday of each week (until the issue is closed).
Status: ongoing

Section editors to provide material to Larry for the next revision of the document.
Status: ongoing

Bill Ham to add the interoperability material to his section
Status: partially done

Greg Vaupotic to post the document relating to reading the Ansoft matrix.
Status: carried over

18.2 New action items from present meeting

TI (Don Getty) to post model info for terminators to the T10 web site.
Status: new

Bob Gannon is actioned start a group of cable assembly folks to create a transition region model using Gigatest as the vehicle.
Status: new

Jason is actioned to provide a draft for the instrumentation interface section of the document.
Status: new

19. Adjourn

The meeting adjourned at 6:00 PM