

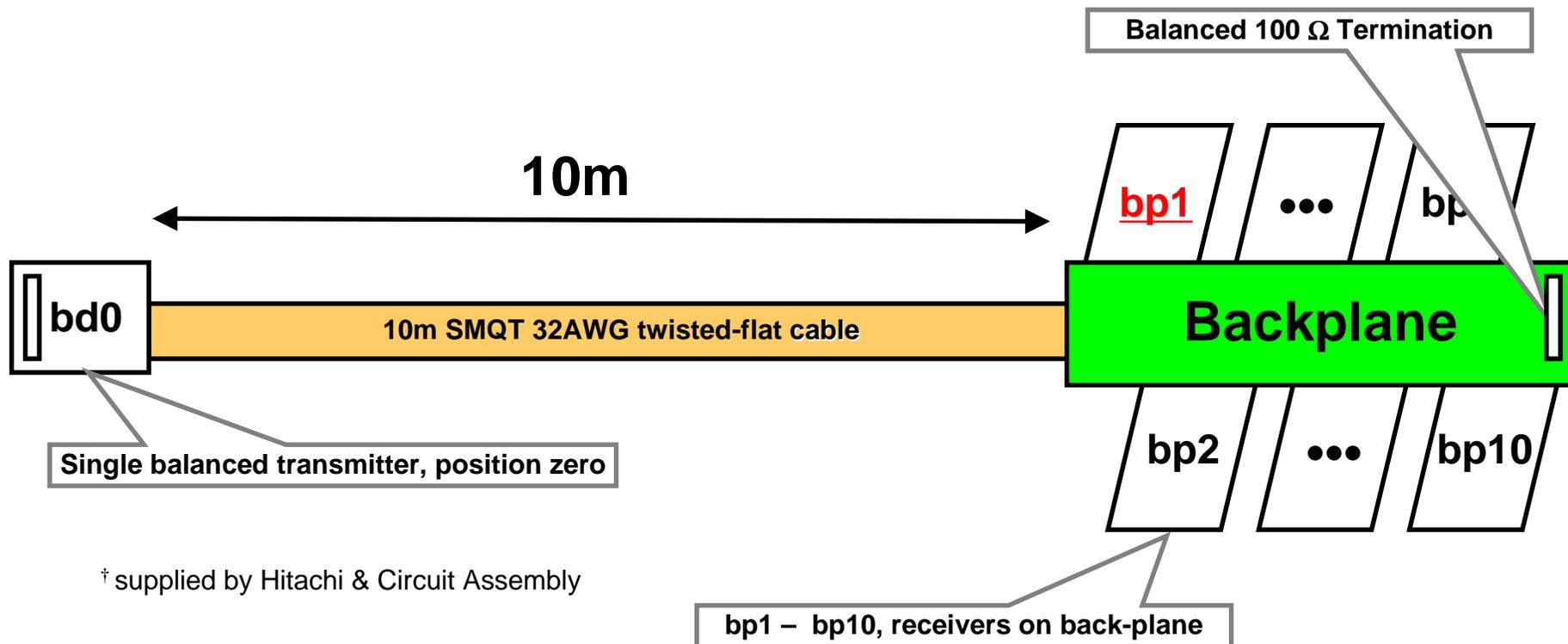
Ultra320 SCSI into a Fully Populated 10-slot Backplane

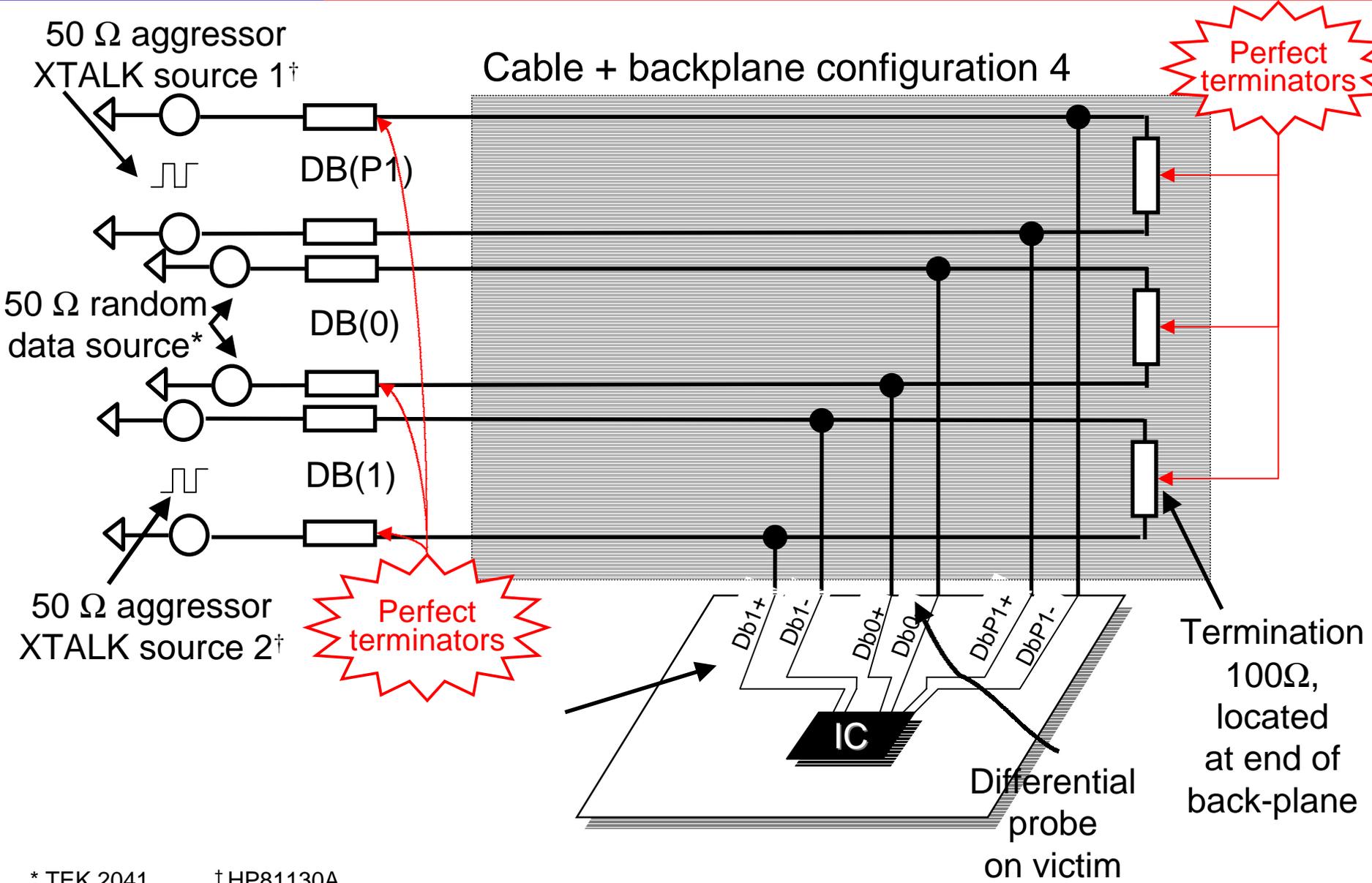
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- **We wanted to obtain measurements on additional standard “worst-case” system configurations.**
 - The system used to gather data in this presentation is from a major manufacturer.
 - This system has low backplane impedance resulting in greater than 50% attenuation @ 80 MHz.
- **Margins for this system were evaluated with the same techniques as used for our other Ultra320 data:**
 - The signals were measured to find the eye opening with ISI, reflections, and crosstalk including: amplitude errors, timing shift errors, and miscellaneous noise.
 - Transmitter driving voltage: +/- 400mV.
 - Transmitted Pattern: 2 μ s of “101010...” training pattern followed by 8 μ s of random data.
 - The equalizer input signals are captured differentially with a Tektronix TDS694C oscilloscope by probing at the backplane.
 - The equalizer output signal is generated by Spectre, simulating in transistor level models and using captured data as input stimulant.

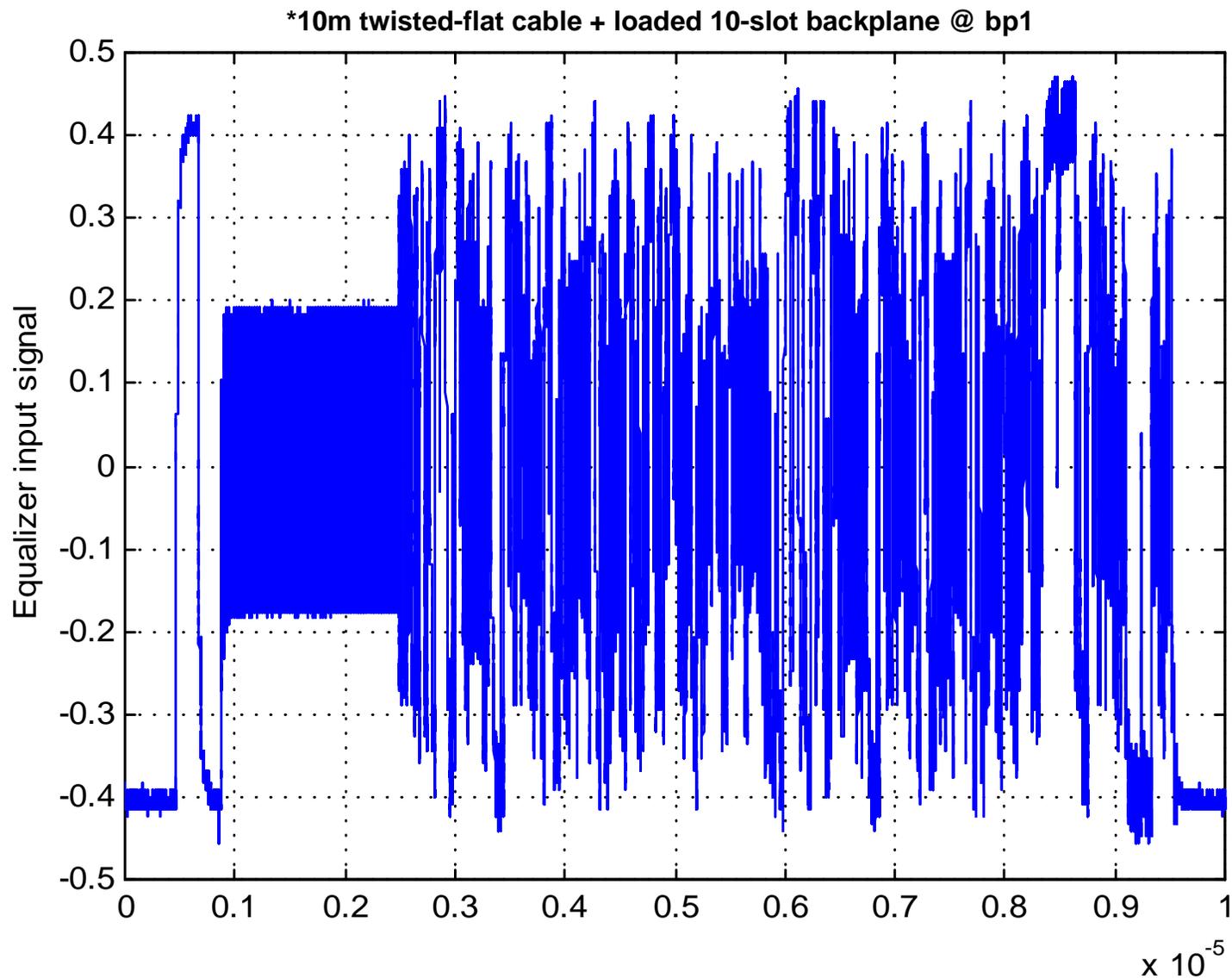
- Hitachi 10 meter 32AWG twisted-flat ribbon cable† plus 10-slot backplane.
- Waveforms captured @ 4Gigasamples per second.

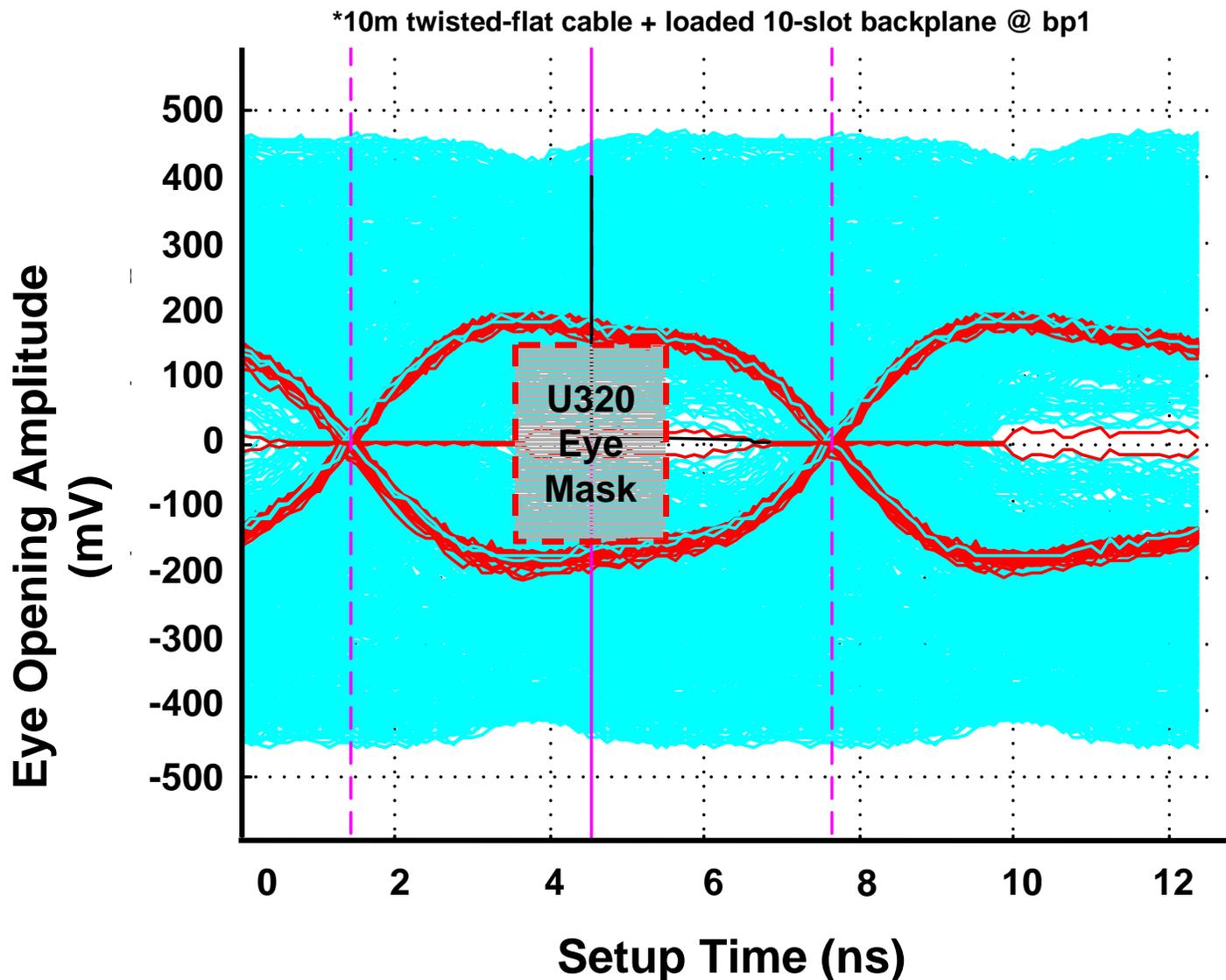




* TEK 2041

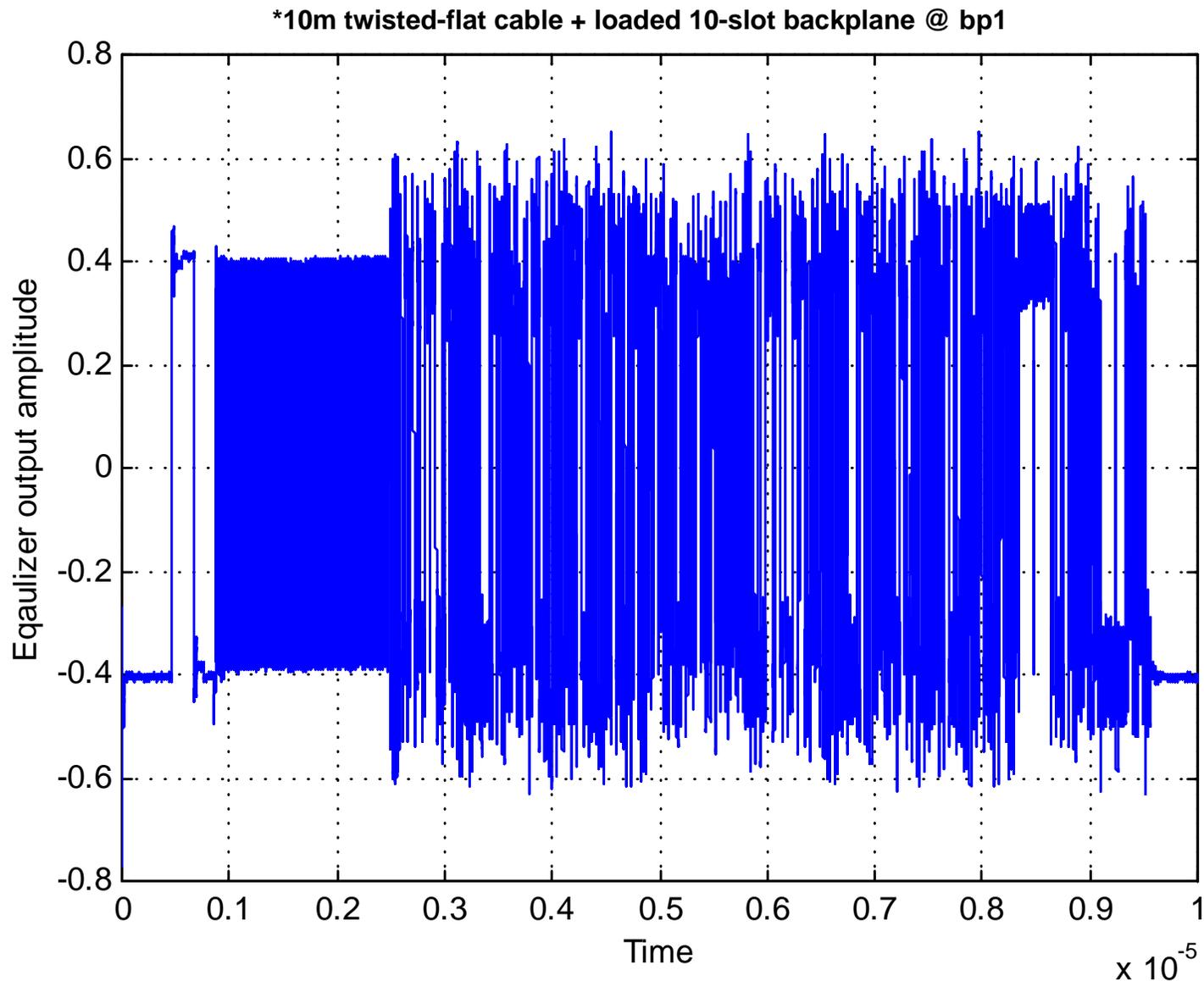
† HP81130A



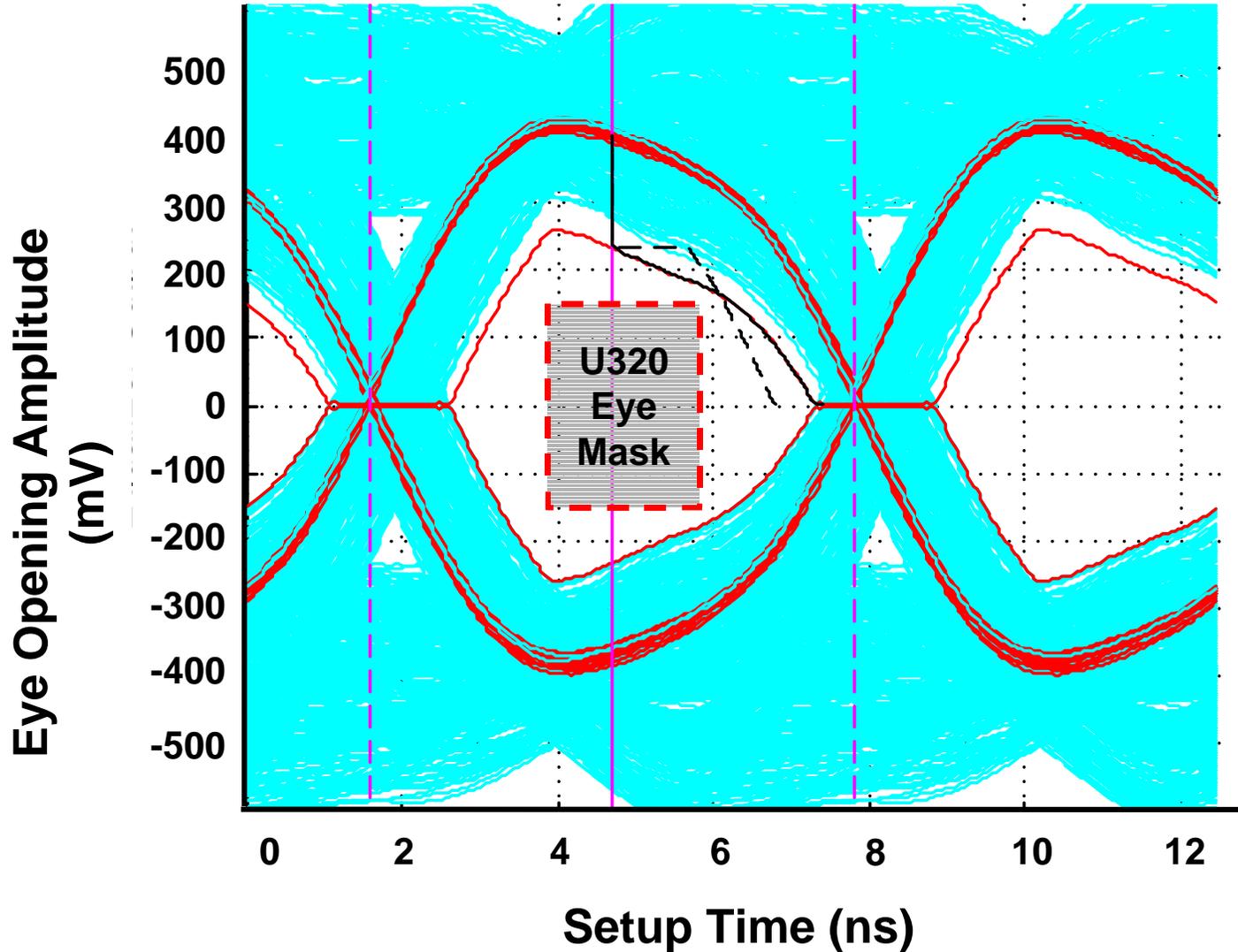


Conclusion: Failing Margin

(Increasing amplitude would still fail)



*10m twisted-flat cable + loaded 10-slot backplane @ bp1



Conclusion: Excellent Margin

