Accredited Standards Committee
X3, Information Processing Systems

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Project: X3T10.1/1146D
Ref Doc.: SSA-PH2 rev 3a
Reply to: John Scheible

To: X3T10.1 Membership
From: John Scheible

Subject: Changes to SSA-PH2 rev 3a proposal

BACKGROUND

This document documents the changes agreed to at the October plenary for SSA-PH2 rev 3a. The source of the input was from reflector traffic prior to the working group, and discussions during the working group. The changes will be rolled into SSA-PH2 rev 4. The input comes from Dave Instone, Dan Tsai, and John Scheible.

PROPOSAL

1) Add "Load" and "Coupling Element" to section 3. Definitions, symbols and abbreviations, since we introduced these two "definitions" May be we should change them to Internal Load and Internal Coupling Element because Load by itself might cause some confusion. It was decided not to define them.
2) Page 4 sec 3.2: I thought AWG stood for American wire gauge.
3) Page 6 Note 1: Vot should be Vit. Remember, this is the one place that Vdd should not be replaced with Vot.
4) Center Fig 4.
5) Page 8 7.1.2 Note 1: we removed line DRIVER fault detection from Annex F this note should be reworded for RECEIVER and put in 7.2.2
6) Page 9 7.1.3.1. Remove the second sentence which starts.. Line Driver measurements.... 96a165r2 Item Issue 3 Changes 3 refers
   also the sentence which says: Additional discrete capacitors between the scope probes and the port connector ground may be needed. is redundant as a sentence before it specifies a MAX of 1.5 pf not the 2 pf +/- of PH1.
7) Fig 7&11. Horizontal line strikes across the Coupling Element capacitor's two plates.
8) On my 4039 at 300 dpi the shading comes out as a lighter shade of black. May I suggest you shade in the bit enclosed by the eye and then change the wording of 'shall fall within the shaded area shown in the pulse mask in Figure 9' in 7.1.4 to:
   'shall remain outside the area shaded and be wholly contained between the V2 and -V2 voltage levels of the pulse mask in Figure 9'.
   This would result in a more normal eye representation. Do the same to the receiver eye as well, no change of words is required here. On an aesthetic note it would also look more normal if you showed the trailing triangle of the bit time preceding T0
9) There is no need to worry about references to the test values they are at least as good as they were before and prior to each table is text specifying the trigger conditions they apply to. In addition appendix E is specific in which table to use.
10) Regarding the actual values on table 3, 4, 7 and 8, I have checked them and have found errors in table 3 and table 4
    Table 3 and Table 4. 200 Mb/s T1: replace 0.47 ns with 0.25 ns (390-140)

Table 4 400 Mb/s T2: replace 1.75 with 1.85 (2500-200-200-250)/1000
Table 4 400 Mb/s T3: replace 2.22 with 2.10 (2500-200-200)/1000
Table 4 200 Mb/s T2: replace 3.50 with 4.19 (5000-280-280-250)/1000

11) Fig 13. We need to add "Load" and "Coupling Element" for each driver. Shall we also swap driver/receiver on one node so driver is "connected" to the receiver ? I also noticed that this is the only figure that driver/receiver have "small circle" to indicate differential +/- signals. Shall we update all other figures to be in line with the industry ?
12) Page 18 Sec 7.5: Para starting: The Lines shall have... a rho has missed the net. 375 ps not rhosec also last para/sentence PCS is not defined in 3.2 but it would be better if the abbreviation was not used here
13) John just noticed that if you change the eyes as my previous Email on eyes suggested then 7.5.7 will have to be amended to include the wording about v2 and -v2.
14) Table 13. Lower case for P/D/C for Port Device Connections. I am nit picking here.
15) Page 46 table 20: notes for Pin 3. The sentence- If optional power is not provided on pin 8 then pin 3 etc.. should be against pin 5 not pin 3. Remember, we always want logic ground present on the connector, that's why we re-instated it to the HSSDC connector.
16) Page 46 Table 21 and Page 50 table 23: Now that we allow a cable to have more than 5 conductors we should either drop the note at the end of both these tables or change them to NOTE- Pins x, x, x and x are not normally connected end to end.
17) Page 49 table 22: add in the notes against pin 4 logic ground the same notes that are against pin 3 of table 20 (less the bit deleted above of course)
18) See Table 20/Table 22 and 7.5 In the above note use 'Table 20' in table 21 and 'Table 22' in table 23.
19) 8.5.2. Change "The interface is polarized with" to "The contact interface is sequenced with make first, break last for pin 2 and 7" Lisa, isn't "polarize" generally used for plugging orientation ?
20) Annex G Fig. G.1. Driver should also includes "Load and Coupling Element".
21) Annex J, Table J.1, change last column from 100 MHz to 200 and 300 to 600.
22) Page 85 The last sentence of the spec: I think 'note generate' should be 'not generate'

EDITORIAL WORK STILL NOT DONE

In an effort to get rev 4 out, several editorial items were not done, including:

1) 2.1 - Need normative reference info for IEC 512-2 part 2.
2) Figures 9 and 12, the eye diagrams - The cross hatching comes out fine on Postscript, but some areas are two sets offset from each other on PCL format. Also the PDF shows it as dark shading. Investigate a better (more consistent) format.
3) Figures 9 and 12 - Could show the end of the preceding sexagon.
4) Figure 13 - removed the circles on the output, but the resister/capacitors were not added for consistency.
5) Figure 40 - Pin1 is italics and should not be.
6) Figure G.1 - Add the terminating resisters for consistency.

Sincerely,

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